A-705A

DIGITAL

MODULES

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MAYNARD, MASSACHUSETTS

digital MODULES

One-page introduction to each module series.

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Basic digital modules. See frequency desired.

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DIODE GATES

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Introduction p. 1
A brief description of analog and digital computers and number systems.

Basic Digital Circuits p. 7
How to construct a variety of general and special purpose logic circuits using DEC modules.

Appendices p. 63
Additional background to digital techniques.

Digital Modules p. 85
Detailed specifications of all modules and other DEC equipment. Use thumb index opposite. Modules come in two types of package and in three frequency lines, as follows:

	500 KC	5 MC	10 MC
Laboratory Modules	3000 Series	100 Series	5000 Series
System Modules	4000 Series	1000 Series	6000 Series

The specification pages are organized in two ways. First, they have borders and tabs colored according to frequency range: cinnamon for 5 mc, blue for 500 kc, orange for 10 mc. Second, they are grouped in five broad categories as shown in the column to the left (refer also to thumb index).

digital MODULES

A complete selection of solid state digital circuit modules in three compatible speed lines specially packaged for systems design, test and construction applications

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

SERIES CHARACTERISTICS
INVERTERS
CAPACITOR DIODE GATES
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FLIP-FLOPS
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SPECIAL AMPLIFIERS SLICERS, ETC.
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PREFACE

DEC Modules are a coordinated set of packaged digital circuits for building and testing computer systems. They are designed to be easy to understand and easy to use. People with no knowledge of Boolean algebra can perform logical designs, and those who like to use Boolean mathematics can very quickly implement their equations. Straightforward static logic is employed and only a small number of modules is needed for most systems because of the high driving capability of each unit.

Two types of packaging are available, Laboratory Modules and System Modules. Laboratory Modules, in aluminum cases, are quickly interconnected with patchcords between jacks which are integrated with a diagram, printed on the front panel, showing the logical operation of the module. Each System Module is a dip-solder printed circuit board mounted in an aluminum frame and furnished with a 22-pin Amphenol plug.

Both types of module come in three frequency ranges: 500 kc, 5 mc, and 10mc. All units are electrically compatible. Although timing characteristics depend upon the frequency range, integration of different frequency lines is simple.

Both types of module come in three frequency ranges: 500 kc, 5 mc, and 10 mc. All units are electrically compatible. Although timing characteristics depend upon frequency range, integration of different frequency lines is simple. Laboratory Module voltage requirements are −15, +10, and −3 volts. System Module voltage requirements are −15 and +10 volts; the 3-volt logic level is generated inside each module that requires it. Both Laboratory and System Modules have two +10-volt inputs for marginal checking.

	500 KC	5 MC	10 MC
Laboratory Modules	3000 Series	100 Series	5000 Series
System Modules	4000 Series	1000 Series	6000 Series

All modules use the same logical principles. These principles, together with typical applications of DEC Modules, are explained with numerous examples in Section 2 below. Section 1 provides a brief introduction to computers and number systems.

INTRODUCTION

Computers, like all machines, are tools for man's labor. They are in daily use for commercial, scientific and military applications, and new uses for them are being discovered at a tremendous rate. Computers influence many aspects of our daily lives: they process insurance premiums, airline reservations, checking accounts, and time cards, to name but a few uses. Hardly an industry is not affected by electric computation devices.

Most computers are of either the analog or digital type. An example of a simple analog computer is an automobile speedometer. A very simple digital computing device is the mileage indicator. Long before the first electronic analog computer was built about 20 years ago, various electro-mechanical computers were used. Two thousand years ago the Greeks developed complex analog devices, among them a device for determining the movement of the solar system which compares favorably with present day gunsighting mechanisms.

The basic difference between analog and digital machines lies in the manner in which they represent the quantities upon which calculations are to be performed. Each type has its particular advantages and disadvantages. In general the analog devices are better suited to applications where an analogy can be formed between the operation of a device and a mathematical process. Measurement is always involved and data changes smoothly, as represented by a curve. Digital computers, on the other hand, manipulate discrete numerical quantities. These quantities may represent alphanumeric information, data, or instructions to the computer. Digital computers are best suited for complex arithmetic computations, logical and decision-making operations, and high volume business-record processing. Analog and digital elements are sometimes combined in a single computer for special purposes.

Digital techniques are finding increasing use in a wide variety of engineering applications, particularly in solving timing and control problems. Digital units are used to control automatic milling machines and to regulate processes in oil refineries. Complex data processing in satellite tracking is performed by digital equipment. As might be expected, the computer industry itself finds many uses for computer-type circuitry: Experimental setups for the development of new techniques and test equipment for subassemblies and completed units are two examples. The list of applications for digital techniques is almost endless, and the list is expanding steadily.

NUMBER SYSTEMS

Early number systems were crude and awkward. A simple system, using a mark for each unit, cannot be used to express large quantities such as a thousand. Later systems, such as Roman numerals, were a great improvement but still extremely difficult to manipulate in ordinary arithmetic. With the arabic or decimal number system which we use today, common arithmetic operations which correspond to true-to-life operations can be defined and used easily.

The decimal number system uses ten symbols representing the quantities zero through nine. Other numbers are constructed by assigning different values (or weights) to the position of the symbol relative to the decimal point. For example, the number 8 represents eight units, while the number 80 represents eighty, and number 800 eight hundred. It is readily apparent that each position in the number has a value ten times the value of the next position to the right. In other words, every positional value is a multiple of ten and can be expressed by ten raised to some power. The tens position is 10^1, the hundreds position 10^2, the thousand position 10^3, etc. The ones position is 10^0, or 1 (as is any number raised to the zero power).

The same progression can also be extended to the right of the decimal point, but here the exponents will be negative. For example, the first position to the right of the decimal point is the tenth position; it has a weight of 10^{-1} or $1/10$. The positional value of the next position to the right is 10^{-2} or 1/100, and so on.

Ten is not a magic number. We find the decimal system easiest to use only because we know it so well. It would be just as simple to have twelve symbols or eight symbols or two symbols, or any other number of symbols. Whatever system we choose, however, the positional values must be multiples of the number of symbols in the system. If our system has three symbols, we say it has a radix of three, and each positional value will be some power of three. Below is the skeleton of a general number system with a radix R. Examples of counting in different number systems are illustrated in Figure 1.

$$R^N \cdots R^3\ R^2\ R^1\ R^0\ .\ R^{-1}\ R^{-2}\ R^{-3} \cdots R^{-N}$$

BINARY NUMBER SYSTEM

Since the binary number system uses two symbols, it has a radix of 2 and the positional values are powers of 2. Examination of the binary counting sequence, Figure 1, shows that the binary number system follows the skeleton system described earlier. The method of performing arithmetic operations in binary numbers is therefore the same as for decimal numbers. For example, $0 + 0 = 0$, and $0 + 1 = 1$. Since there is no symbol for two, however, $1 + 1 = 0$ and 1 to carry. The tables for performing arithmetic operations in binary are given in Figure 2. With only two symbols the tables are considerably simpler than in the decimal number system. Much simpler computer circuitry is the natural consequence.

	DECIMAL	DUODECIMAL	OCTAL	BINARY
Positional Values (in decimal)	tens ones	dozens ones	eights ones	sixteens eights fours twos ones
	0	0	0	0
	1	1	1	1
	2	2	2	1 0
	3	3	3	1 1
	4	4	4	1 0 0
	5	5	5	1 0 1
	6	6	6	1 1 0
	7	7	7	1 1 1
	8	8	1 0	1 0 0 0
	9	9	1 1	1 0 0 1
	1 0	A	1 2	1 0 1 0
	1 1	B	1 3	1 0 1 1
	1 2	1 0	1 4	1 1 0 0
	1 3	1 1	1 5	1 1 0 1
	1 4	1 2	1 6	1 1 1 0
	1 5	1 3	1 7	1 1 1 1
	1 6	1 4	2 0	1 0 0 0 0
	1 7	1 5	2 1	1 0 0 0 1
	1 8	1 6	2 2	1 0 0 1 0
	1 9	1 7	2 3	1 0 0 1 1
	2 0	1 8	2 4	1 0 1 0 0
	2 1	1 9	2 5	1 0 1 0 1
	2 2	1 A	2 6	1 0 1 1 0
	2 3	1 B	2 7	1 0 1 1 1
	2 4	2 0	3 0	1 1 0 0 0

Figure 1

Counting in different number systems. The duo-decimal number system has a radix of twelve; the symbols A and B are used here to represent the quantities ten and eleven respectively. The octal system has a radix of eight and the binary system a radix of two.

Binary Addition
A + B = S (Sum)
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 0 & 1 to carry

Examples

```
  101101        101101
+   1010    +    1100
--------      --------
  110111        111001
```

Binary Subtraction
A − B = D (Difference)
0 − 0 = 0
0 − 1 = 1 & 1 to borrow
1 − 0 = 1
1 − 1 = 0

Examples

```
  101101        101101
−   1100    −   11001
--------      --------
  100001        10100
```

Binary Multiplication
A · B = P (Product)
0 · 0 = 0
0 · 1 = 0
1 · 0 = 0
1 · 1 = 1

Example

```
  101101
     101
  ------
  101101
 000000
101101
--------
11100001
```

Binary Division
A ÷ B = Q (Quotient)
0 ÷ 0 = ?
0 ÷ 1 = 0
1 ÷ 0 = ?
1 ÷ 1 = 1

Example

```
      1001
  ----------
101 | 101101
      101
    -----
      0001
      0000
    -------
        10
        00
      -----
       101
       101
```

Figure 2. Binary arithmetic

BINARY-DECIMAL CONVERSION

Binary-decimal conversion may be performed by hand using the methods outlined in Figure 3. A binary number is converted to decimal simply by adding the positional weights of all those positions where a 1 appears.

Decimal to binary conversion is more a process of trial and error. First, subtract the largest power of 2 which will go into the number that is being converted. Repeat this process on the remainder until the remainder is equal to zero. The binary number then has ones in those positions with the values corresponding to the powers of two which were substracted; all other positions are zero.

Since computer inputs and outputs must often be in decimal notation, a variety of special codes are used in computers. These are referred to as binary coded decimal (BCD) because they use only two symbols, but can be directly converted to decimal. In some cases these codes are used only in the input-output section of the computer while the internal computer work is done in binary. In other cases all of the arithmetic operations are done in the binary coded decimal. A large variety of such codes can be constructed and methods for performing arithmetic operations depend upon the code. More information on codes is included in the Appendix and in the reference books listed in the bibliography.

```
(32   16   8   4   2   1)
 1    0    1   1   0   1    =   32 +  0 + 8 + 4 + 0 + 1 = 45
           1   0   1   0    =    0 +  0 + 8 + 0 + 2 + 0 = 10
 1    1    0   1   1   1    =   32 + 16 + 0 + 4 + 2 + 1 = 55
```

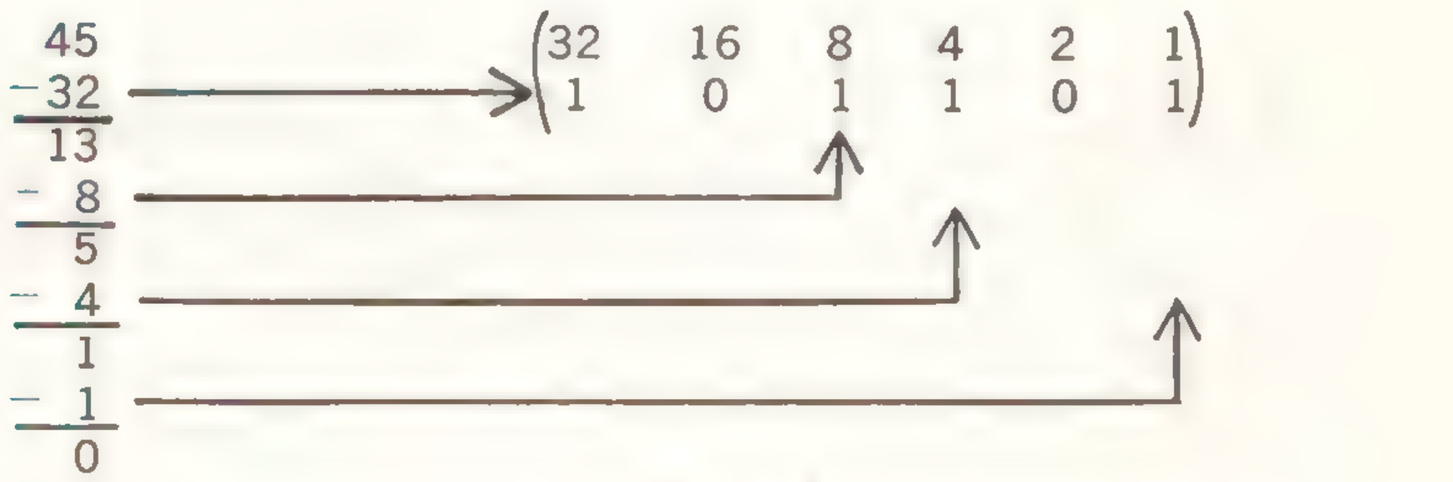


Figure 3.
Binary to decimal and decimal to binary conversion

OCTAL NUMBER SYSTEM

As the name implies, the octal number system has a radix of eight, i.e. it uses eight discrete symbols: 0, 1, 2, 3, 4, 5, 6, 7. The positional values in the octal number system are powers of eight. The octal number system is widely used by digital engineers and computer programmers. It can easily be converted to binary and at the same time it is considerably easier to work with than binary where a long string of zeros and ones becomes cumbersome.

The binary-octal conversion may be performed quite simply due to the fact that 8 is the third power of 2. This produces a direct correlation between the successive three-bit groups in a binary number and the octal digits. That is, an octal number may be converted to binary digit by digit, while from decimal, the entire number must be converted to binary. Octal to binary conversion is shown in Figure 4.

Arithmetic operations in octal are quite similar to the operations in decimal. A more detailed discussion of this can be found in some of the reference books in the bibliography.

NOTATION

When there may be some doubt as to the number system being employed, it is customary to add the radix of the number system (in decimal) as a subscript to the number. For example, 777_8 indicates that this is the number 777 written in the octal number system. The same number in the decimal system would be 511_{10}. Obviously, in working with different number systems it is extremely important to be certain which system is being used. For example, take that tricky little question: "What's 2 and 2?"

$2 + 2 =$ Meaningless for radix of 2
$2 + 2 = 11_3$
$2 + 2 = 10_4$
$2 + 2 = 4_{5 \text{ or more}}$

Octal	Binary
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
10	1000
11	1001
.	.
.	.

Examples

Octal	Binary
426	100 010 110
166	1 110 110

Figure 4.
Octal to binary conversion

BASIC DIGITAL MODULES

THE TRANSISTOR INVERTER

Most logical operations with DEC Modules are performed with saturating PNP transistor inverters. When a junction transistor is turned completely on or "saturated," the collector is practically a short circuit to the emitter of the transistor. If the emitter is at ground in this condition, the output from the collector will also be at ground voltage.

When a junction transistor is turned completely off or "opened," the collector-to-emitter path is practically an open circuit. If the collector is connected to a clamped load resistor, the collector will be at −3 volts.

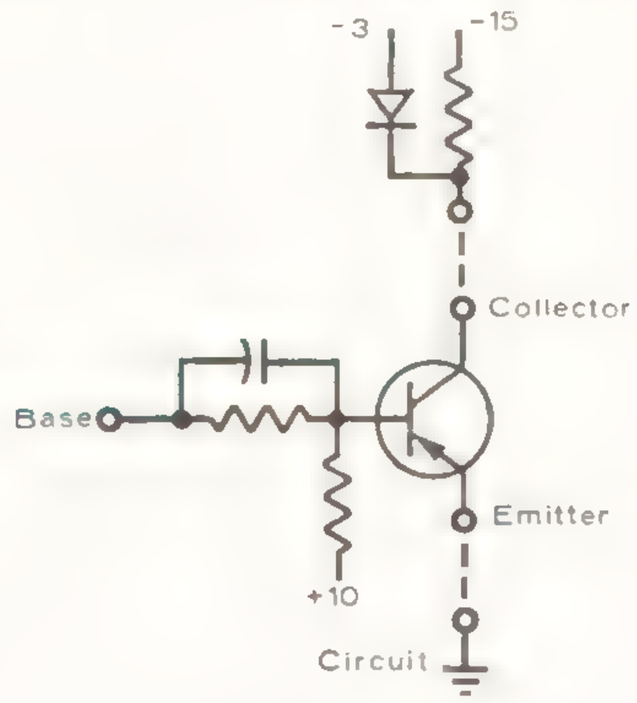


Figure 1

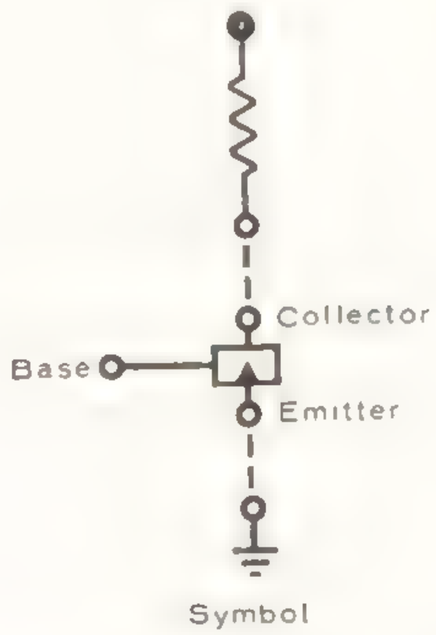
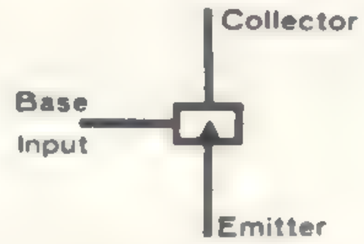


Figure 2

Figure 1 is a schematic drawing of a DEC Inverter and Clamped Load Resistor. The capacitor shunting the input resistor is used to provide overdriving current to the transistor during input level changes, thus switching the transistor much more rapidly. The resistor to +10 volts biases off the transistor to protect against noise voltage. The load resistor is clamped to −3 volts with a diode so that, when the transistor is off, the output signal is always at −3 volts regardless of the loading on the inverter output.

To simplify logic drawings, the symbology of Figure 2 is used. When the input is negative, the output is "shorted" to ground. When the input is positive or at ground level, the transistor is open circuited and the output, if connected to a clamped load resistor, is at −3 volts.

DEC SYMBOLOGY

A small rectangle with an enclosed solid triangle is an inverter.	 INVERTER
A resistor with a large solid dot is a standard DEC clamped load resistor.	CLAMPED LOAD
The solid diamond is a logic level for which the assertion level is −3 volts.	LEVEL — NEGATIVE
The open diamond is a logic level for which the assertion level is ground.	LEVEL — GROUND
The solid arrowhead is a negative pulse (from ground).	PULSE — NEGATIVE
The open arrowhead is a positive pulse (from ground).	PULSE — POSITIVE
Arrowheads (or diamonds) are used at all branch points to indicate signal flow.	

DEC LOGIC

Dual-polarity level logic is used with DEC Modules. The "logical" voltage levels are −3 volts and ground. Correspondence between the logic state, ONE or ZERO, and the voltage levels of −3 and ground, is indicated at each point in the "logic" drawing by a diamond. This diamond defines the necessary voltage level for the action desired. A solid ◆ diamond denotes a −3 volt level for assertion and a hollow ◇ diamond denotes a ground level for assertion. When two uses are to be made of the same level a split ◆ diamond is used.

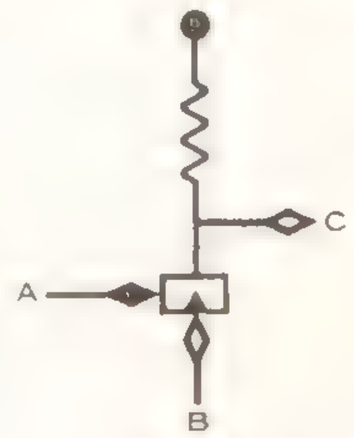
With these symbols, the logical designer is able to produce in one step a logical drawing which can be directly implemented with DEC Modules. This method also allows a combination of amplification and gating without added inversions, usually necessary if a single logical state is always associated with a single logical voltage level.

The illustrations below show how the DEC logical method is used to form an AND gate or an OR gate from a single inverter. The inverter serves as an AND gate when the definitions are:

A = 1, if negative (−3V)

B = 1, if ground

C = 1, if ground



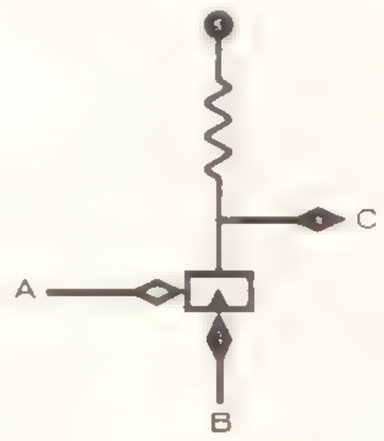
AB = C

The same inverter serves as an OR gate if the definitions are:

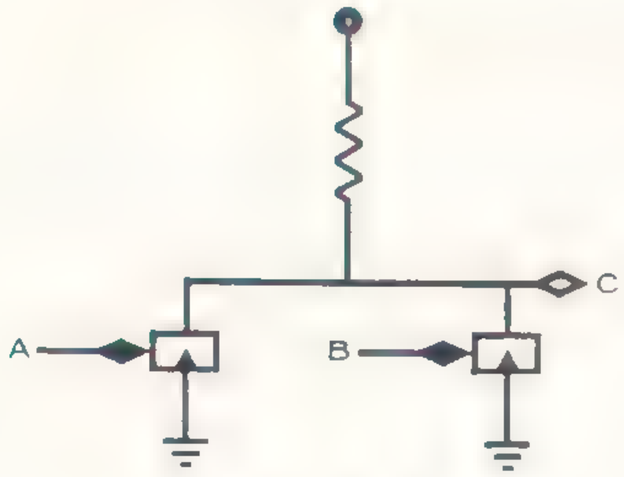
A = 1, if ground

B = 1, if negative

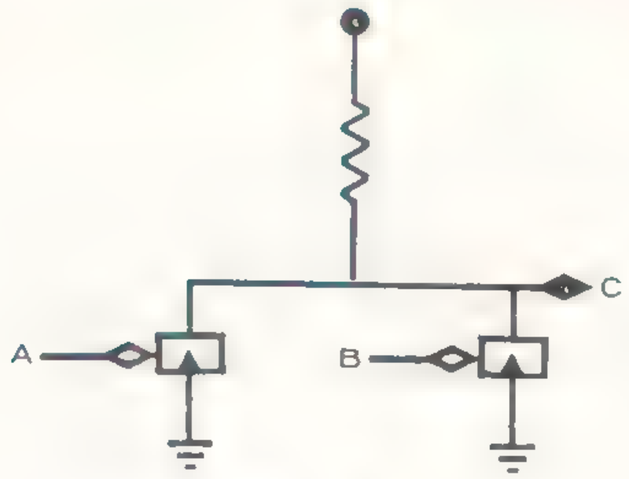
C = 1, if negative



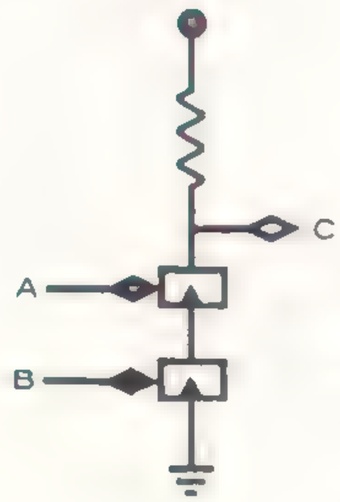
A + B = C



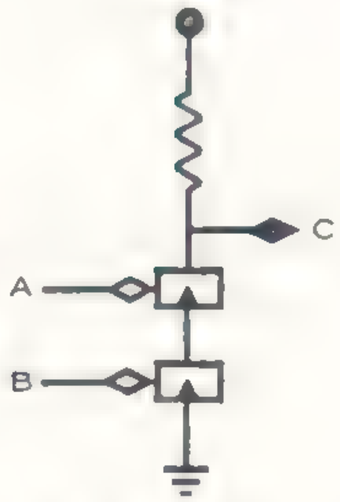
A + B = C



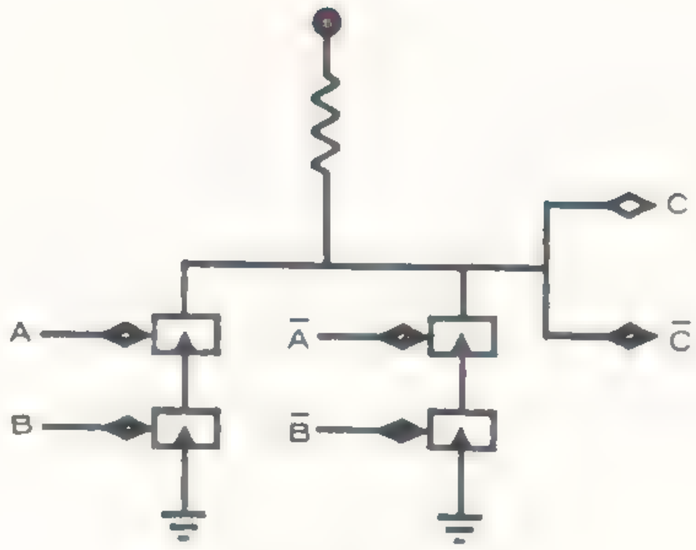
AB = C



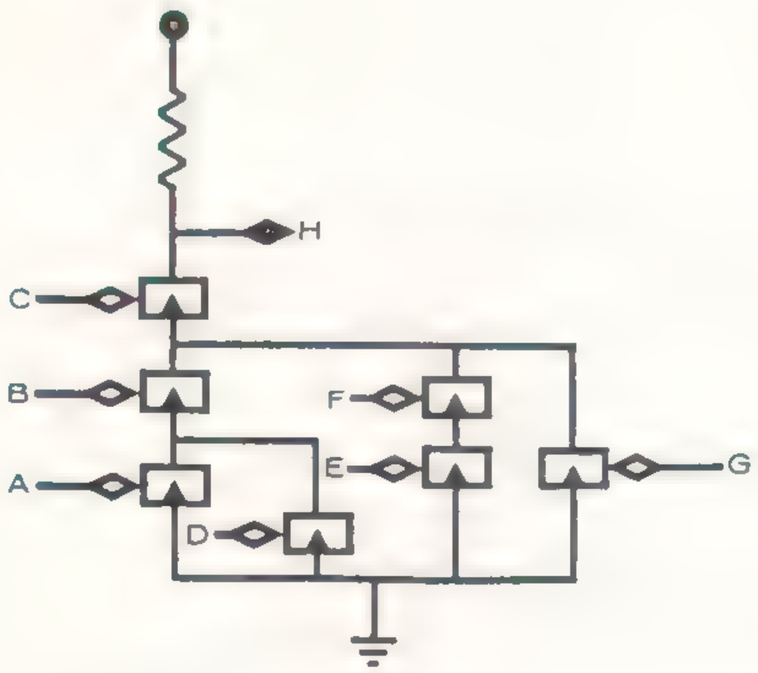
AB = C



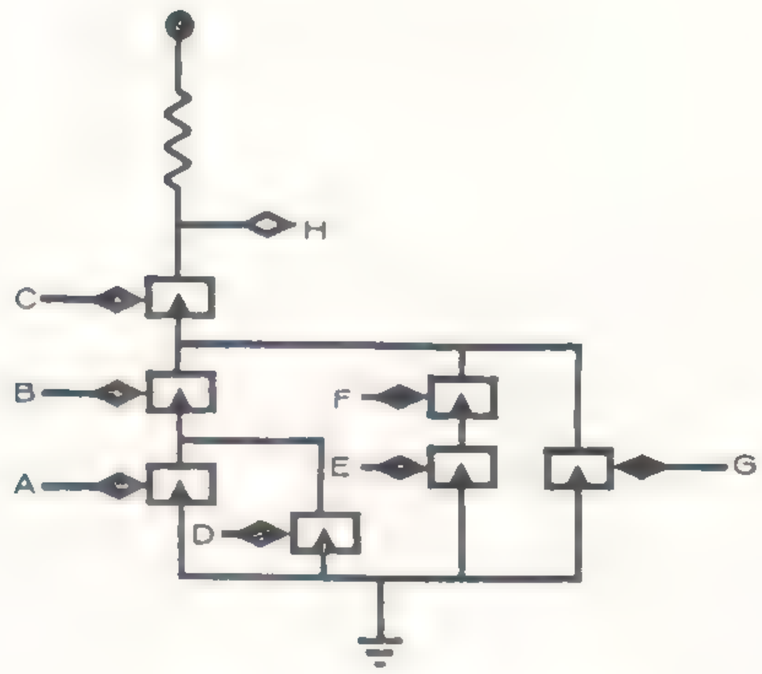
A + B = C



$C = AB + \bar{A}\bar{B}$
$\bar{C} = \bar{A}B + A\bar{B}$



$H = C + (B + A \cdot D) \cdot (E + F) \cdot G$



$H = C \cdot [B \cdot (A + D) + E \cdot F + G]$

Figure 3 Common AND and OR gate possibilities

After the desired logic has been performed with level gates in series and parallel combinations, the results can be sampled and read into a flip-flop or other active element with a DEC Standard Pulse. This may be accomplished by applying the conditioning level to the emitter of an inverter and the sampling

pulse to the base of the same inverter. The collector of this inverter (or the collector of a diode gate used in the same manner) can be used to drive one flip-flop or other active element. Since the sampling pulse must always have a sharp leading edge in order to activate the flip-flop or other element, the pulse is never used in performing logic. It is only used in sampling a logic level.

In lower speed systems it is possible to differentiate a changing voltage level to produce the sampling pulse. This may be done with the capacitor-diode gates in DEC's 4000 Series of low speed modules. The level indicating the results of the logic is applied to the conditioning level input of the capacitor-diode gate, and a level change is applied to the differentiating input. The resulting signal is a short pulse which may be used to read the results of the logic into a flip-flop.

The use of a pulse sampling or differentiating level type system involves slightly different methods of implementing a given system. However, the basic principles are the same in both systems, and conversion from one type of unit to another is a simple matter.

DIODE LOGIC

Diodes may be added to the inverter input in order to form a logical AND or a logical OR gate. The circuit in Figure 4 illustrates a diode gate which can serve as an OR gate for negative signals or an AND gate for ground signals. When input pin A or input pin B is held at a negative voltage, the base input to the inverter will also be negative and the inverter collector will be brought to ground. When both A and B are ground voltage, the positive bias on the base assures that the transistor will be cut off and that the collector of the inverter will be at a negative voltage. If either pin A or pin B is unconnected, the circuit will act as a simple inverter.

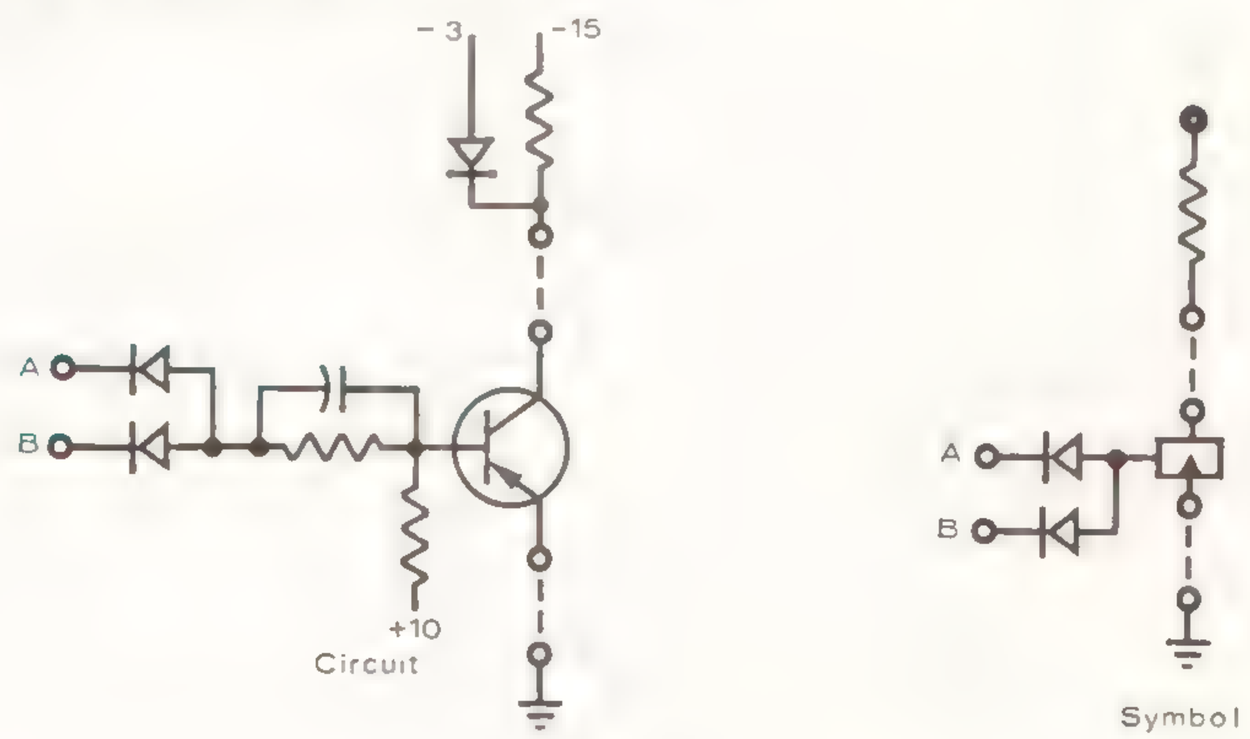


Figure 4

Figure 5 shows a similar diode gate with the diodes in the reverse direction and a negative bias voltage. This circuit will operate as an AND gate for negative signals and an OR gate for ground levels.

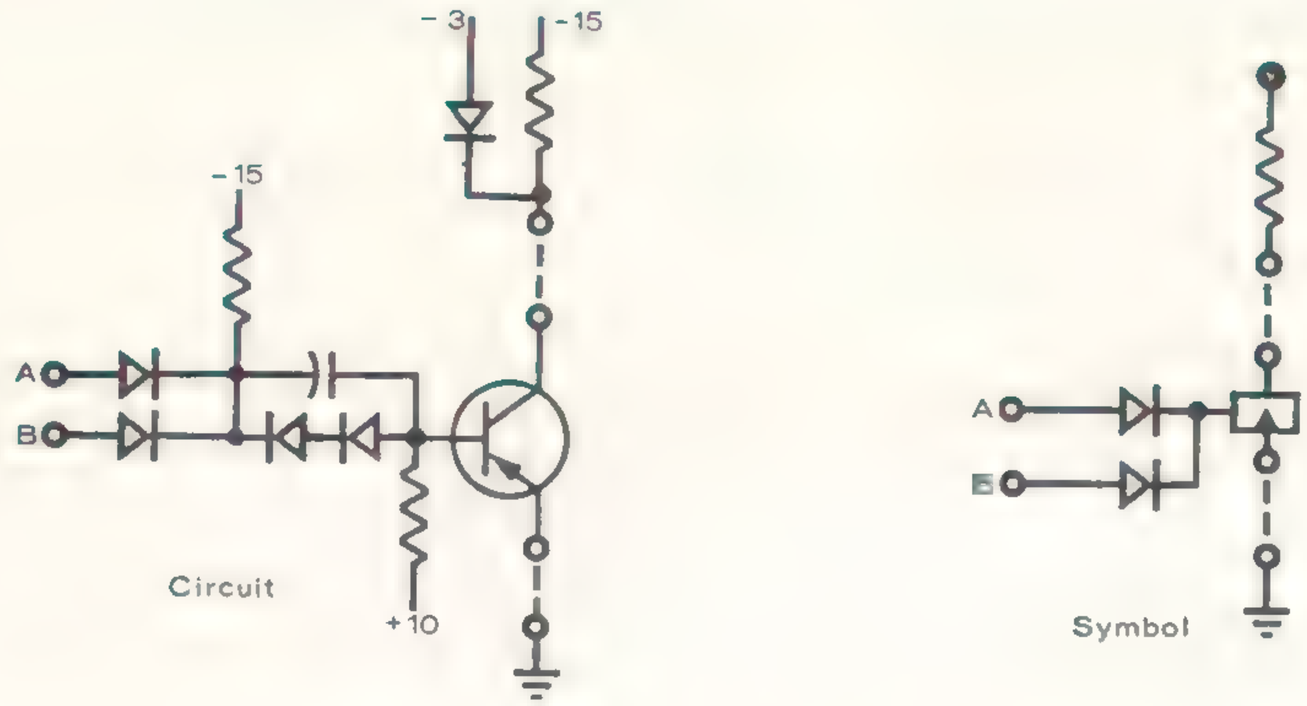


Figure 5

Figure 6 shows a group of two input negative AND circuits which are ORed together. The back to back diode circuitry is possible because of the internal bias in each set of gates.

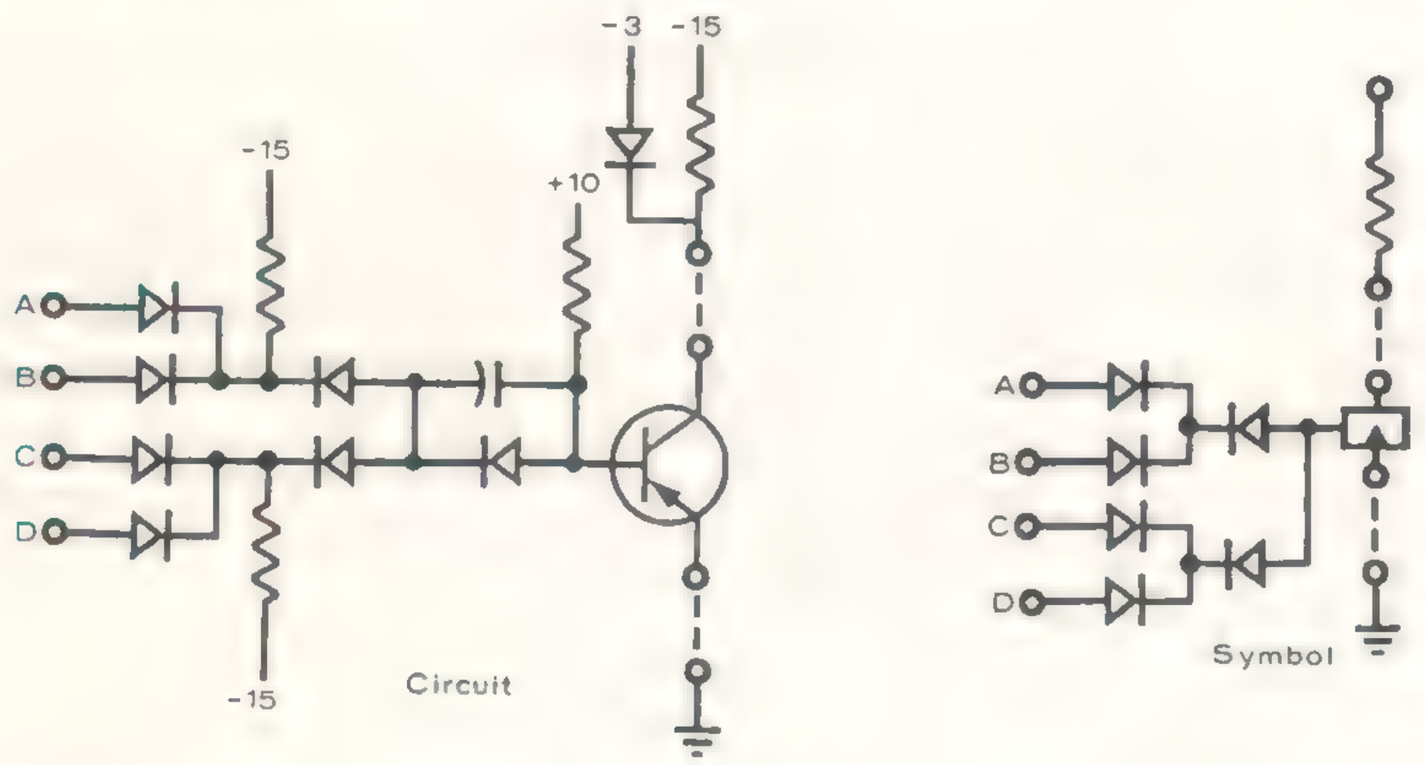


Figure 6

All DEC Diode Gates are permanently connected to a transistor inverter which re-establishes the voltage level after every gate. Thus, DEC Diode Gates may be cascaded indefinitely.

CAPACITOR-DIODE GATES

Schematic drawings of two capacitor-diode gates are shown in Figure 7. If the capacitor and resistor inputs are held at a constant voltage level for a few times constants, the capacitor will be fully charged. If the voltage at the input of the capacitor is then suddenly changed, a pulse will appear at the input of the diode. If the applied level has been of the correct value to enable the gate, the diode will be forward biased when the pulse is applied.

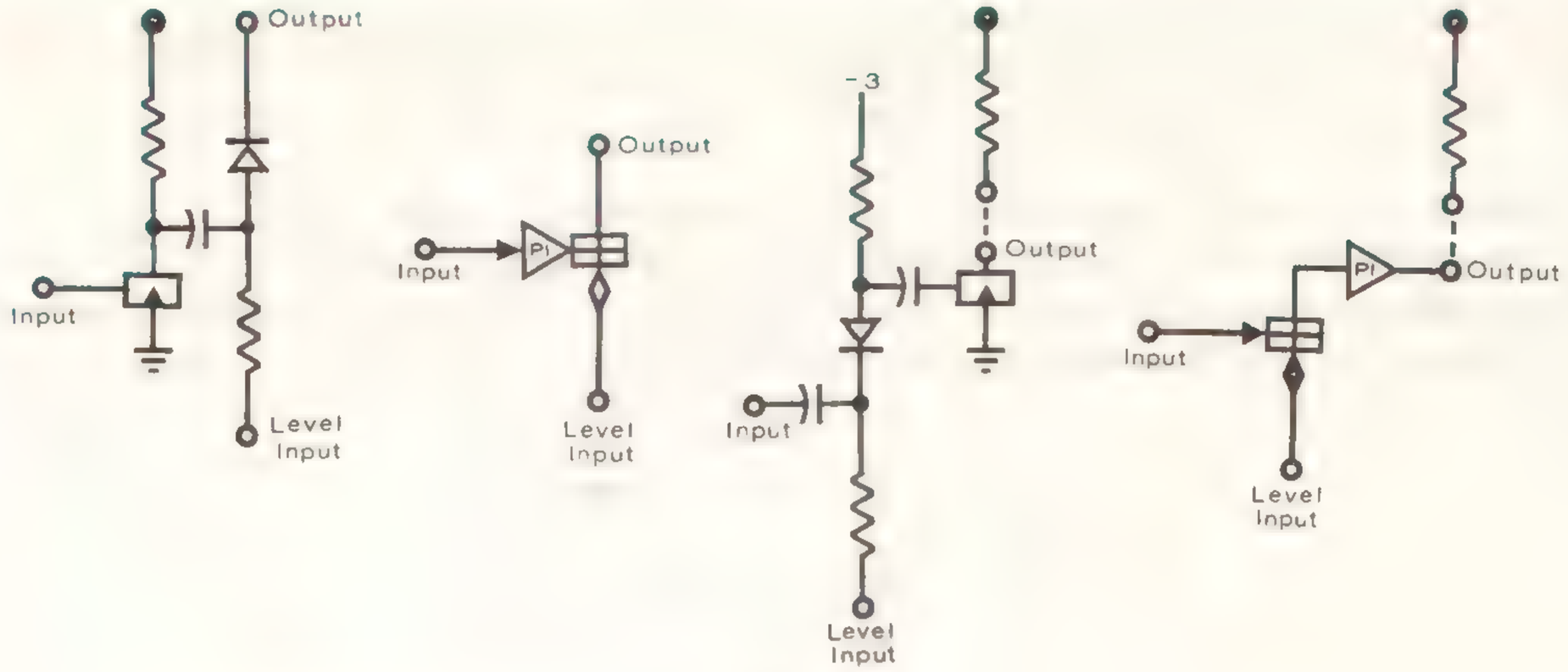


Figure 7

The capacitor-diode gate is principally used in combination with a transistor inverter for additional power. However, the capacitor-diode gate has three advantages which are not available in a simple inverter. These are:

1. The level gate input, the resistor, presents no DC load.

2. The RC time constant of the gate requires that the conditioning level be present a certain amount of time before the pulse occurs. This introduces a delay between the application of a new gate level and the time the gate is conditioned, and allows the sampling of unbuffered flip-flops at the same time the flip-flop is being changed.

3. The capacitor-resistor combination differentiates a level change. This is useful when it is desired to use a level change to trigger a unit which normally operates from a pulse.

DEC manufactures two types of capacitor-diode gates. The Types 4126 and 4128 Positive Capacitor-Diode Gates are preceded by a pulse inverter while the Types 4125, 4127 and 4129 Negative Capacitor-Diode Gates are followed by the pulse inverter.

Those gates where the inverter precedes the capacitor diode are called positive capacitor-diode gates, since the conditioning level is positive for assertion; i.e., the level input must be ground if a pulse is to be passed through the gate. The pulse input to these gates is negative since it will pass through an inverter before reaching the capacitor-diode combination. These gates are used for driving unbuffered Type 4214 Flip-Flops only.

The negative capacitor-diode gates have much greater output driving ability since the pulse inverter is on the output end. The inputs to this gate are a Negative Pulse (or negative going level change) and a negative level for asser-

tion. The pulse inverter will produce a positive-going pulse (relative to −3 volts). The negative capacitor-diode gates will drive any 4000 Series buffered flip-flop, pulse amplifier, or delay unit.

A full duration DEC Standard 0.4 microsecond Pulse can be produced from a level change using a Type 4604 Pulse Amplifier and Standardizer. The Type 4603 may be used if the input is driven by a Negative Capacitor-Diode Gate and a feedback loop is connected as shown in Figure 8.

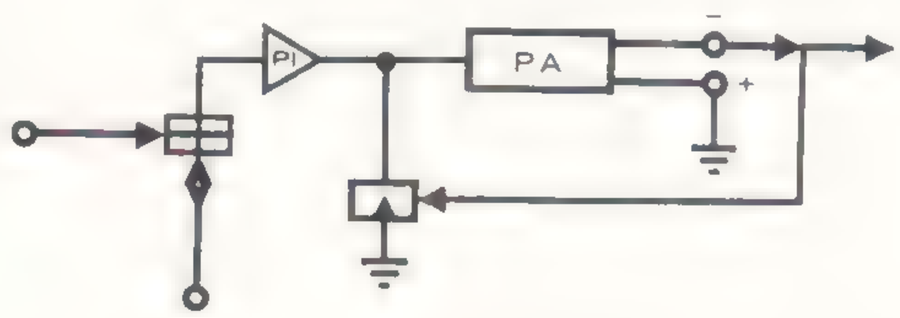


Figure 8

FLIP-FLOPS

If two grounded inverters are interconnected, as in Figure 9, a bi-stable "flip-flop" is obtained. When one side is cut off, its output is negative. This holds the other side on, which, in turn, holds the first side off.

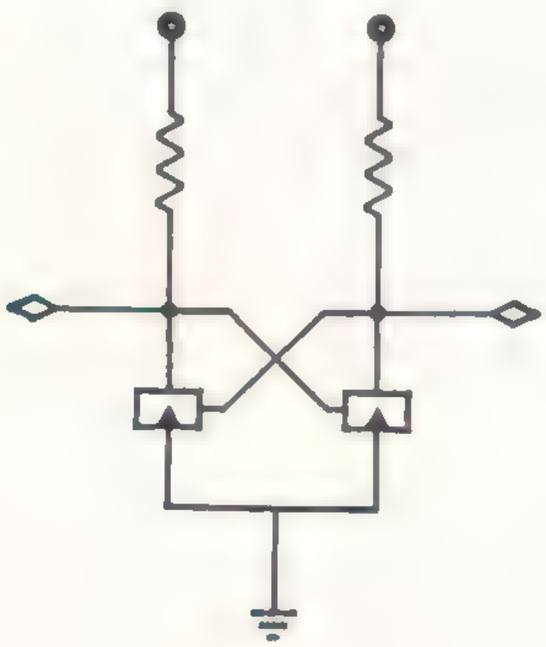


Figure 9

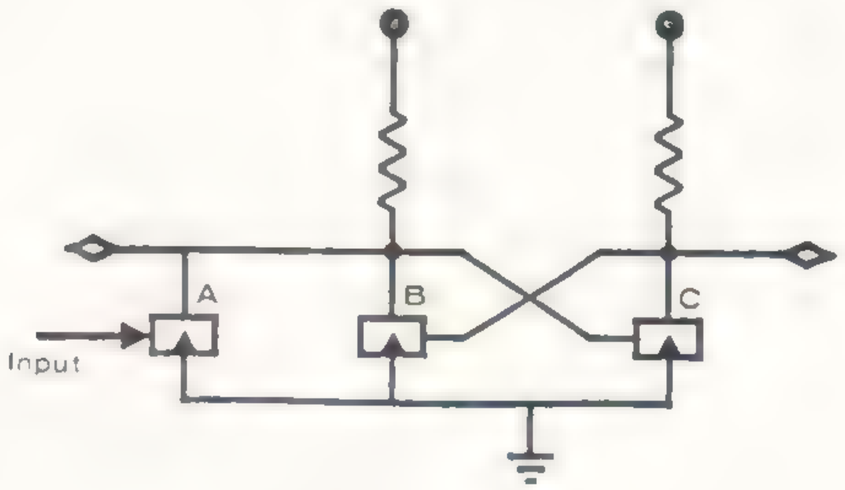


Figure 10

If a grounded inverter A is connected to the off side B of the flip-flop in Figure 10, the state of the flip-flop can be changed by pulsing the base of transistor A with a negative signal. This extra transistor will short the collector of transistor B to ground and will cut off transistor C, which will turn on transistor B. The flip-flop will then stay in that state even after the signal is removed from A.

Simple flip-flops, such as in Figure 10, can be used wherever the load on the output is light and economy is important. DEC System Modules Types 1213 and 4213 contain circuits similar to this one.

For general applications, it is desirable to have flip-flops with very low output impedance so that they can drive many other circuits. For this reason, most DEC Flip-Flops have buffer amplifiers on each side of the flip-flop.

A simple network is placed between the flip-flop in Figure 11 and the output amplifiers, which delays the change in the output. When the flip-flop is changed with a standard pulse, this delay is long enough so that the output does not change until after the pulse is over. This allows flip-flops to be sensed while they are being pulsed, which makes shift registers, counters and adders relatively simple.

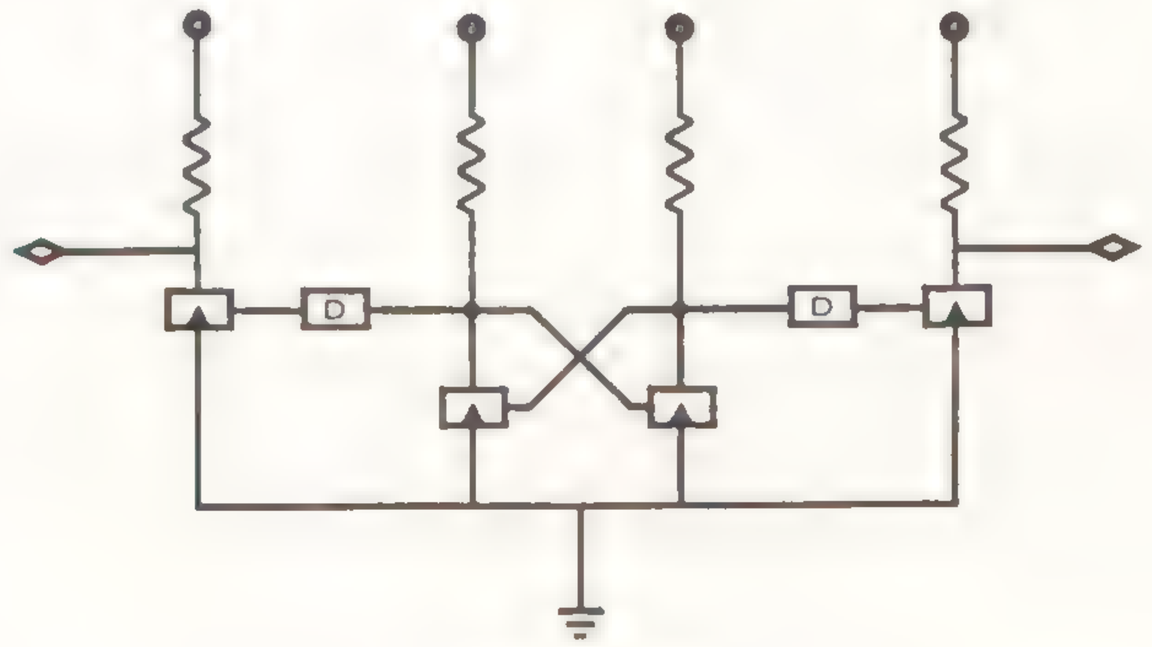


Figure 11

The symbol for a flip-flop is shown in Figure 12. In order to set the flip-flop to the desired state, the inputs at the bottom are "shorted" through inverters* to ground. When the input on the ZERO side has been shorted to ground, the ZERO output is set to the −3 volt level and the ONE output is at ground. This is defined as the ZERO state. Similarly, when the flip-flop is in the ONE state, the ONE output is at −3 volts and the ZERO output is at ground.

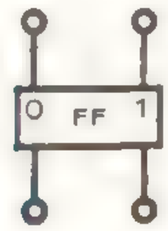


Figure 12

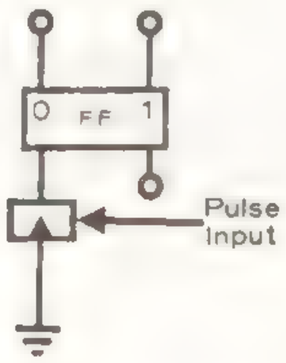


Figure 13

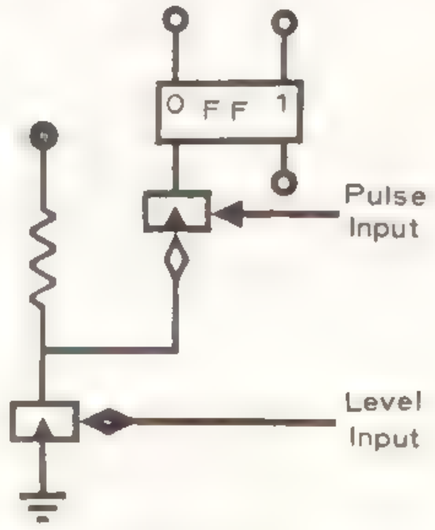


Figure 14

*With DEC Unbuffered Flip-Flops, the individual inverters may be replaced by capacitor-diode resistor configurations with a single inverter driving many such circuits. All quadruple flip-flop packages have such gates built in (except the Type 4214 which is used with Type 4126 of 4128 gates). Because of the nature of the RC coupling, this method is limited to low frequency applications.

Flip-flops are always changed by momentarily shorting an input to ground, as shown in Figure 13. The input to the inverter is a DEC Standard Negative Pulse of 2.5 volts amplitude relative to ground.

To gate information into a flip-flop, two inverters can be connected in series, as in Figure 14. If the level input is at ground when the upper inverter is pulsed, the flip-flop terminal will not be shorted to ground; but if the level input is at −3 when the negative pulse arrives, the input is shorted and the flip-flop is cleared.

Since most DEC Flip-Flops have buffer amplifiers, it is permissible to use the buffer as the level gate. This added flexibility is useful since it allows reading into a flip-flop with only one inverter gate.

Figure 15 is a "jam transfer" gate employing DEC Buffered Flip-Flops. The contents of flip-flop A can be "jammed" into flip-flop B with a single pulse independent of the previous state of flip-flop B. The outputs of A are connected directly to the emitters of the pulse gates feeding the inputs of B. Both inverter pulse gates are pulsed simultaneously but only the gate which has ground on its emitter will pass the pulse to set the flip-flop. For example, if flip-flop A holds a ONE, its ZERO output terminal will be at ground, allowing the right-hand gate to pass the pulse and set flip-flop B.

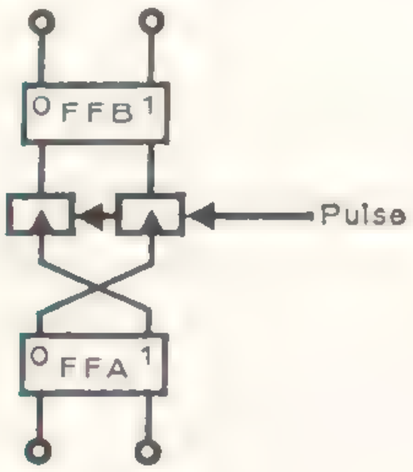


Figure 15

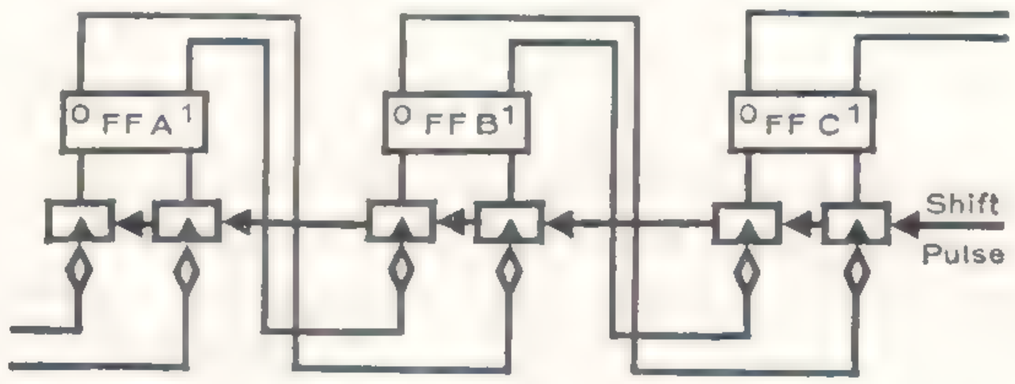


Figure 16

The shift register of Figure 16 is another use of the jam transfer gate of Figure 15. Since the outputs of the flip-flops do not change until the shift pulse has passed, no logical delays are needed between flip-flops.

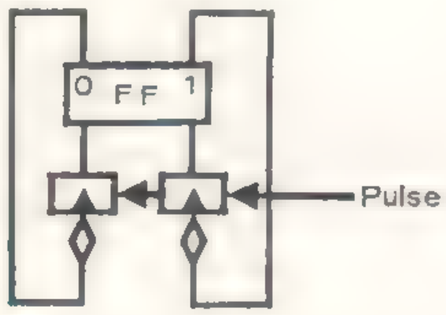


Figure 17

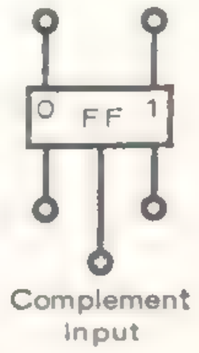


Figure 18

When the inverters of Figure 17 are pulsed, the state of the flip-flop will be changed or "complemented." On some of the DEC Flip-Flops this gating is done internally, and a complement terminal is brought out, as in Figure 18.

There is also a complement output terminal P which will deliver a DEC Standard Negative Pulse every time the flip-flop complement input is pulsed. This P pulse output is useful in counters and adders.

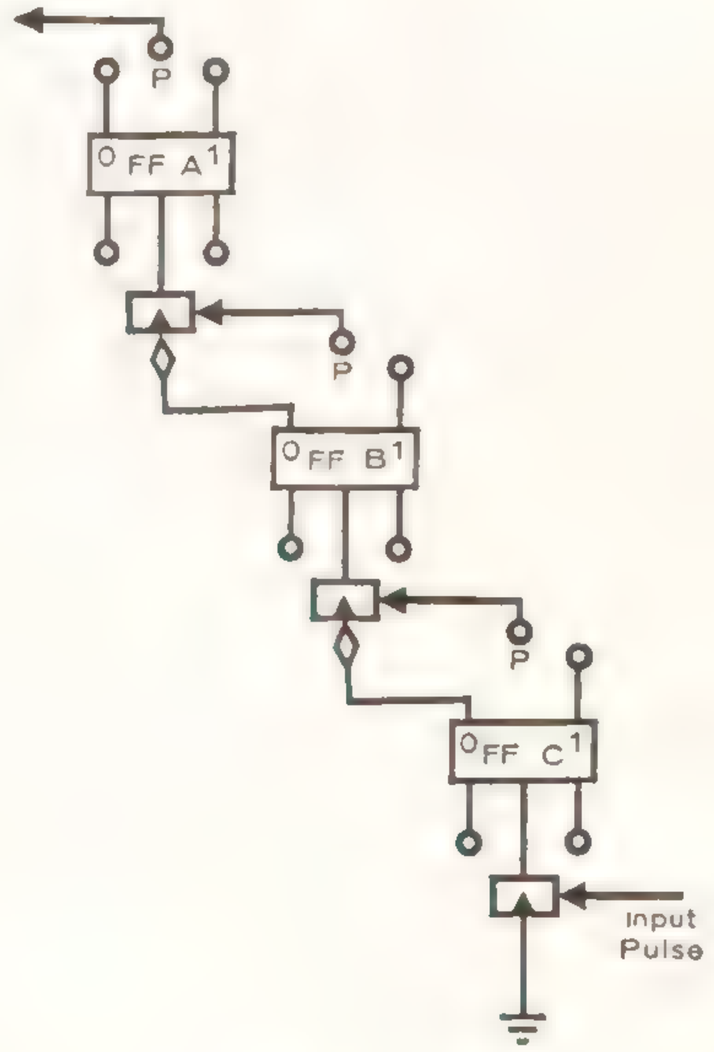


Figure 19

A typical counter arangement using DEC Complementing Flip-Flops is shown in Figure 19. The pulses being counted enter on the right. They always complement flip-flop C and generate a standard pulse at P. This P Pulse complements flip-flop B when flip-flop C holds a ONE. When this P Pulse gets through the gate and actually complements B, it will generate a P Pulse out of B. The process is continued down the length of the counter. Only one inverter and one flip-flop are needed for each bit in the counter.

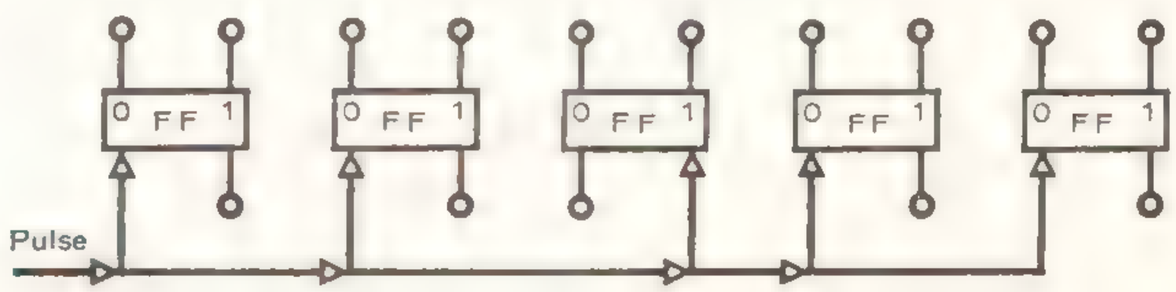


Figure 20

System Module flip-flops also have direct clear and set terminals which allow flip-flop registers to be set or cleared without the use of pulse gates on each flip-flop. The input to these terminals is a DEC Standard Positive Pulse of 2.5 volts amplitude relative to ground. These pulses can be produced by DEC Delays, Pulse Amplifiers, Clocks, and Pulse Generators. Figure 20 shows a register being set to 00100 using the direct inputs.

DELAYS

DEC Delay Units are flip-flops which have only one stable state. When the input terminal is "shorted" to ground by a standard pulse, the level output terminal will switch from its normal ground level to the −3 volt level for a fixed period of time, which is adjustable. A standard pulse will be produced at the pulse output when the level output returns to its normal 0 volt condition. The pulse output comes from a pulse transformer which has both terminals available so that either positive or negative pulses may be obtained, depending on which terminal is grounded. Typical waveforms for a delay unit are shown in Figure 21.

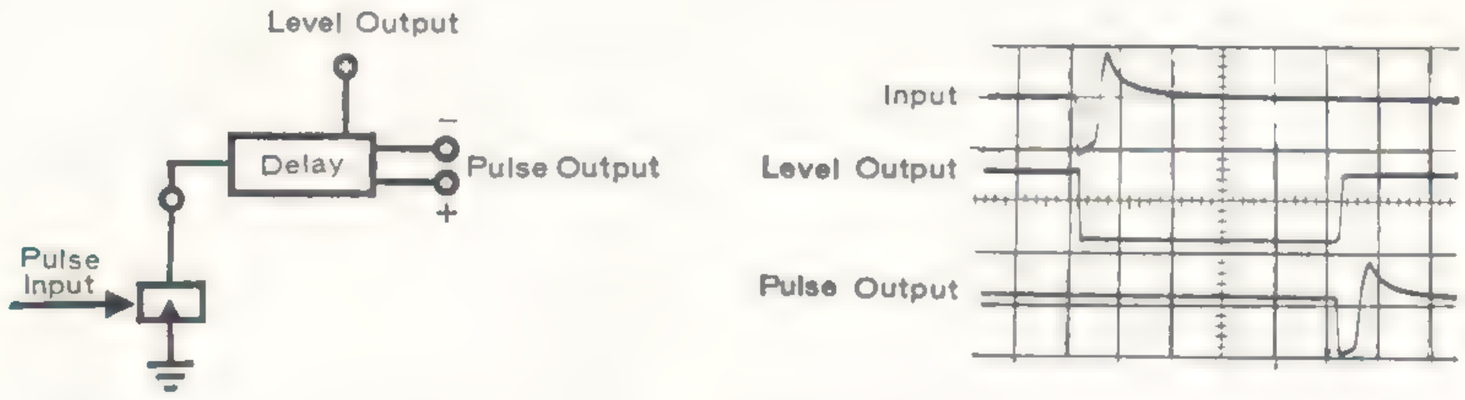


Figure 21

PULSE AMPLIFIERS

DEC Pulse Amplifiers are a powerful logical element because they not only amplify and standardize the shape of pulses, but also gate pulses. When the same logical gating is to be done on a whole register of flip-flops, it often can be done once before the pulse amplifier drives the register.

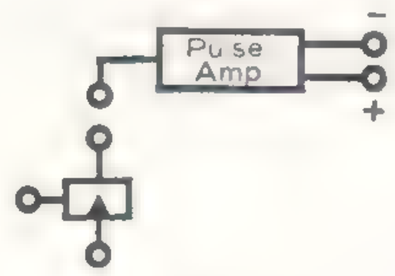


Figure 22

The outputs of the pulse amplifiers come from pulse transformers, which have both terminals available so that either positive or negative pulses may be obtained, depending on which terminal is grounded. Positive pulses are used to direct set and clear flip-flops without inverters. Negative Pulses are used for setting, clearing and complementing with inverters.

CLOCKS

DEC Clocks produce standard pulses from stable, variable frequency, RC-coupled oscillators which have a wide range of frequencies available. These clocks are often used as a primary source of timing for large systems. Where very precise timing is needed, crystal clocks which contain a single-frequency crystal oscillator are available.

Figure 23

PULSE GENERATORS

DEC Pulse Generators are used to initiate action as a result of outside activity. Every time the input of these pulse generators goes more negative than $-2\frac{1}{2}$ volts after having been more positive than -1 volt, a standard pulse is generated. Most outside actions can be converted into voltage levels that will fill this criterion.

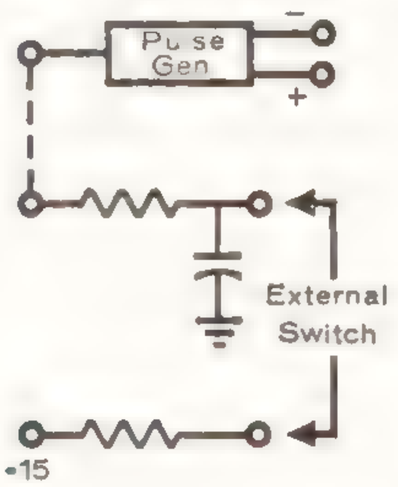


Figure 24

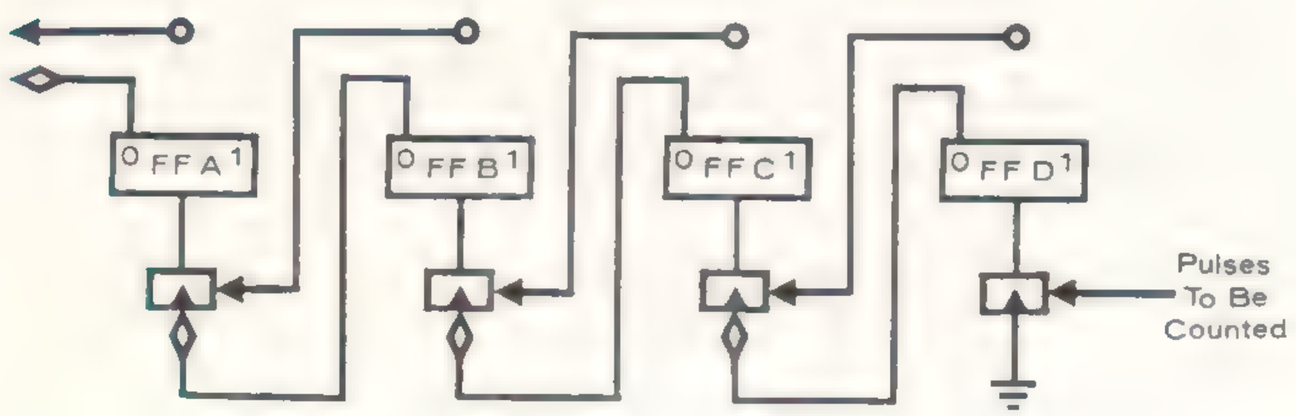
It is difficult to generate a single pulse from a switch or relay closure because contacts bounce many times before they finally make a solid contact. If these are connected directly to a pulse generator, they will produce a pulse for each contact bounce. An integrating circuit is included which can be connected between the pulse generator and the contact. This circuit converts the many fast voltage changes into a single slow change, which generates a single pulse.

BUFFERED FLIP-FLOPS
TYPICAL APPLICATIONS

COUNTERS

Building a counter with DEC flip-flops is straightforward due to the built-in delay and the availability of the P pulse terminal. A carry pulse is created when the P pulse is fed to the base of a gate which is conditioned by the ONE state of the flip-flop.

STRAIGHT BINARY COUNTING



COUNTING SEQUENCE	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Figure 25
Straight binary counter
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)

When flip-flop D in Figure 25 is in the ONE state, its ZERO output terminal is ground. When it receives a complement pulse, the gate will pass a P pulse into the complement input terminal of flip-flop C. If flip-flop D has been in a ZERO state, the P pulse would have been prevented from complementing flip-flop C. The series connection of P pulse and gates is the high-speed carry chain. The carry propagate time per digit is much less than the flip-flop's total transition time.

To assure that flip-flop D will not be in the process of changing state while flip-flop C is receiving its carry pulse, a delay has been built into each flip-flop package. This insures that the ONE and ZERO output terminals will not change until after the carry pulse has been gated.

Each bit of the counter requires one flip-flop and one transistor gate. There are two gates contained in each DEC Flip-Flop Type 201, 1201, 3201, and 4201. If DEC Laboratory Modules are used, the results can be read by means of the indicator lights on the front panel. DEC System Modules Types 1201 and 4201 are compatible with Indicator Drivers Types 1675 and 1669, which are suitable for driving remote indicator lights.

SPECIAL COUNTS

Often it is desirable to build a counter that will produce a signal after a particular number (N) of events have occurred. If N is an integer power of 2, the output is automatically produced by the final digit of a counter of appropriate length. If N is not a power of 2, gating must be performed to detect the desired number, generate a signal, and reset the counter to 0.

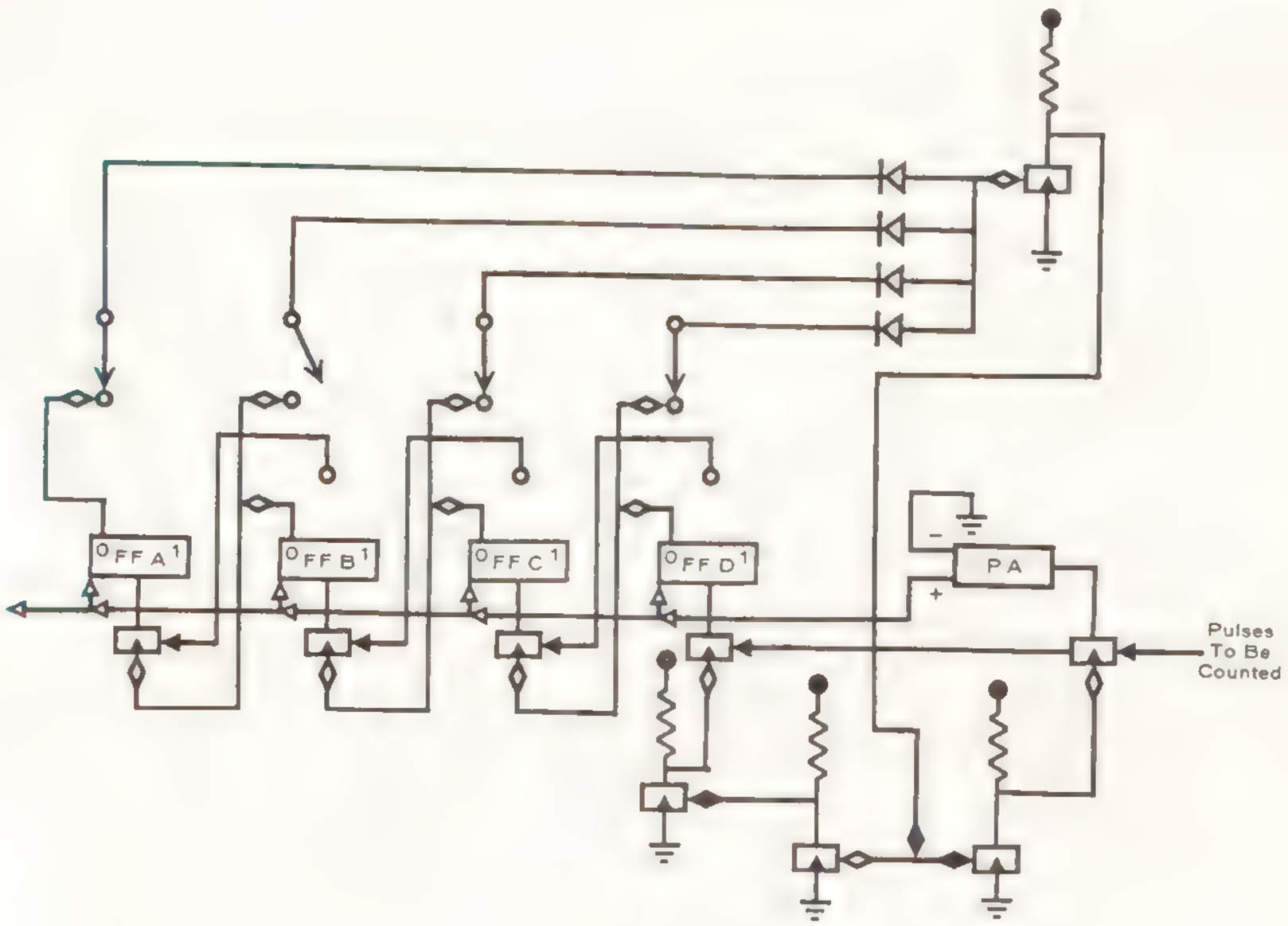
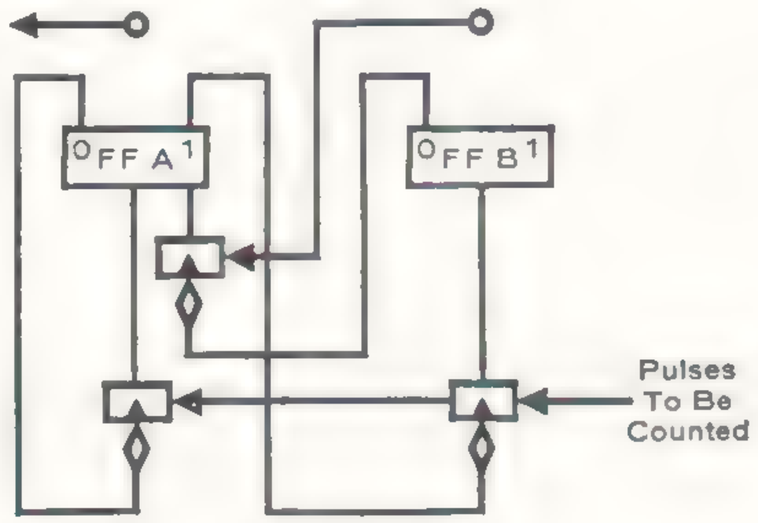


Figure 26
Arbitrary count — count of 12 illustrated
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)

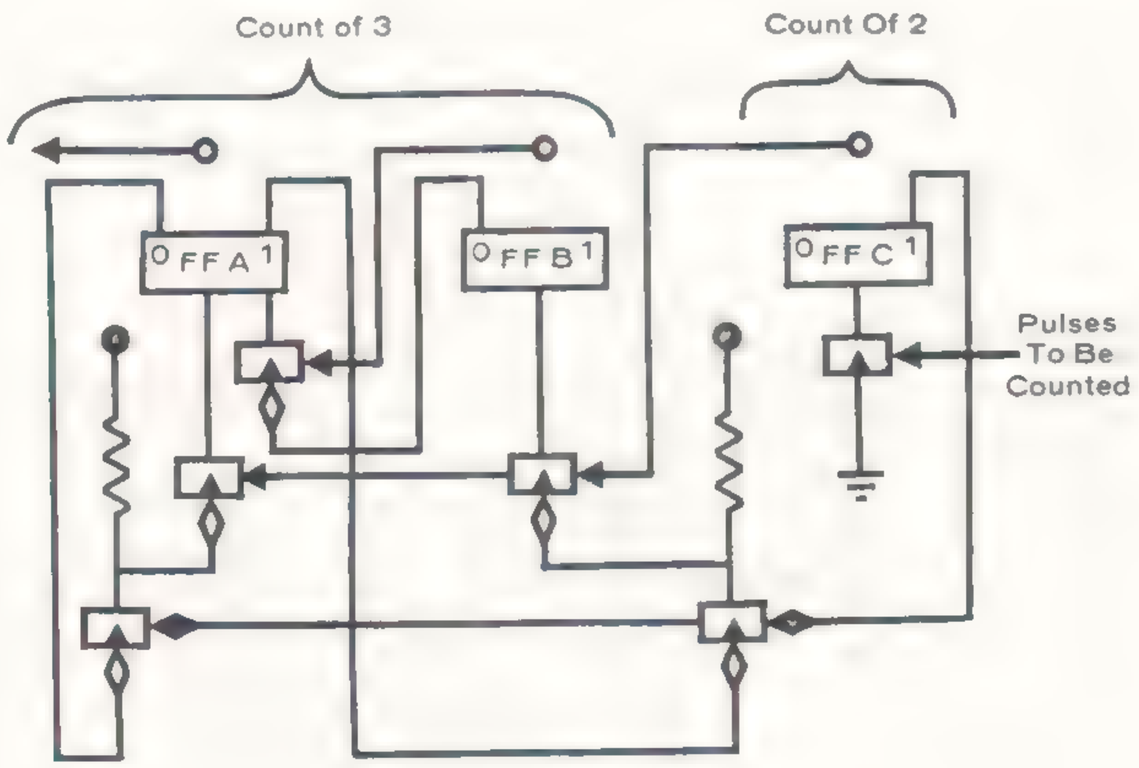
Transistor inverter gates or diode gates may be used to sense the number N–1, close the input to the counter, and re-route the Nth input pulse so that it will clear the counter and generate an output signal. Although this is not always the optimum method, it is a completely general method which will work for any value of N.



COUNTING SEQUENCE	
0	00
1	01
2	10

Figure 27
Count of 3
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)

A typical counting sequence is shown for N = 3 in Figure 27. The progress of the count is shown in the table. When the count of 2 is reached, the next pulse will clear the counter and generate an output signal.



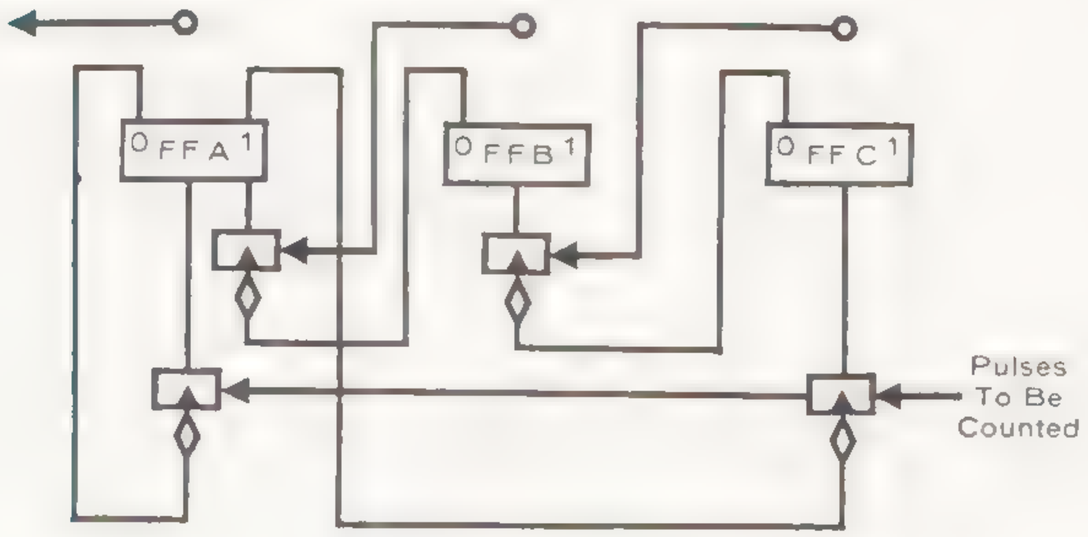
COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100
5	101

Figure 28
Count of 6
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)

A counter for 6 is made from the counter for 3 by preceding it with a binary counter (Figure 28). Examination of the counting sequence shows that the least

significant digit alternates between ZERO and ONE, while the two most significant digits follow the same pattern as the count of 3. The circuit for flip-flops A and B is identical to that for the count of 3 except that two additional gates are necessary. These are required because the input to the count-of-3 portion includes a conditioning level, as well as a pulse.

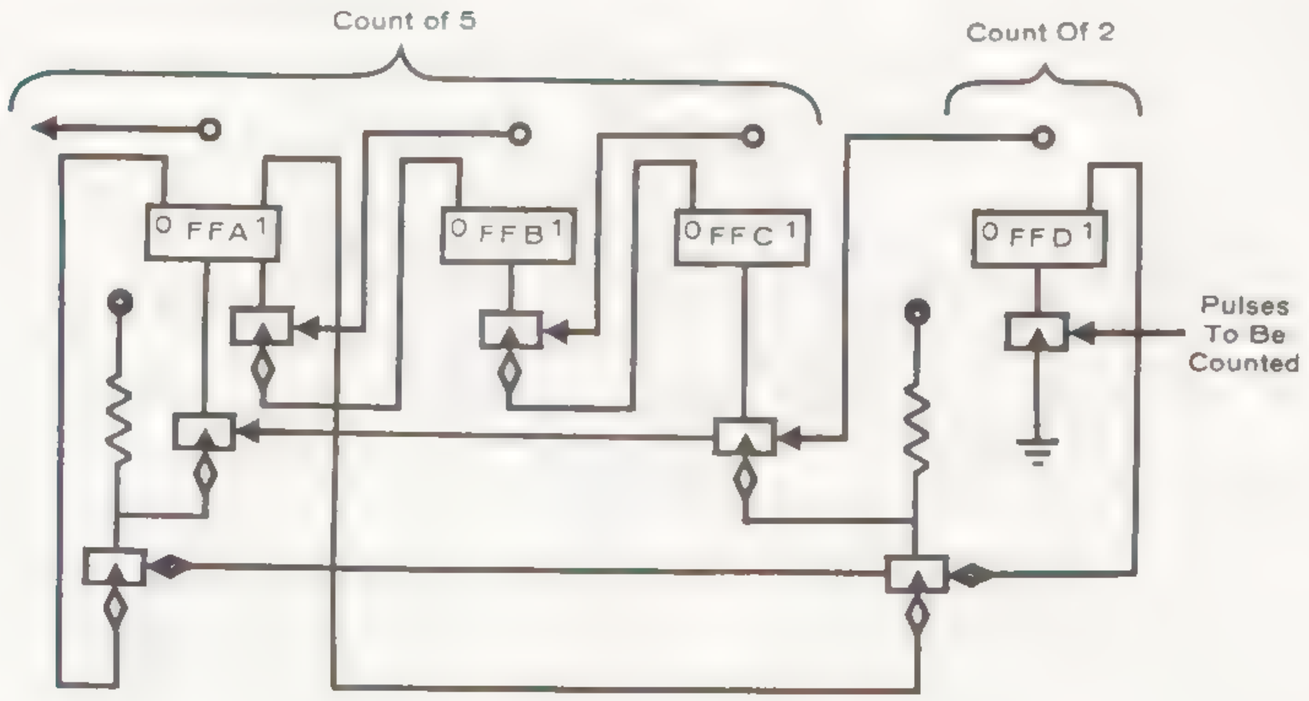
BINARY CODED DECIMAL COUNTING



COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100

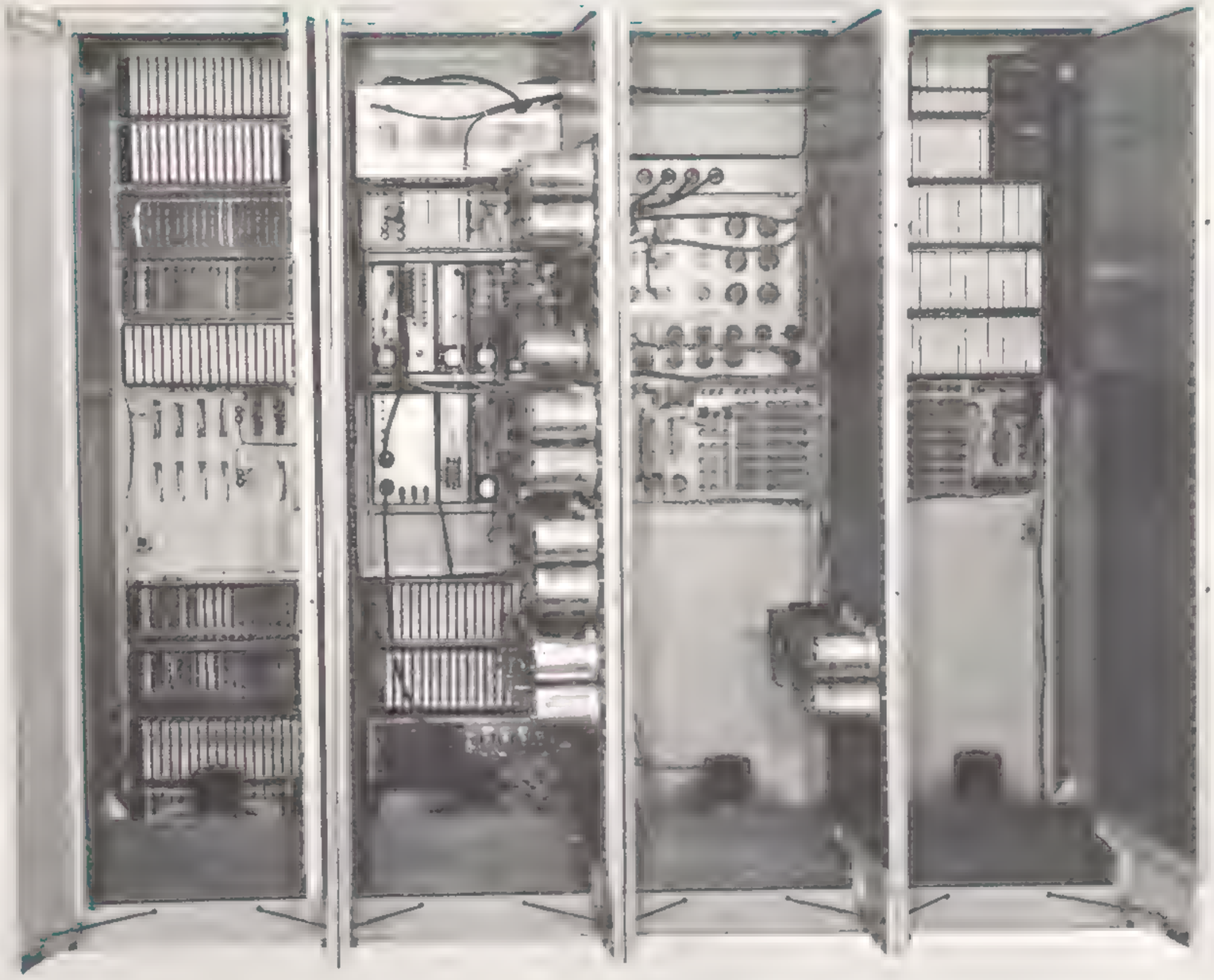
Figure 29
Count of 5
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)

From the simple count-of-5 circuit, binary coded decimal counters may be generated.

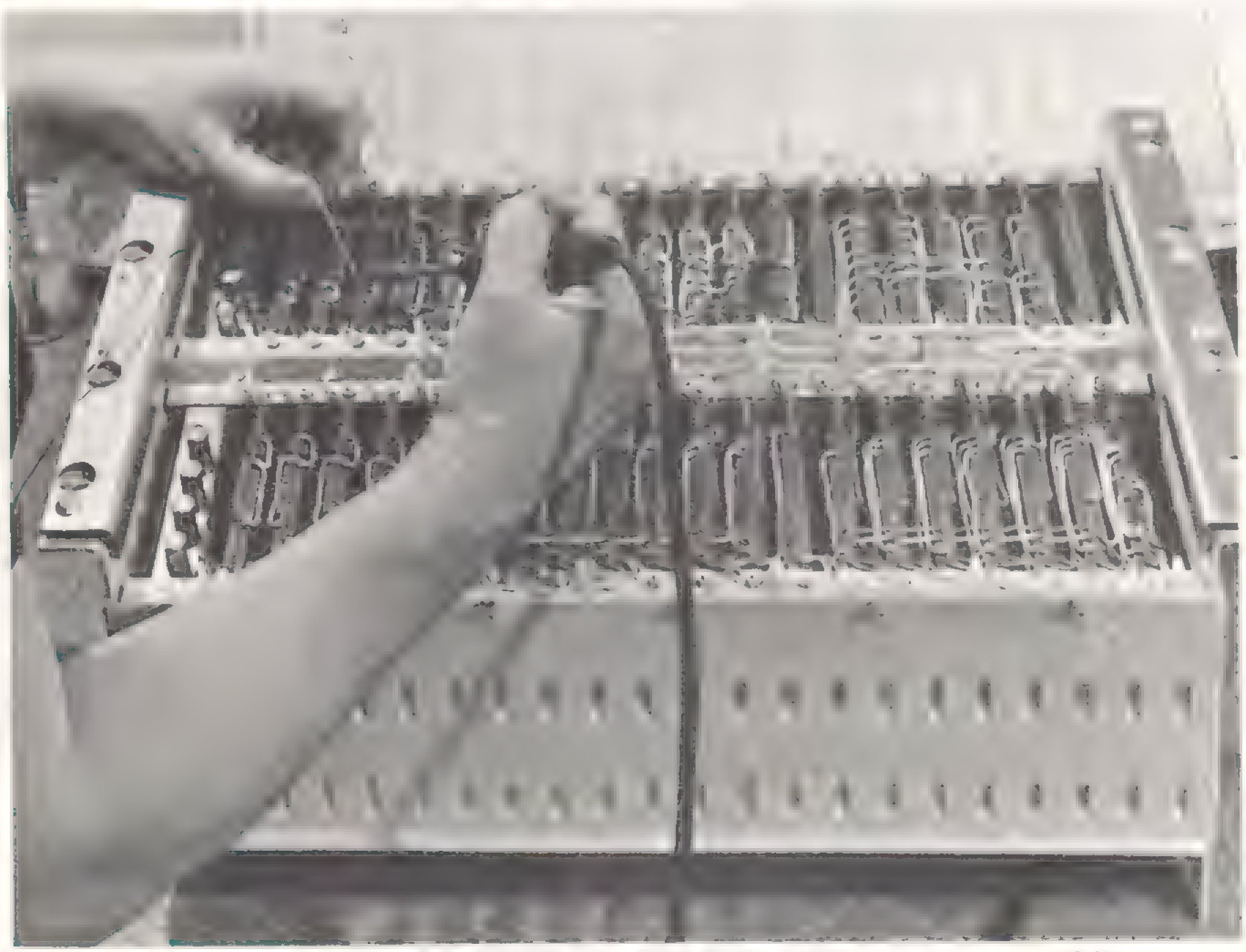


COUNTING SEQUENCE	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Figure 30
Count of 10 — binary-coded decimal
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)



Construction of digital systems, such as this DEC Memory Tester, is greatly simplified by the use of System Modules.



Mounting panels may be pre-wired to form system sub-assemblies.

To give a count of 10, the counter for 5 is preceded by a binary counter (Figure 30). This circuit is compatible with DEC's BCD Decoder and Light Driver Type 1671, which has 10 output lines for driving a decimal output display.

A counter for 100 can be made by cascading two BCD stages. Because the complement input to A is used only at the time the decade is cleared, the P pulse can feed the next stage without being gated. Any number of BCD stages may be cascaded in a similar manner.

Up counters and down counters are among the logical operations which can be performed with the DEC Basic Logic Kit

DOWN COUNTERS

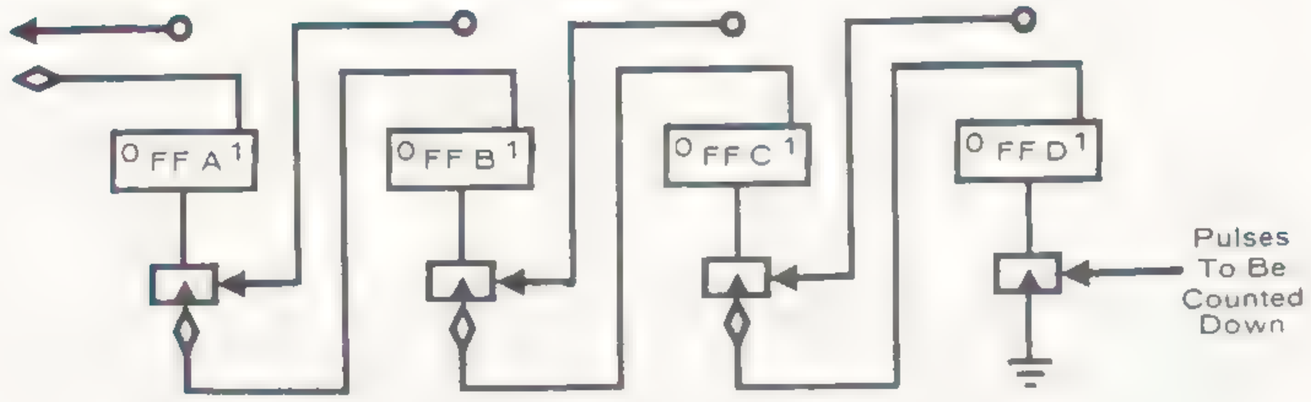


Figure 31
Down counter
(DEC Flip-Flops Type 201, 1201, 3201, or 4201)

In a down counter, each successive pulse will decrease the count by 1. The method for building a down counter is essentially the same as that used in the up counter, except that each flip-flop input is conditioned by the ZERO state of the previous flip-flop. In this way, the P pulse chain will form a high-speed borrow circuit instead of a carry circuit.

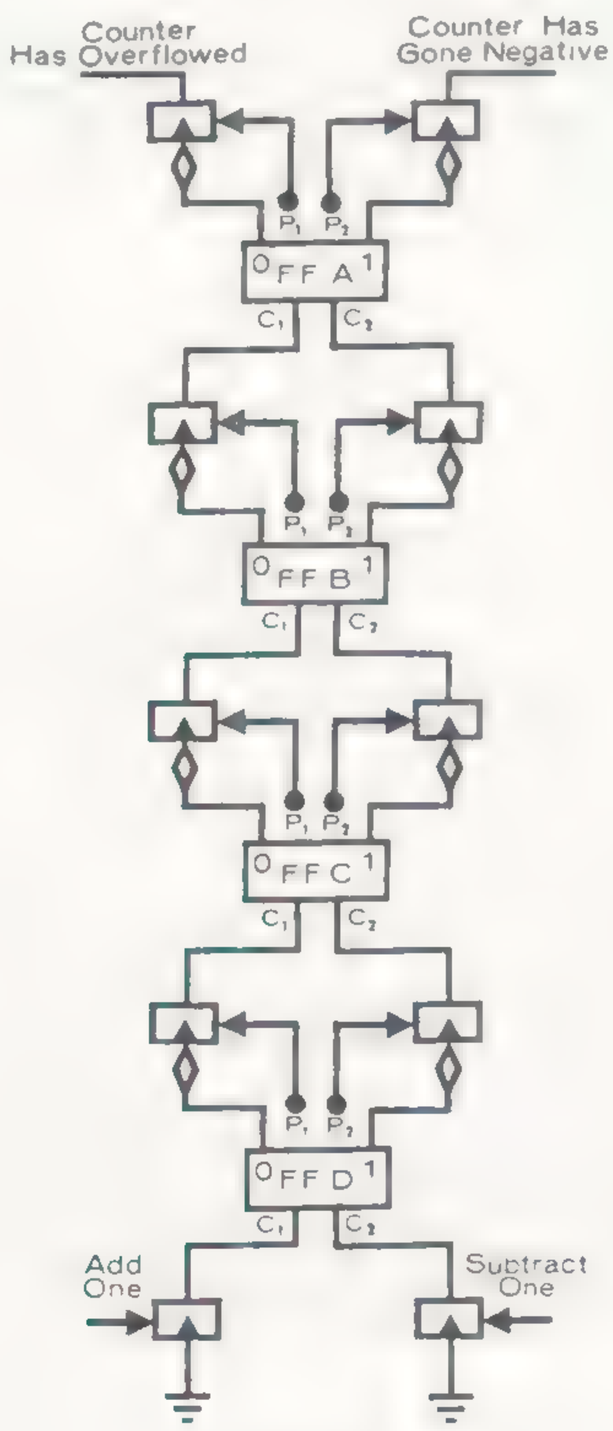


Figure 32
Binary up-down counter
(DEC Flip-Flops Type 1201 or 4201

An up-down counter combines the techniques found in the individual up and down counters. This is made possible by use of DEC Flip-Flops Type 1201 or 4201. Each of these units contains a flip-flop with two independent sets of complement and associated P pulse terminals. Thus, it is possible to connect one set to form a high-speed carry circuit, while the other set forms a high-speed borrow circuit. Of course, the add and subtract pulses should not be allowed to arrive simultaneously.

10 MEGACYCLE COUNTING

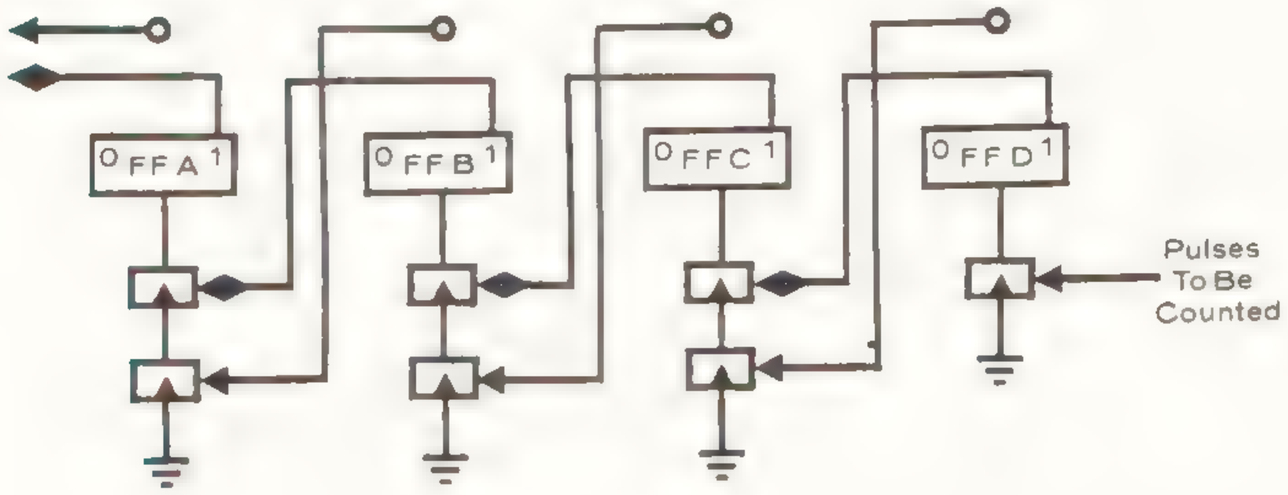


Figure 33
10 mc binary counter
(DEC Flip-Flops Type 5201 or 6201)

The logic behind a 10 megacycle counter is the same as that for a 5 megacycle or 500 kilocycle counter; however, the loading rules differ. Two inverters are required for each bit. The pulse must go to the lower inverter, as shown, to insure sufficient pulse gain to propagate the carries.

Only one 10 megacycle flip-flop is needed for counting at 10 megacycles where carry propagate time is not important. Such a mixed system is shown in Figure 34. In the transition from one type of equipment to another, a pulse amplifier with feedback is required to lengthen the pulse.

PARALLEL ADDERS

Addition of the contents of the incident number register to the contents of the accumulator is accomplished in two discrete steps, a half-add and a carry. This is made possible by using DEC Flip-Flops Types 1201 or 4201 as in Figure 35. These units have two discrete complement inputs, each with its own P pulse terminal.

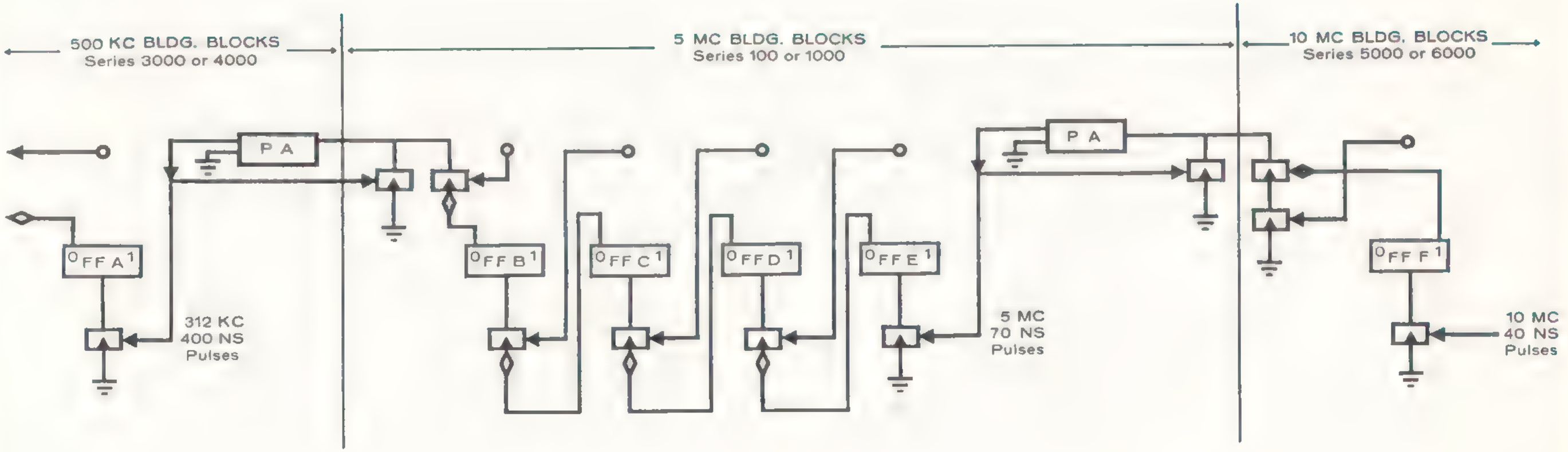


Figure 34
10 mc counter, mixed system — showing pulse stretching
(Lower cost than Figure 37 counter, but longer propagate time)

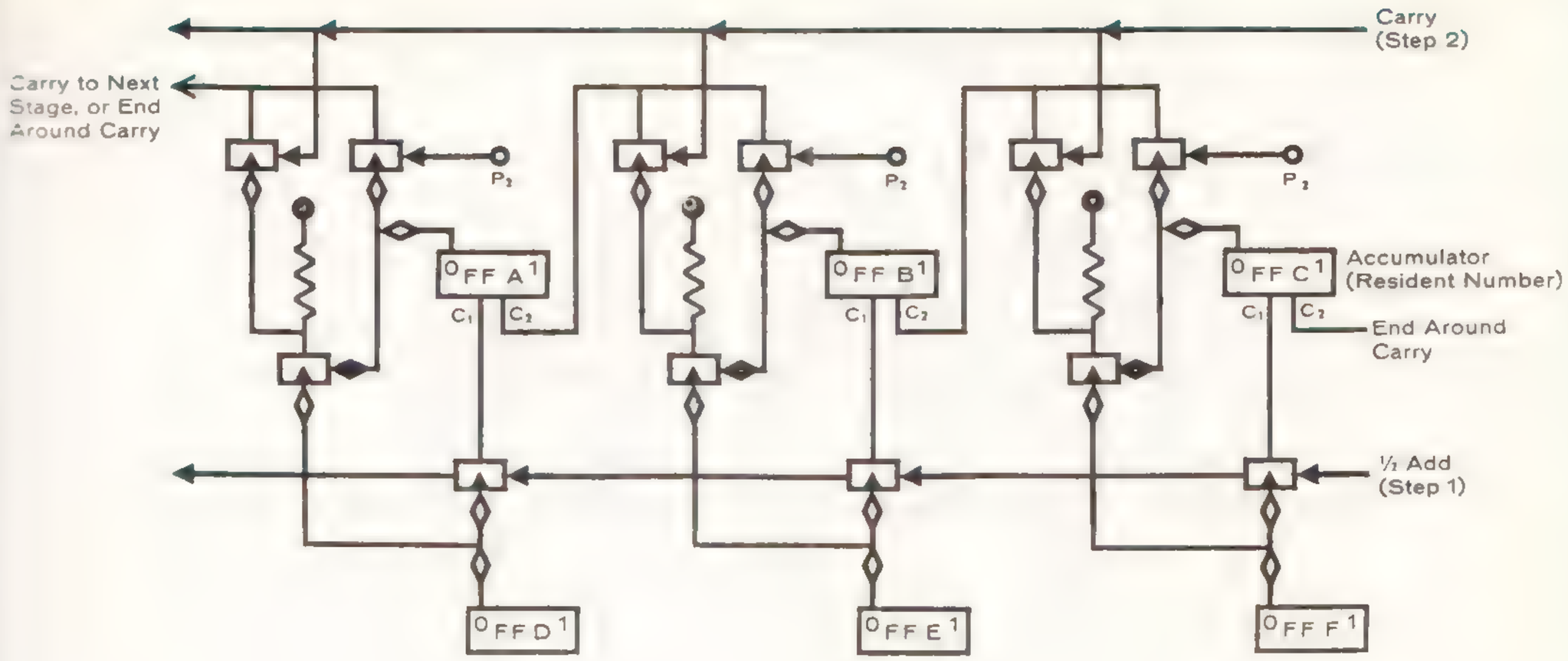


Figure 35
Parallel adder
(Accumulator Flip-Flops DEC Type 1201 or 4201)

The first step is half-add. Each digit of the accumulator is complemented if the corresponding digit of the incident number is a ONE.

The second step is carry. A carry will be generated if a digit in the accumulator is ZERO and the corresponding incident number digit is ONE. A carry will be propagated if an accumulator digit is ONE and it also receives a carry pulse from the next less significant accumulator digit. After the carries have propagated, the contents of the incident number register may be modified to add another number to the accumulator.

Table I provides some examples.

INCIDENT NUMBER	ORIGINAL ACCUMULATOR NUMBER	ACCUMULATOR AFTER HALF-ADD	ACCUMULATOR AFTER CARRY
001	010	011	011
001	001	000	010
001	011	010	100

Table I

10 mc counter, mixed system — showing pulse stretching
(Lower cost than Figure 37 counter, but longer propagate time)
Figure 34

Variations of this technique can be used to make a subtracter, a multiplier, a divider, etc. A faster adder can be built by using 10 megacycle Flip-Flops Type 6202, as shown in Figure 36.

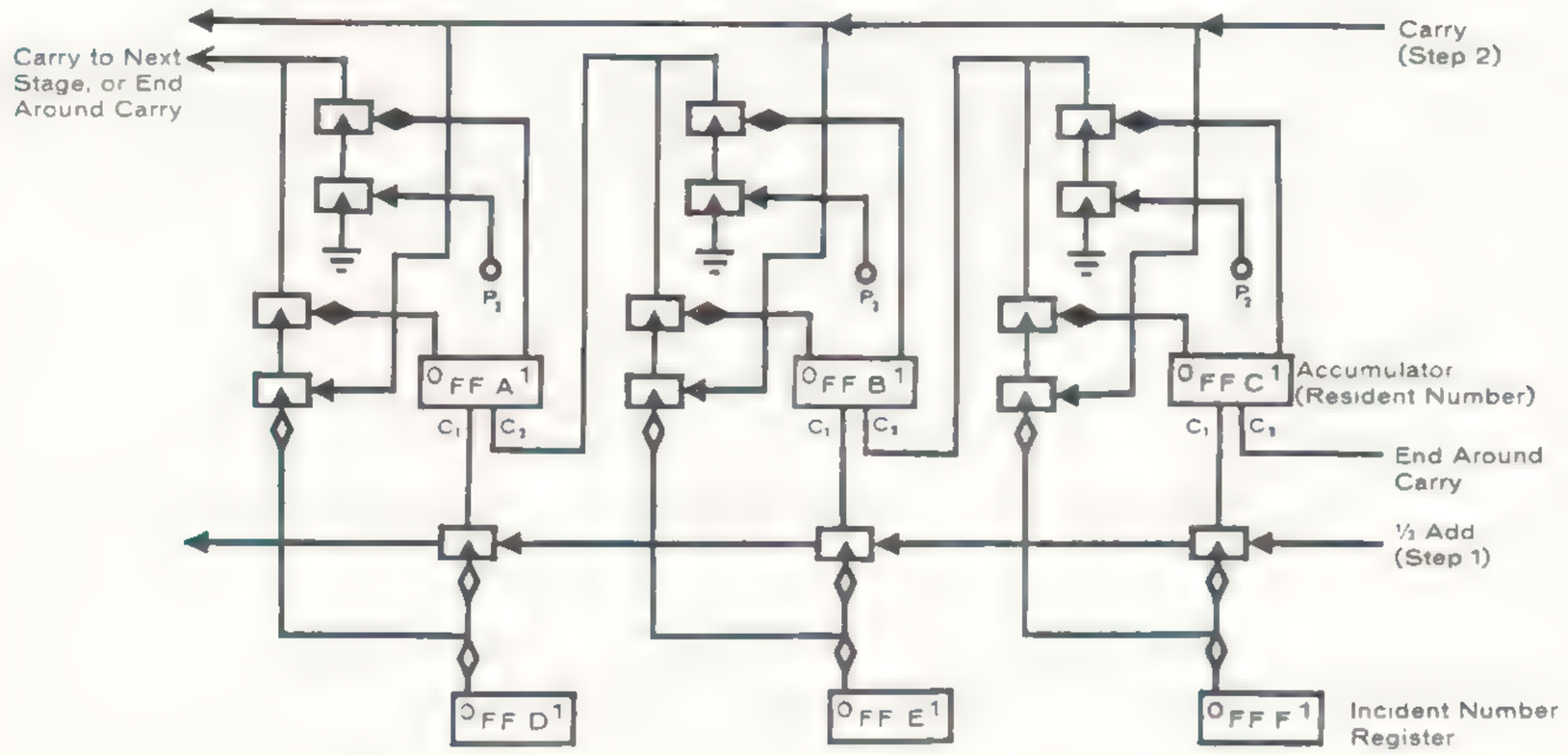


Figure 36
Parallel adder using 10 mc flip-flops
(Accumulator Flip-Flops DEC Type 6202)

SUBTRACTERS

An adder may be used for subtraction as well as addition. To subtract a number from the accumulator, the number is made negative and added to the accumulator. The steps involved in performing a subtraction depend on whether the "one's complement" or the "two's complement" number system is used to represent a negative number.

The "one's complement" number system is easiest to implement. To subtract a number from the accumulator, the steps are: (1) complement the incident number, (2) half-add, and (3) carry. With this number system it is necessary to implement an "end-around carry" from the most to the least significant digit. This connection is shown in Figures 35 and 36.

Subtraction is performed in DEC's PDP computers by (1) complementing the accumulator, (2) half-add, (3) carry, and (4) recomplementing the accumulator.

COMPARATORS

COMPARING A TOGGLE SWITCH REGISTER AND A FLIP-FLOP REGISTER

The simplest comparator is the type used in building a counter which will stop or reset itself after a preset number of counts. This type of comparator, as illustrated in Figure 26, consists merely of a string of diode gates with each diode connected through a toggle switch to a flip-flop. Each toggle switch corresponds to a single binary bit, with a closed switch representing a ONE and an open switch representing a ZERO. Since opening a toggle switch has the same effect as removing the corresponding diode, there may be several numbers which would generate a comparator output. However, the first comparator output will correspond to the desired number if the counter always begins in the all ZERO state. This, of course, requires that the counter be reset, or the counter input be terminated as soon as the comparator output appears.

The comparator output, in Figure 26, is used to close the counter input and re-route the next count pulse to perform the clearing action. Since this action requires an additional input pulse, the toggle switches must be set to detect one less than the desired number.

This technique can also be used with a down counter. The diode gates are then connected to the flip-flops so that a closed switch corresponds to a ZERO. The first comparator output is used to preset the counter to the all ONE state or to turn off the counter input.

Comparing a toggle switch register with an arbitrary flip-flop register requires a single-pole double-throw switch for each bit. Thus both ZEROS and ONES are detected.

COMPARING TWO FLIP-FLOP REGISTERS*

Comparison of two flip-flop registers requires an "EXCLUSIVE OR" for each corresponding pair of bits, since there are two possible conditions which will produce an inequality; i.e., bit A1 = 0 and B1 = 1 or A1 = 1 and B1 = 0. The entire set of EXCLUSIVE OR's must then be OR'd together to determine when any pair of bits is unequal.

Figure 37 shows an example of a two-register comparator. The EXCLUSIVE OR's consist of two inverters. The final ORing function is accomplished by simply tying the inverter outputs together. Whenever the two bits of any pair are different, the comparator output will be at ground. When there are no differences, the output will be negative.

Of course, there is a limit to the number of inverters which can be connected in this manner. If a single standard clamped load resistor is used to define the −3 logic level, then the maximum number of "on" bases is six (as explained in

*See also page 51

the section entitled "Loading Definitions" and the technical literature describing the inverters). Since only one base in each EXCLUSIVE OR pair can be "on" at a time, the maximum configuration is actually seven pairs of inverters.

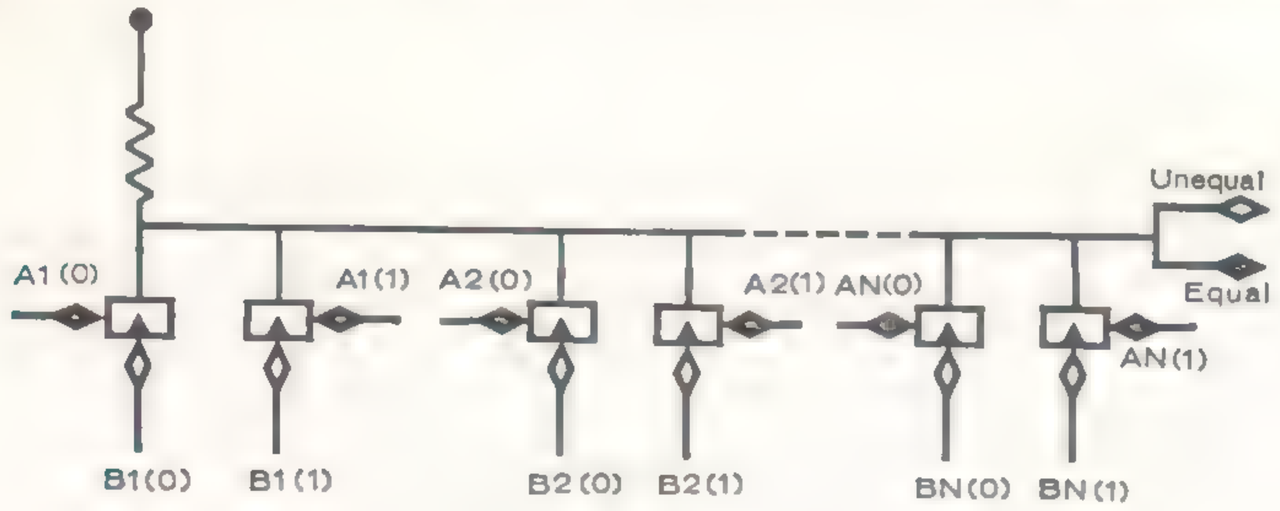


Figure 37
Comparator
(10 mc, 5 mc or 500 kc inverters)

To increase the allowable number of inverters, the clamped load resistor may be replaced by a 10,000 ohm resistor externally wired to the −15 volt terminal. The maximum configuration is then 14 pairs of inverters; however, the output can drive only one inverter base.

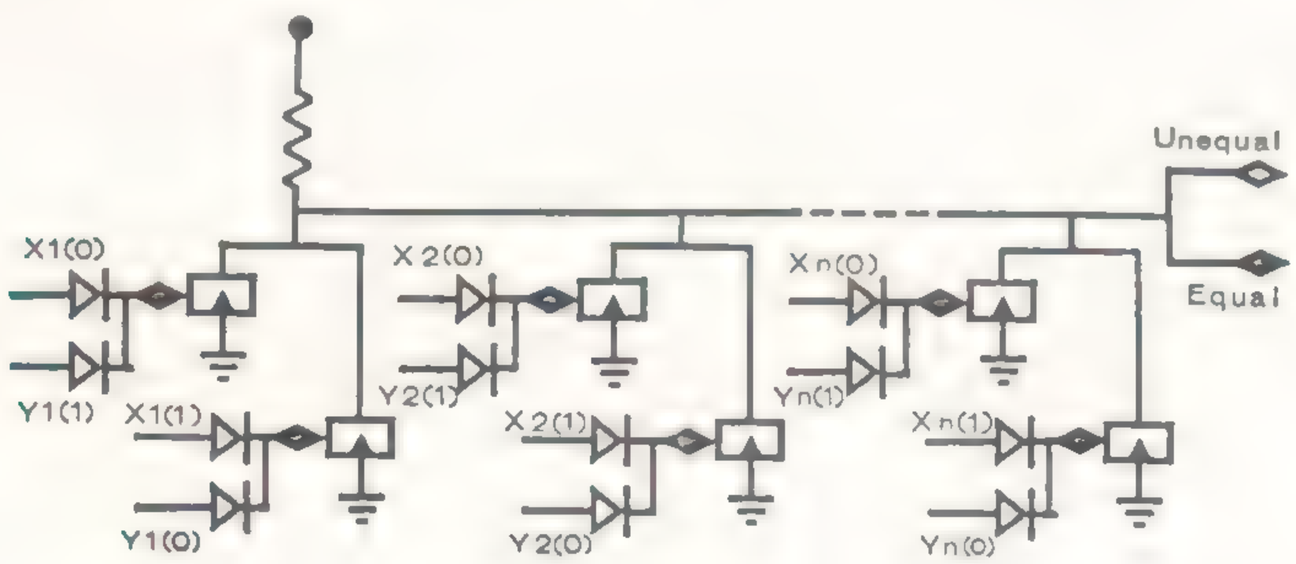


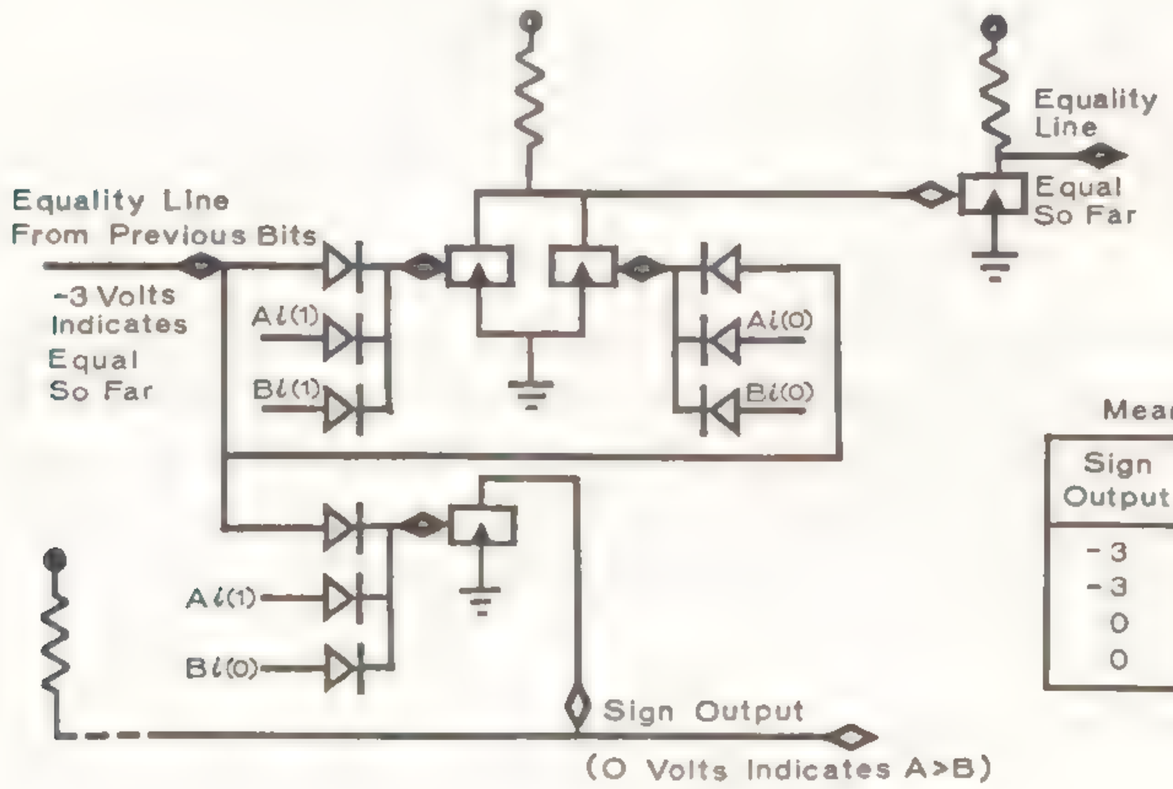
Figure 38
Comparator
(DEC Diodes Type 1113 or 4113)

Figure 38 shows an equivalent comparator with the inverters replaced by two-input diode units. Here the load determining factor is the i_{co} of the transistors. If only one unit Base Load is to be supplied by the output, then up to 100 pairs of diode gates may be used. If the number of pairs of diode gates is decreased, then the output driving ability is increased proportionally.

SIGN OF AN INEQUALITY

A more sophisticated comparator is used to compare the numerical value of two registers to determine equality or the sign of an inequality. This problem requires that each pair of bits be investigated in the order of their significance. Once an inequality has been discovered, all further investigation must be stopped so that the differences in bits of lesser significance will not affect the output.

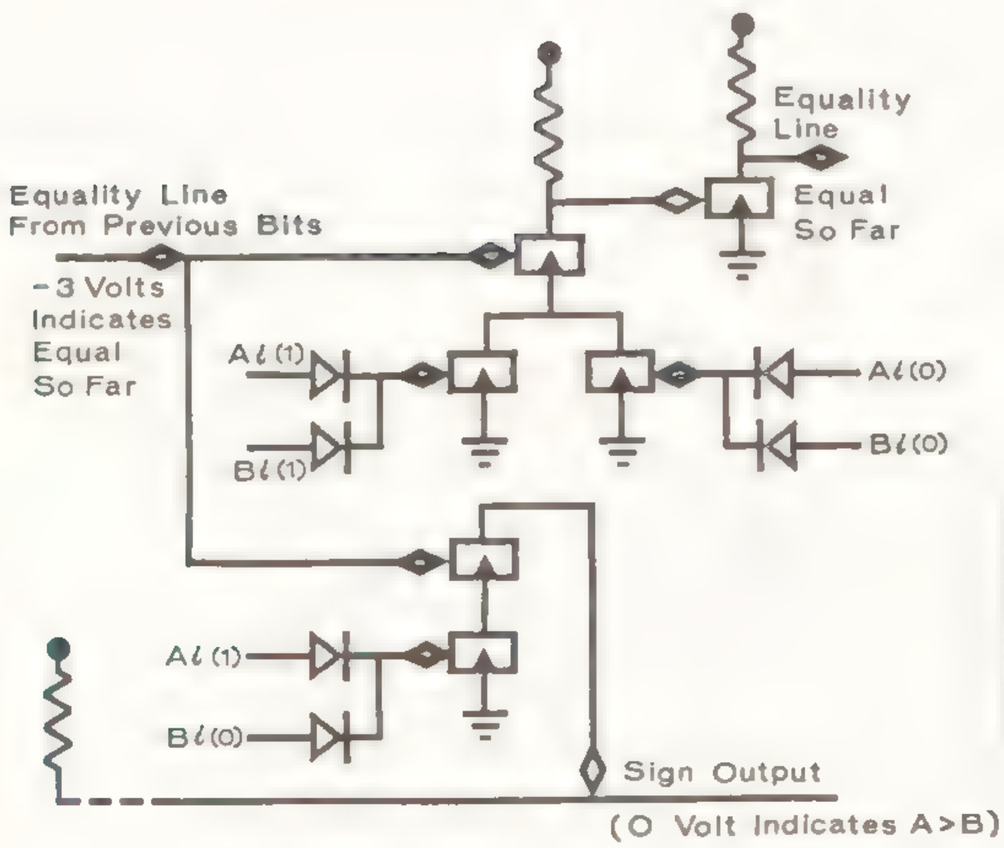
Figures 39 and 40 show the i^{th} stage of such a comparator chain. To begin investigation, the equality line is brought to −3 volts. This negative signal is ANDed with an EXCLUSIVE OR for the first pair of bits. If there is equality, then the negative signal will propagate down the equality line. If all corresponding pairs of both registers are equal, the negative signal will appear at the end of the final stage. However, if an inequality is reached, further investigation will be stopped and the equality line output will remain at ground. If this inequality is such that register A is greater than register B, then a ground signal will be generated at the sign output.



Meaning of Outputs

Sign Output	Equality Output	Meaning
-3	-3	A=B
-3	0	B>A
0	0	A>B
0	-3	Impossible

Figure 39
Comparator
(DEC Diodes Type 1115 or 4115)



Meaning of Outputs

Sign Output	Equality Output	Meaning
-3	-3	A=B
-3	0	B>A
0	0	A>B
0	-3	Impossible

Figure 40
Comparator
(DEC Diodes Type 1113 or 4113)

There is no limit to the number of stages through which the equality line may propagate. The restrictions on the sign output are similar to those described in the previous section. In Figure 39 the sign output is fed by diode units with grounded emitters. Thus, the output will drive one unit base load if it is connected to one clamped load resistor and up to 100 diode gates.

With the configuration for the sign output as shown in Figure 40, it may be necessary for a single "on" transistor to supply the base current for other transistors with both negative bases and emitters. If a standard clamped load resistor is used to define the output level, then a maximum of seven inputs may be connected. If the clamped load resistor is replaced by a 10,000 ohm resistor wired to the −15 volt terminal, then the maximum number of inputs is 14.

PARITY GENERATOR

A Parity Generator is a comparator which compares flip-flops within the same register. The circuits shown in Figures 41 and 42 are made up of EXCLUSIVE OR's as in the previous examples. Each EXCLUSIVE OR determines whether the sum of its two inputs is odd or even. The circuits are built up in a pyramid arrangement so that the output of the final EXCLUSIVE OR gives the parity of the sum of all the inputs.

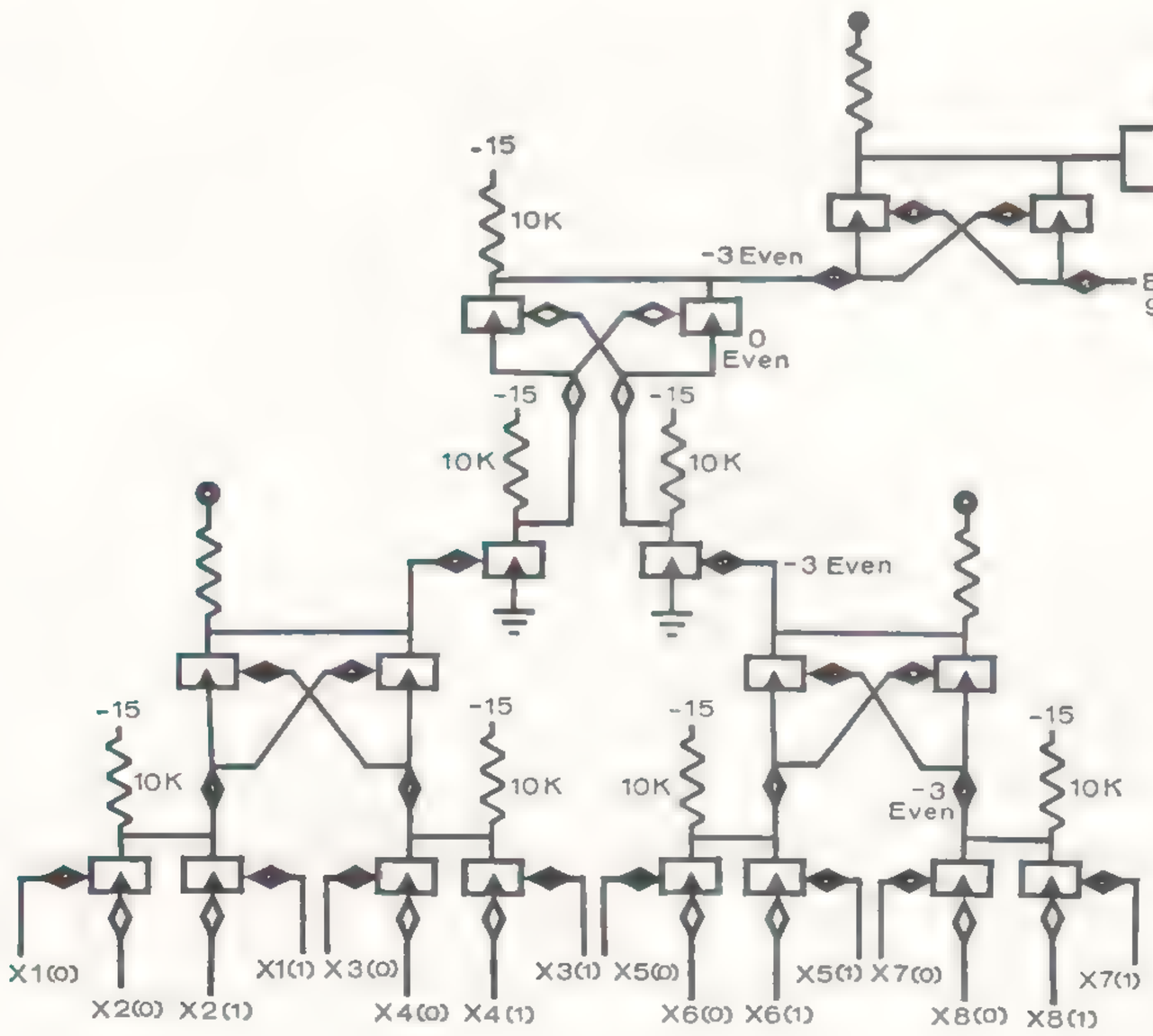


Figure 41
Parity circuit
(5 mc or 500 kc inverters)

To lighten the load on the inverters, 10,000 ohm resistors are used instead of standard clamped load resistors. The maximum series configuration is three inverters or one inverter and one 2-input diode gate. When the emitter of an inverter is driven from a flip-flop output (Figure 41), the flip-flop must be counted as an inverter.

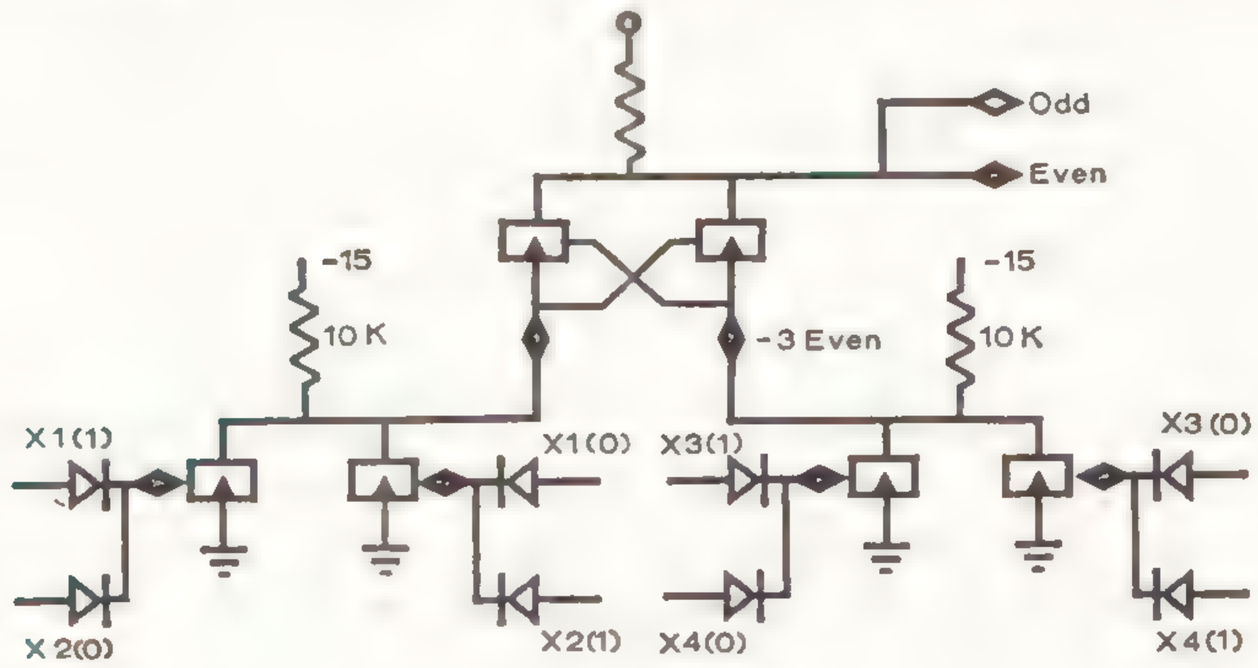


Figure 42
Parity circuit
(DEC Diodes Type 1113 or 4113)

SYNCHRONIZERS

Synchronizers are extremely important in any digital system, not only to determine what will happen if two asynchronous or incompatible signals occur, but also to assure that catastrophic errors will not result from such signals. Asynchronous signals are often commands such as start, stop or clear. Incompatible signals must be guarded against whenever a single flip-flop register is connected for more than one possible mode of operation.

Some typical cases where synchronizers are required are as follows:

1. Shift Registers — When a shift register is being changed from parallel mode to serial mode or vice versa, care must be taken that a split or partial pulse is not allowed to enter the system. Such a pulse could result in a partial shift, partial read-in or partial read-out. Likewise, a bi-directional shift register should never be commanded to shift left and shift right at the same time.

2. Counters — Particular care must be taken with start or stop signals which occur at random times relative to the counter input. If a synchronizer is not used, this situation might result in a split or partial pulse which would enter the system and propagate only part way down the carry chain. Thus, the entire number in the counter, or any part of that number, could be wiped out. A similar split pulse might occur in a bi-directional counter if the add and subtract inputs were pulsed simultaneously.

Basically, a synchronizer is accomplished by ANDing together a random input signal and a primary pulse train (usually a clock) and using the results of this AND gate to set a single flip-flop. If the random signal arrives while the clock pulse is occurring, the single synchronizer flip-flop makes the decision as to whether the signal will be accepted or rejected. Provision must also be made for the rejected signal to be accepted by the next clock pulse; thus, the input signal may be slightly delayed by the synchronizer flip-flop, but there will be no "middle" state which would activate only a portion of the main circuit.

LEVEL SYNCHRONIZER

Figure 43 shows a method of synchronizing a command level, such as a mode control, with a primary pulse train. When the input level is ground, the primary pulse train will be gated through terminal A. When the input level is negative, the primary pulse train will be gated through terminal B. If the input level is in the process of changing at the time the clock pulse occurs, then the decision to accept or reject the signal change will be made by the synchronizer flip-flop only. Thus, no pulses will ever be gated through both terminals A and B, and no split pulses will ever be gated through either terminal. This method, or a variation, is often used in controlling the direction of count in an up-down counter.

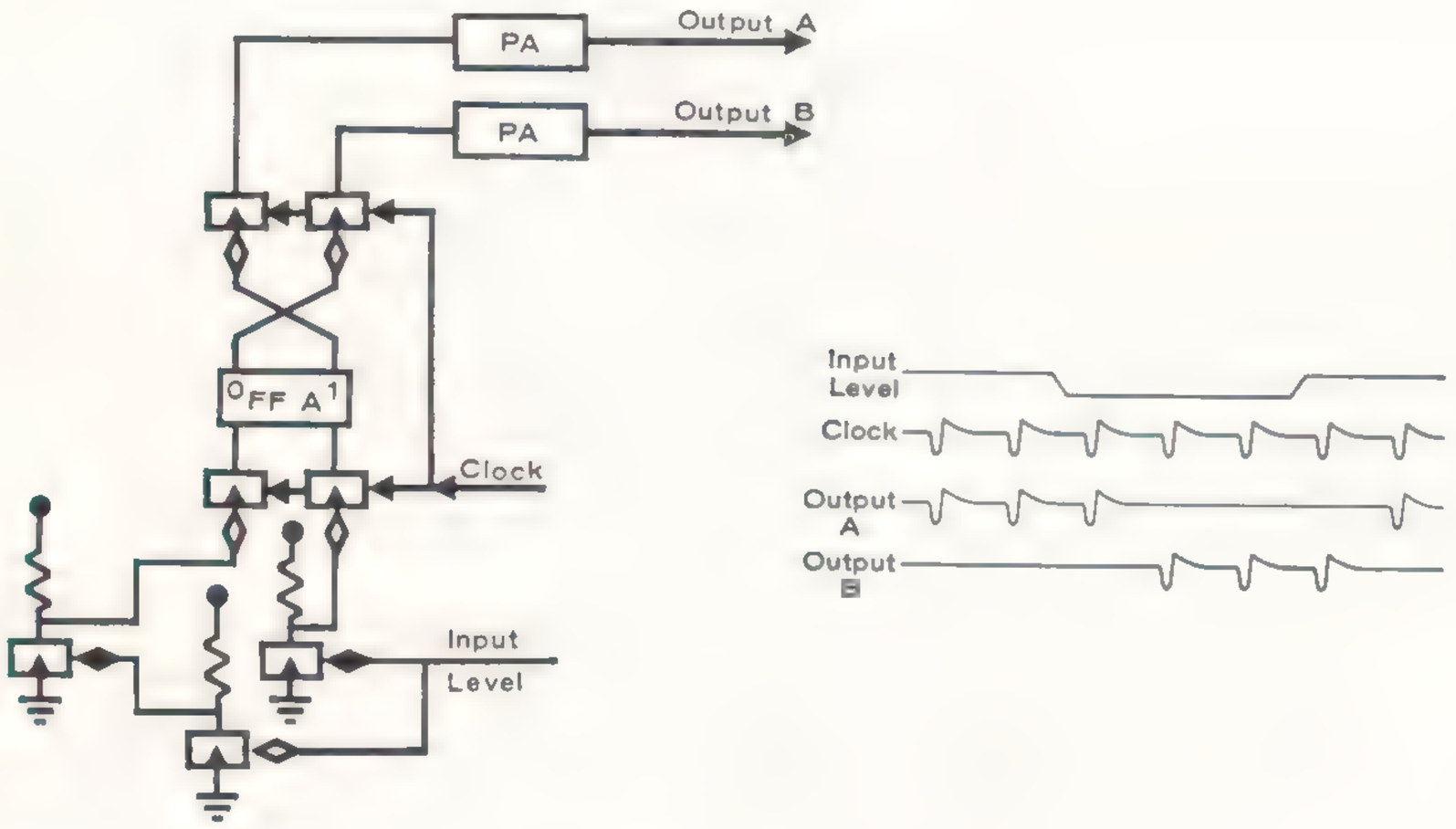


Figure 43
Level synchronizer
(DEC Flip-Flops Type 201, 1201, 1204, 1209, 3201, 4201, or 4209)

START-STOP SYNCHRONIZER

Figure 44 shows a method for synchronizing start and stop commands with a primary pulse train. This type of synchronizer is extremely important in counters which are used to measure time intervals.

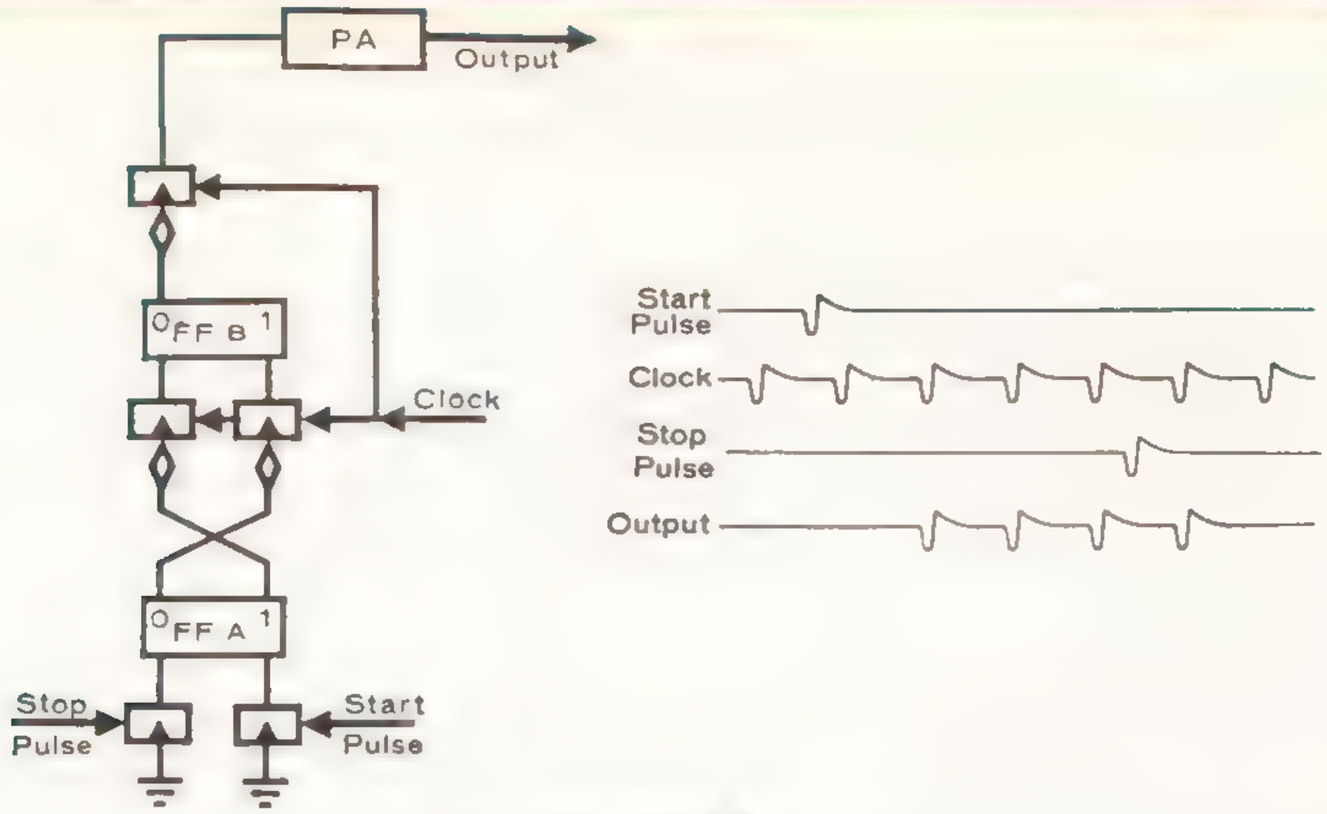


Figure 44
Start-stop synchronizer
DEC Flip-Flops Type 201, 1201, 1204, 1209, 3201, 4201, 4209, 5202, 6202 or 6208)

The random start and stop pulses will be converted to stop or start levels by flip-flop A. Flip-flop B will convert this randomly changing level into a level that changes synchronously with the clock. This level, in turn, conditions the output pulse train. The action may be delayed by one clock pulse. However, a split pulse will never be allowed to enter the main system.

SINGLE PULSE SYNCHRONIZATION

Figure 45 shows a method for synchronizing a single pulse with a primary train of pulses. The operation of the synchronizer is similar to that of Figure 44 except that the stop command is automatically generated by the first pulse to leave the synchronizer. Thus, one, and only one, pulse will pass into the main system, and this pulse will be synchronized with the clock.

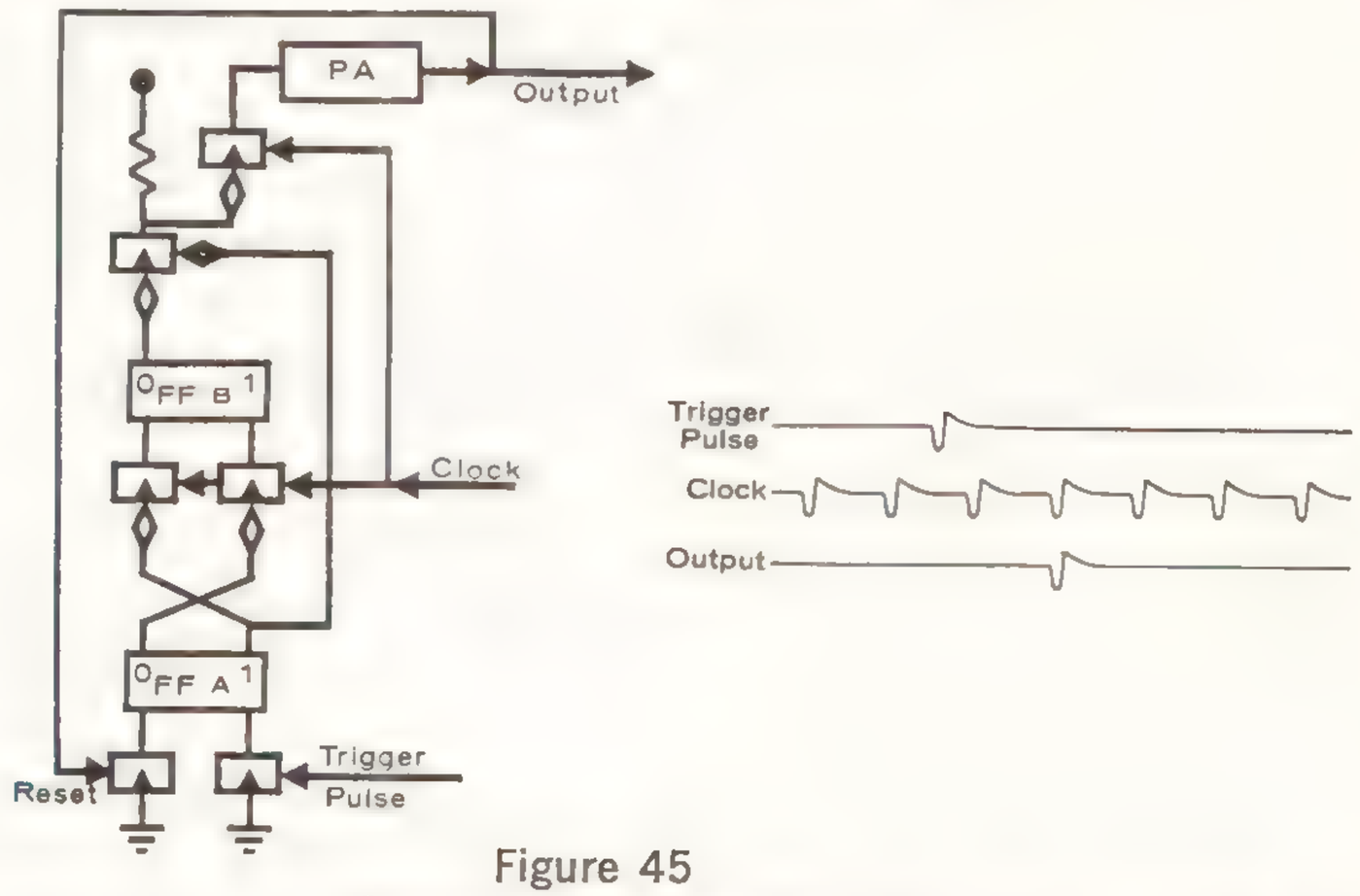
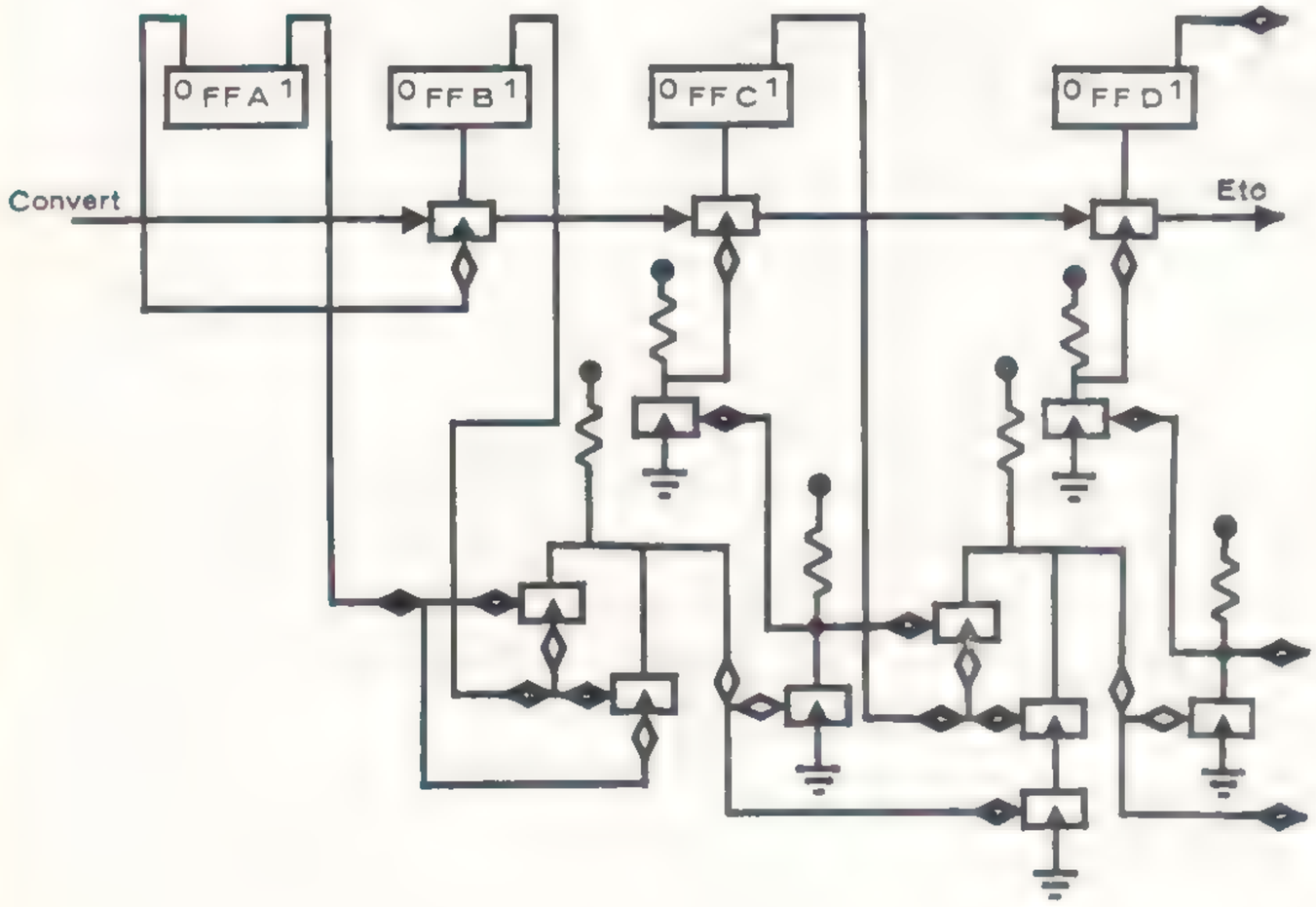


Figure 45
One-pulse synchronizer
(DEC Flip-Flops Type 201, 1201, 1204, 1209, 3201, 4201, or 4209)

GRAY-TO-BINARY CODE CONVERTER

A frequent problem in digital control work is to convert a Gray coded number, such as a shaft position, into a pure binary number so that it can be used conveniently in arithmetic operations. The DEC converter begins examination with the most significant bit and proceeds down the line, making use of two basic conversion principles: (1) the most significant digit is identical in Gray and binary and (2) if a digit is a 1 after being converted to binary, the following digit is complemented.

The DEC converter does not require any shifting or transferring of information. All logic is done by means of inverter gates, arranged in such a way that the convert pulse will simultaneously convert all digits from Gray to binary.



BINARY	GRAY
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
0101	0111
0110	0101
0111	0100
1000	1100
1001	1101
1010	1111
1011	1110
1100	1010
1101	1011
1110	1001
1111	1000

Figure 46
Gray-to-binary converter
(DEC Flip-Flops Type 201, 1201, 3201, 4201, or 4209)

UNBUFFERED FLIP-FLOPS TYPICAL APPLICATIONS

COUNTERS

A simple binary counter may be implemented quite easily with the 4215 Flip-Flop package as illustrated in Figure 47. The ONE output of each flip-flop is connected to the complement input terminal of the next flip-flop in the chain. Whenever a flip-flop goes from the ONE to the ZERO state, a positive going level change occurs at the ONE output terminal and complements the next flip-flop in the chain, thus producing a carry. The time required for carry propagation is approximately 50 nanoseconds per flip-flop.

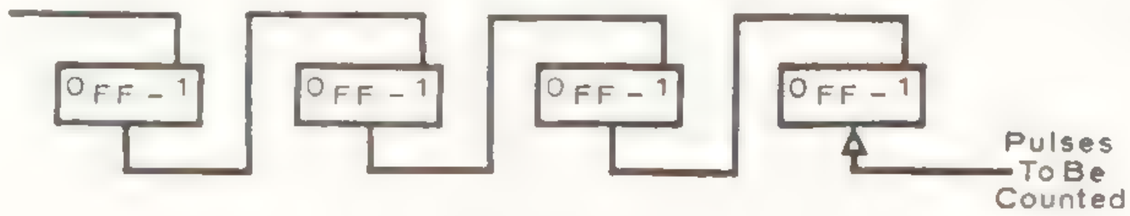


Figure 47
Up counter
(DEC Flip-flop Type 4215)

Since the act of clearing flip-flops will attempt to propagate carries, clear signals should be at least 1 microsecond in duration to allow all carries to die out.

SPECIAL COUNTS

Often it is desirable to build a counter that will produce a signal after a particular number of events have occurred. If this number is an integral power of 2, the output is automatically produced by the final bit of a counter of appropriate length. If this number is not a power of 2, special gating must be performed to detect the desired number, generate an output signal, and clear the counter. Two of the flip-flops in the 4215 package have special gates for this purpose.

Flip-flop A of the 4215 has conditional set and conditional reset input terminals. The conditional set will operate only when the flip-flop is in the ZERO state. The conditional reset will operate only when the flip-flop is in the ONE state. Thus the flip-flop will complement if the conditional set and reset are simultaneously pulsed.

The inhibit terminal on flip-flop C, if negative, will inhibit flip-flop C from being complemented to the "ONE" state. It will not, however, inhibit flip-flop C from being complemented from "ONE" to "ZERO".

Experimenting with the use of these terminals will illustrate many counts which may be achieved with no gating in addition to that included in the package. Figure 48 illustrates a count of 3 and Figure 49 illustrates a count of 5. The configuration shown in Figure 50 may be used to obtain a special count of $2^M(2^{N+1}+1)$.

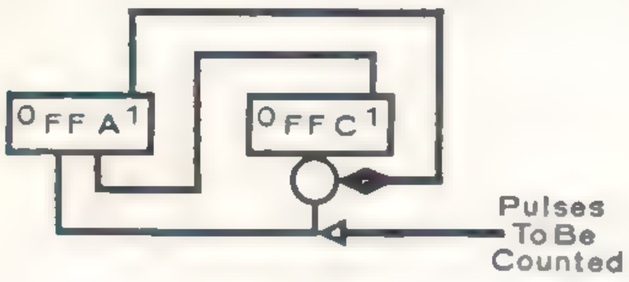


Figure 48
Count of 3
(DEC Flip-flop Type 4215)

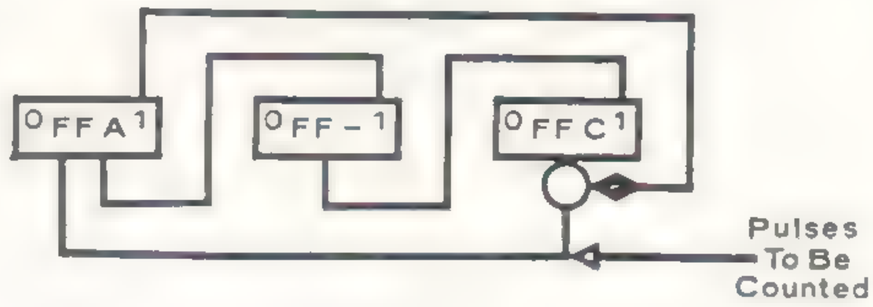


Figure 49
Count of 5
(DEC Flip-Flop Type 4215)

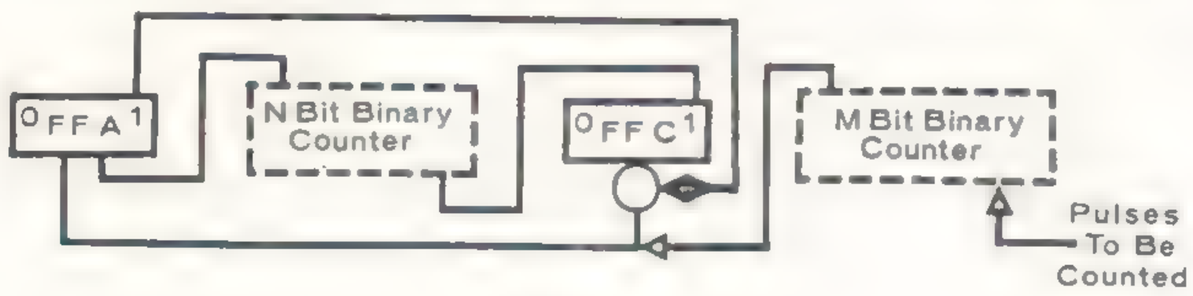


Figure 50
Count of $2^M(2^{(N+1)}+1)$
(DEC Flip-Flop Type 4215)

BINARY-CODED DECIMAL COUNTING

A one decade, binary-coded decimal counter, Figure 51, can be made from one 4215 package with no additional gates (See appendix A for an explanation of binary-coded decimal codes). The counter will operate as a binary counter until the most significant bit (flip-flop A) is in the ONE state. This will inhibit the input to flip-flop C. The next carry signal from flip-flop D will bypass flip-flop C and clear flip-flop A. Thus, the counter will be in the all ZERO state and a carry will be generated. The code being used is the 8-4-2-1 code and may be decoded with a DEC Type 1671 BCD Decoder and Light Driver, which has ten output lines for driving a decimal output display.

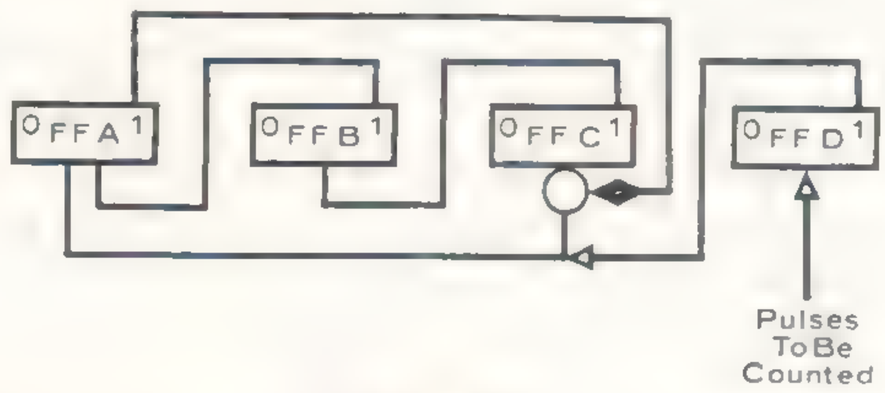


Figure 51
Count of 10, binary-coded decimal, 8421 code
(DEC Flip-Flop Type 4215)

Decades such as this may be cascaded indefinitely for any desired size counter.

TOGGLE SWITCH PRESET COUNTER

Figure 52 illustrates a general type of preset counter where the number of counts is determined by a toggle switch register. The desired number is set into the toggle switch register with a closed switch corresponding to a logical ONE, and an open switch corresponding to a logical ZERO. When the counter has reached the desired number, the output of the diode AND gate will go to ground. This will remove the inhibit signal from flip-flop C. The next count pulse which enters will set flip-flop C, thus clearing the counter. The following count pulse will add ONE to the counter and also clear flip-flop C. Each succeeding count pulse will add ONE to the counter until the desired number is again reached.

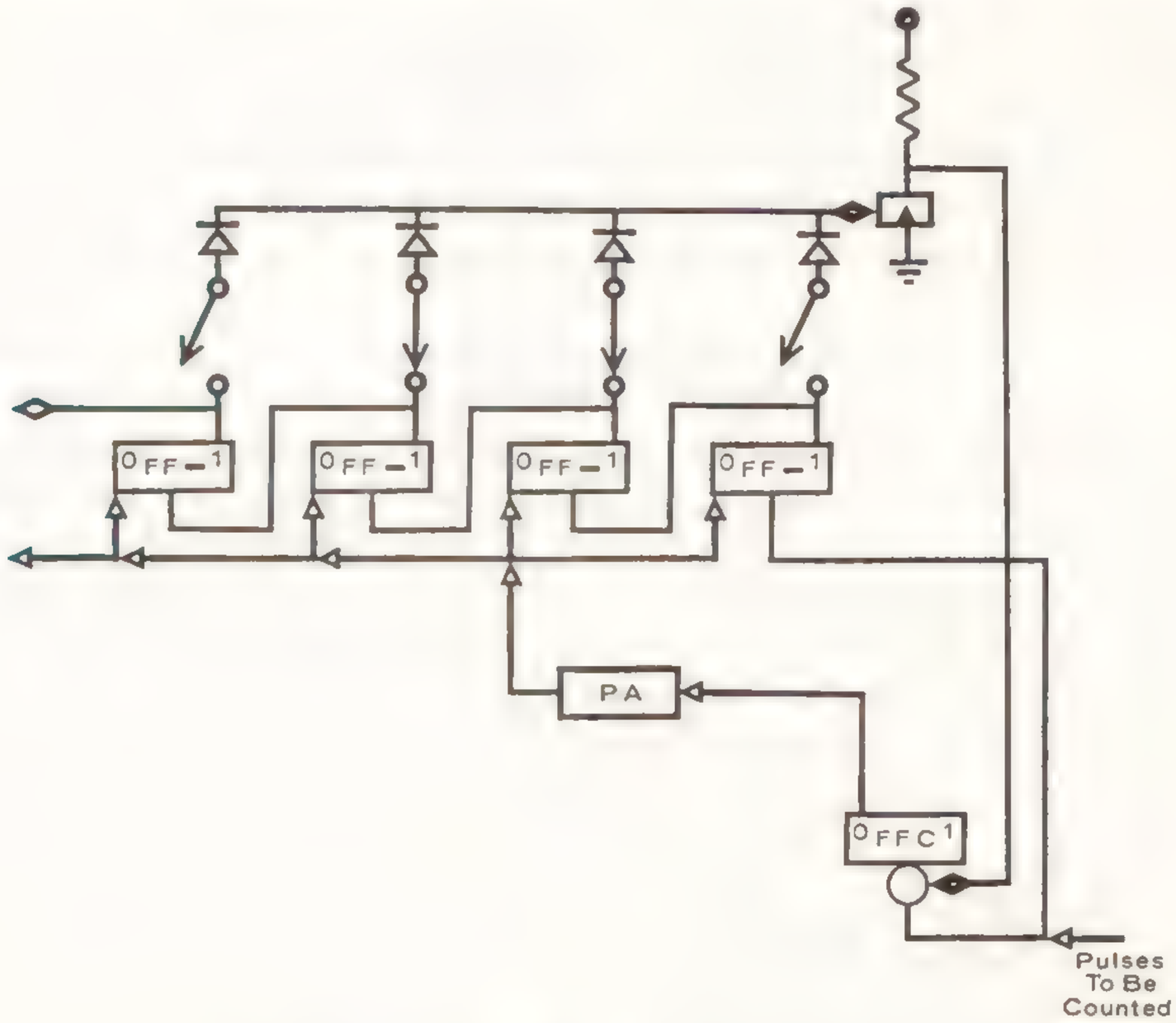


Figure 52
Preset counter (count of 7 illustrated)
(DEC Flip-Flop Type 4215 and Pulse Amplifier Type 4604)

At first, it would appear that this method of detecting the desired number could lead to ambiguities, since no ZERO states are detected. There is no ambiguity, however, since the counter always begins in the ZERO state and counts upward. In the above illustration for example, the condition for resetting the counter requires a ONE in flip-flops B and C. This condition could be met by the decimal numbers 6, 7, 14, and 15. Actually, however, the counter will always be reset after the count of 6 and, hence, will never reach other numbers. Since the resetting action requires an additional pulse, counted as number ZERO, the number of counts in a cycle is actually one more than the number indicated by the toggle switches.

Since clearing the counter will tend to produce carries, the clear pulse must be a DEC Standard 1 Microsecond Pulse such as produced by a Type 4604 Pulse Amplifier and Standardizer.

DOWN COUNTER

In a down counter, each successive pulse will decrease the count by 1. The method for building a down counter is essentially the same as that used in building an up counter, except that each flip-flop input is connected to the ZERO output terminal of the previous flip-flop rather than the ONE output terminal. In this way, a borrow chain is formed.

Flip-flops may be individually cleared in a down counter, since this does not generate a borrow signal. However if the flip-flops are to be set, provisions must be made to inhibit or override the borrows, as follows: Relabel the flip-flop outputs and use the direct clear input as a direct set input; or set the flip-flop with an inverter attached to the ZERO output terminal. In either case, the signal must have a duration of at least one microsecond.

UP-DOWN COUNTER

An up-down counter, as illustrated in Figure 53, combines the techniques found in individual up and down counters. Since it is necessary to isolate the carry chain from the borrow chain, Type 4125 Capacitor-Diode Gates are used. The count direction is selected by bringing to a negative voltage the conditioning level inputs of the appropriate chain of capacitor-diode gates. If a negative-going level change occurs at the pulse input of one of the conditioned capacitor-diode gates, a positive-going pulse will be produced at the pulse inverter output, complementing the next flip-flop in the chain.

For proper counting operation, only the selected capacitor-diode chain should be brought to a negative voltage; the conditioning levels of the other chain should be at ground. The counter may be complemented by bringing all capacitor-diode gate conditioning levels to a negative voltage and pulsing the input. If all conditioning levels are ground, and the input is pulsed, the first flip-flop only is complemented.

To assure sufficient set-up time for the conditioning levels, the conditioning levels should be brought to their final values at least 1 microsecond before the pulse is applied. The levels should be maintained until the carry or borrow has had sufficient time to propagate the entire length of the chain. The propagation time per stage is approximately 0.1 microsecond.

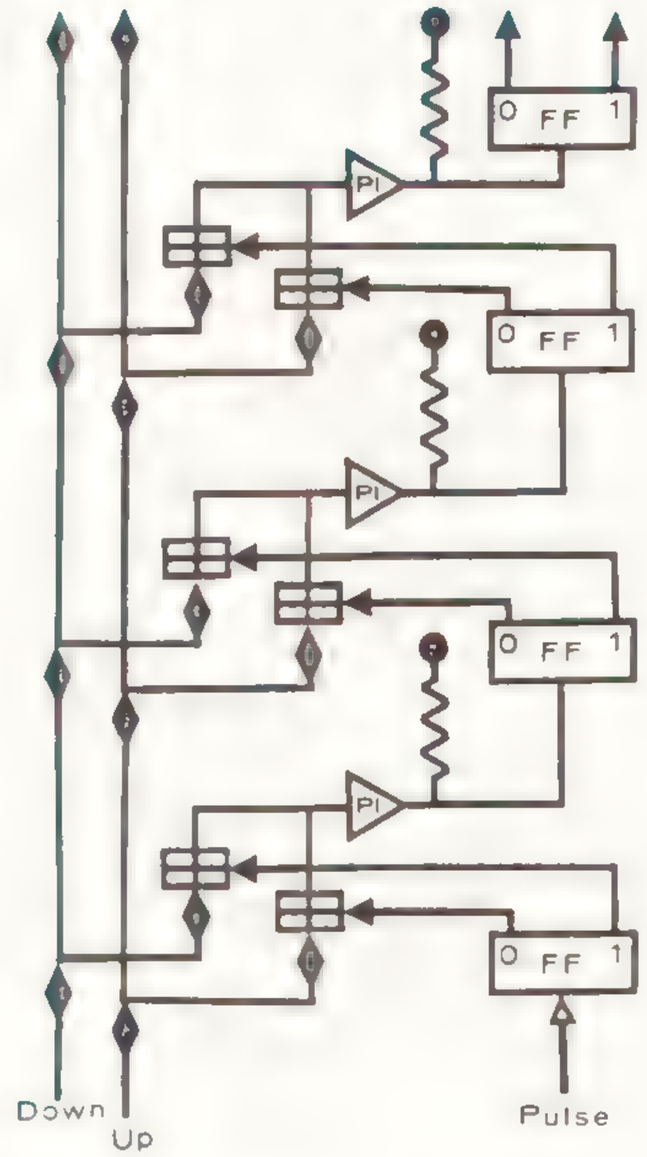


Figure 53
Up-down counter
(DEC Flip-Flop Type 4215)

BCD UP-DOWN COUNTER

A BCD up-down counter uses the same techniques as a binary up-down counter. Special gating is added such that, when the counter is at nine, a count up level followed by a pulse will clear the counter and generate a carry. In a similar manner, when the counter is in the ZERO state and an appropriate count down signal is applied, the counter will be set to nine and will generate a borrow signal. Figure 54 illustrates one decade of a BCD up-down counter employing the 8421 code.

The conditions governing the capacitor-diode gate conditioning levels are the same as those for a binary up-down counter; however, since the 8421 code is not self-complementing, the act of pulsing the counter with both conditioning chains at a negative voltage would result in a meaningless number.

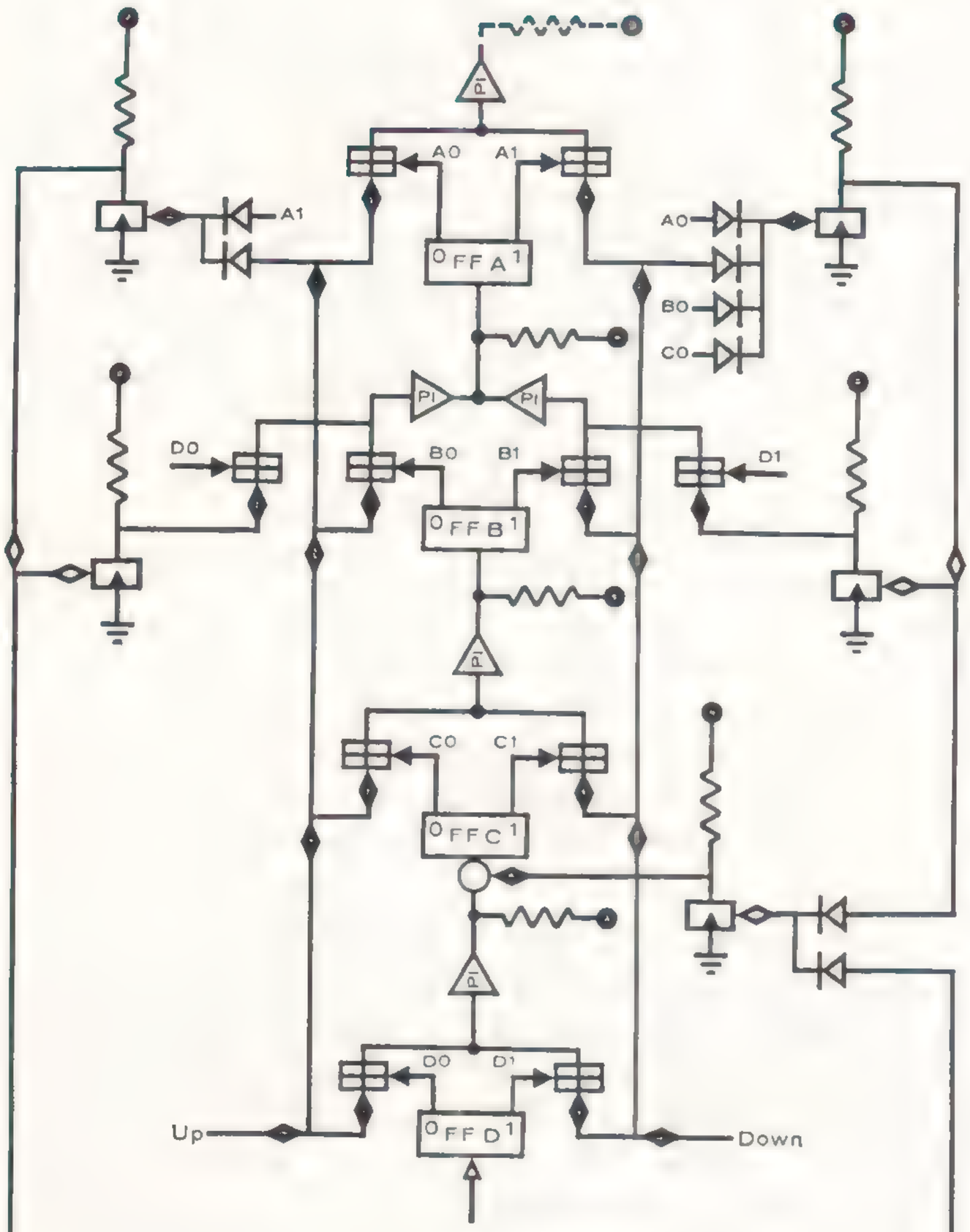


Figure 54
BCD up-down counter, 8421 code
(DEC Flip-Flop Type 4215)

A simpler BCD up-down counter can be made using the Excess 3 code (see Appendix A for an explanation of this code). An Excess 3 up-down counter takes advantage of the fact that a 0 to 9 transition and a 9 to 0 transition are both made by complementing all flip-flops in the decade. Figure 55 shows a counter employing this technique.

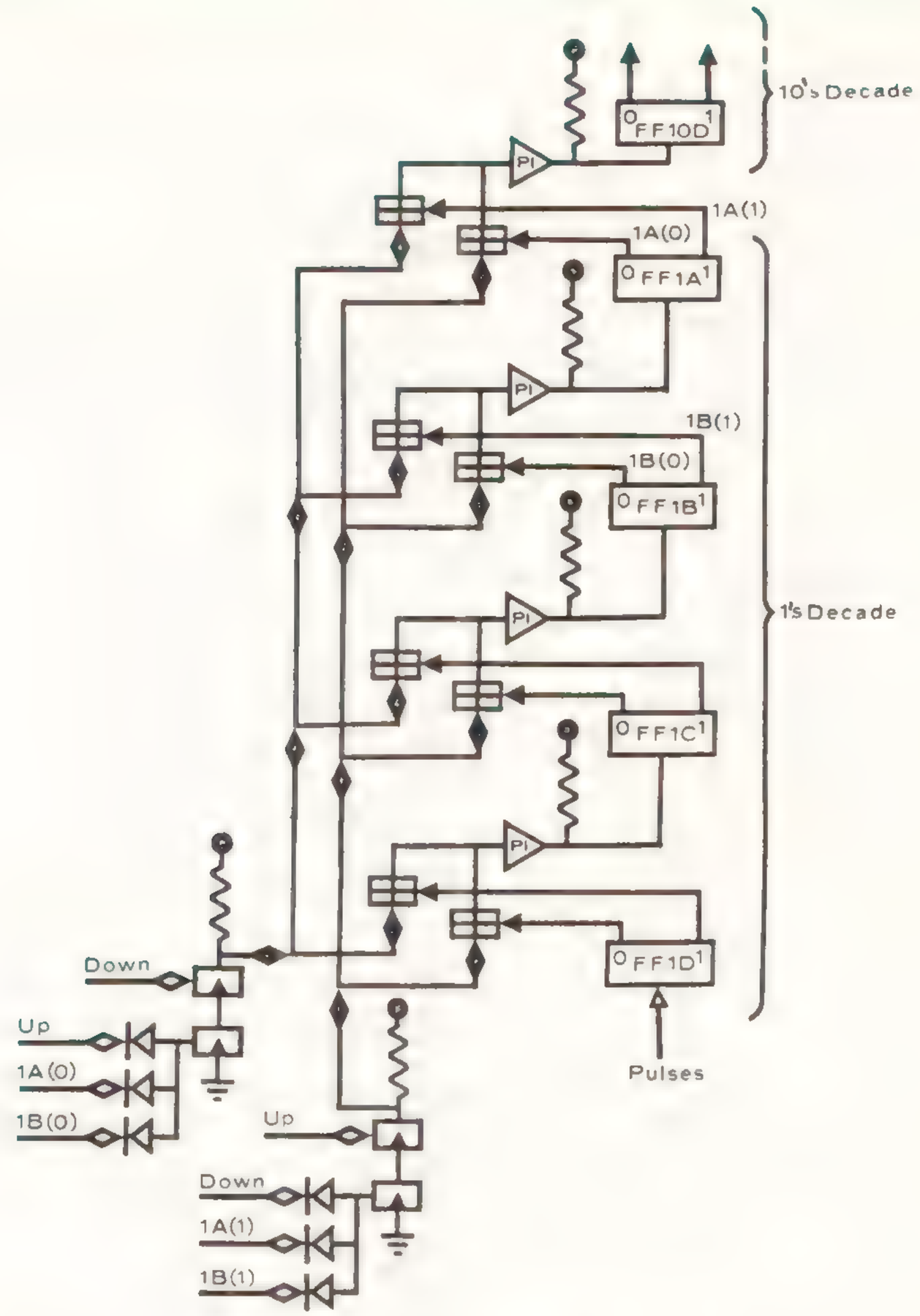


Figure 55
BCD up-down counter, Excess 3 code
(DEC Flip-Flop Type 4215)

SHIFT REGISTERS

DEC Shift Registers employ "jam transfer" gating. Two capacitor-diode gates connect the outputs of each flip-flop to the inputs of the next flip-flop in the register. All capacitor-diode gates are simultaneously pulsed and the contents of all flip-flops are simultaneously moved forward. Such gates are included in the Quadruple Flip-Flop Types 4213 and 4216. With additional gates, shift registers may be implemented with any type of DEC Flip-Flops.

Figure 56 illustrates how a DEC Type 4215 Flip-Flop may be used to implement a shiftable counter.

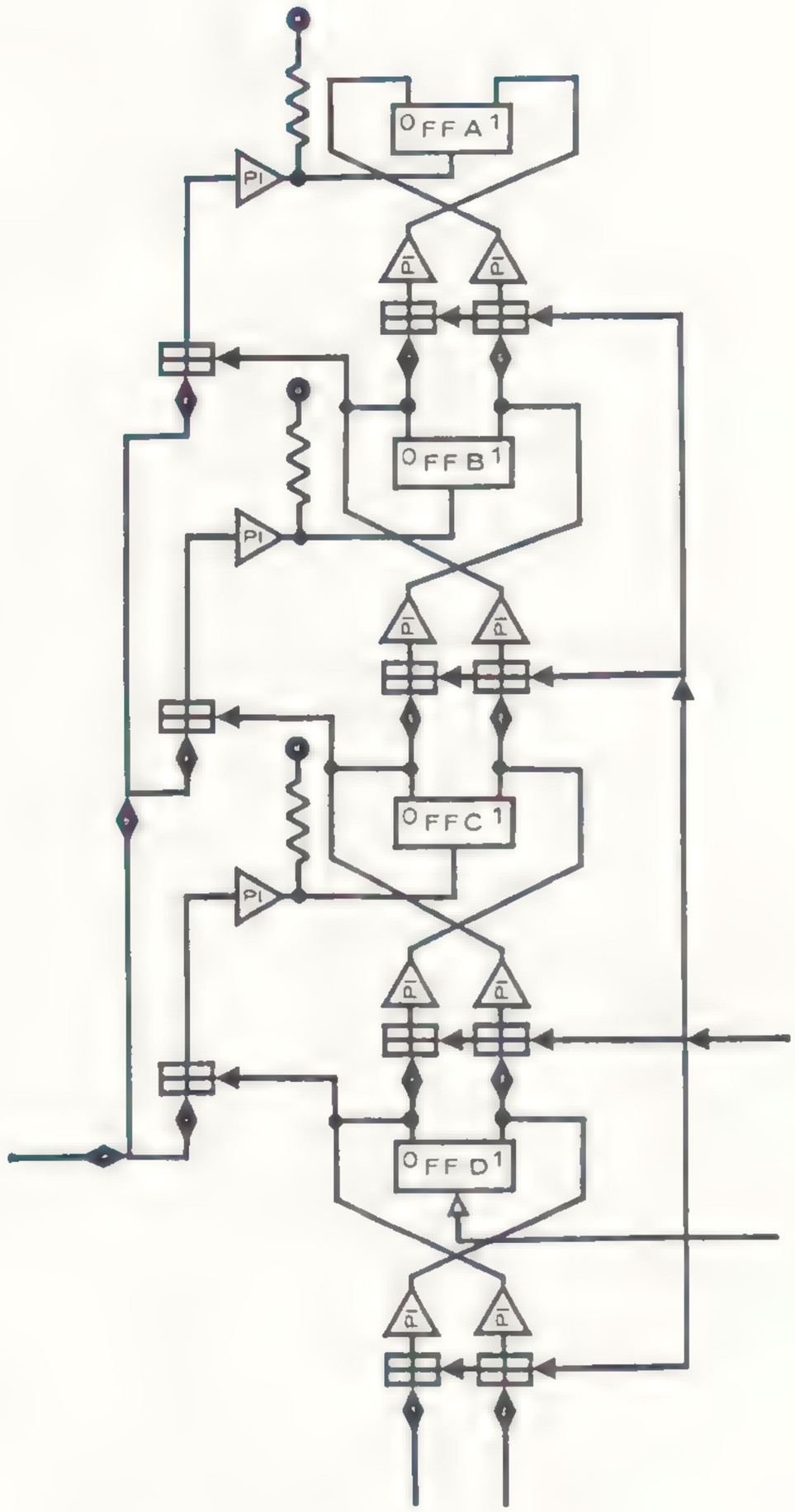


Figure 56
Shiftable counter
(DEC Flip-Flop Type 4215)

ADDERS AND SERIAL ADDERS

Figure 57 illustrates a bit-by-bit adder. The content of register A is added to register B and the sum is stored in register B. The two numbers to be added are read into registers A and B with the least significant bits in flip-flops A_N and B_N. When a shift pulse is received, the content of each flip-flop is advanced one place. The least significant bits are added, together with the carry, and read into flip-flop B_O. If a carry occurs, it is stored in the carry flip-flop. When (N + 1) shift pulses have been received, the sum is located in register B.

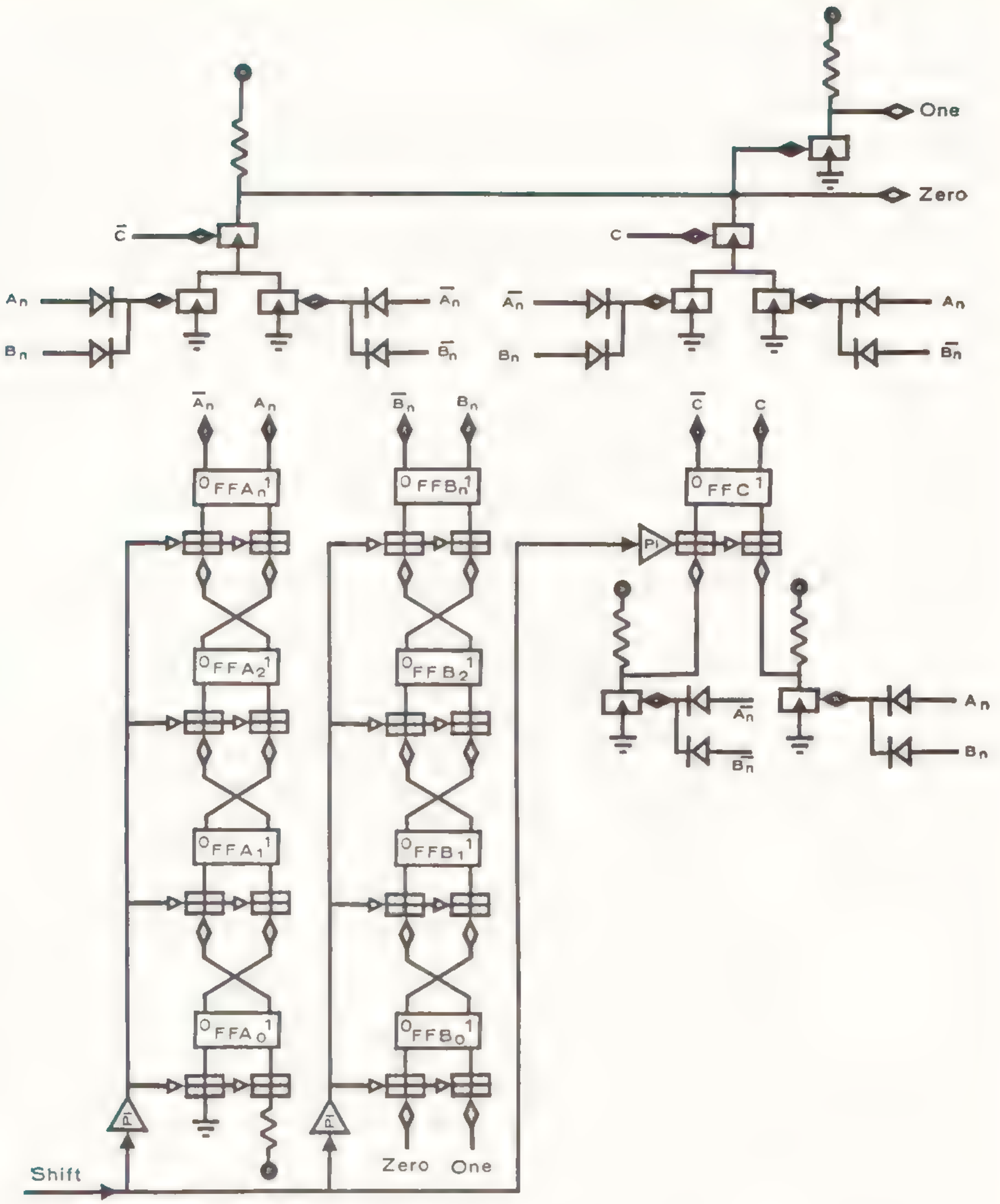


Figure 57
Serial adder
(DEC Flip-Flop Types 4213, 4214, 4216 or 4218)

Variations of this technique can be used to make a serial subtracter, multiplier or divider.

PARALLEL ADDERS

Parallel addition of the contents of an incident number register to the contents of an accumulator is accomplished in two discrete steps, half-add and carry, as shown in Figure 58. Isolation of the two steps is made possible by the use of negative capacitor-diode gates.

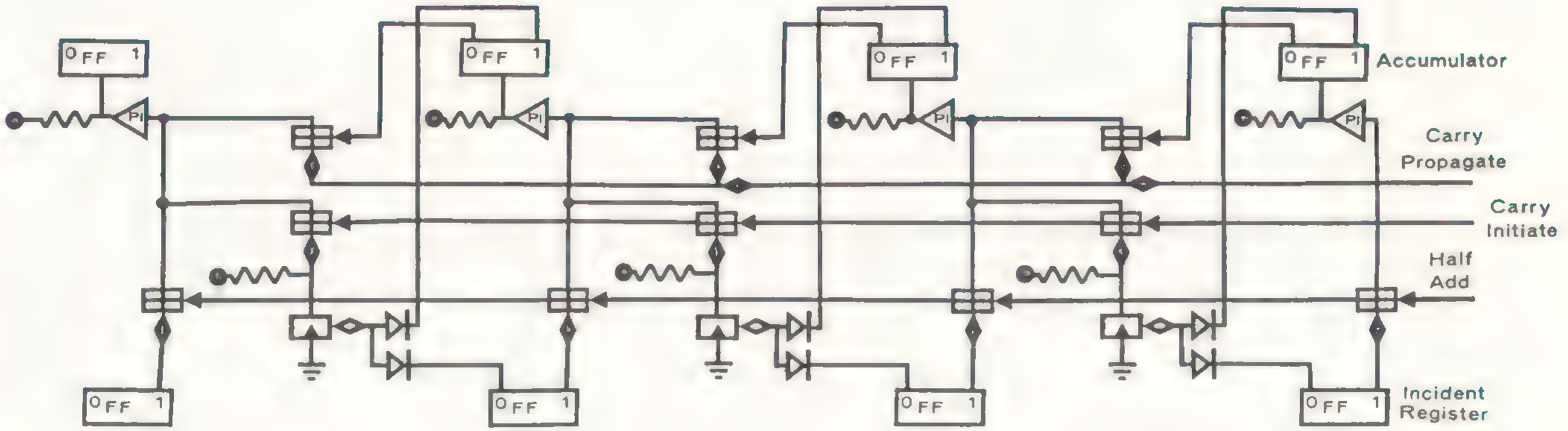


Figure 58
Parallel binary adder
(DEC Flip-Flop Type 4215 for accumulator)

The first step is half-add. Each digit of the accumulator is complemented if the corresponding digit of the incident number is a ONE.

The second step is a carry. A carry will be generated if a bit in the accumulator is ZERO and the corresponding incident number bit is a ONE. The carry will be propagated if an accumulator bit is a ONE and it also receives a carry pulse from the next less significant accumulator digit. After the carries have been propagated, the contents of the incident number register may be modified to add another number to the accumulator.

INCIDENT NUMBER	ORIGINAL ACCUMULATOR NUMBER	ACCUMULATOR AFTER HALF-ADD	ACCUMULATOR AFTER CARRY
001	010	011	011
001	001	000	010
001	011	010	100

Table II

Variations of this technique can be used for a parallel subtracter, as described on page 30.

BCD PARALLEL ADDERS

The technique used in designing a BCD adder depends upon the particular code desired. Codes which are derived from the binary number system can be implemented in a standard binary adder with an appropriate correction factor to account for the fact that a BCD decade uses only ten of the sixteen possible states.

The basic steps for complete addition are as follows:

1. Add the two BCD coded numbers in natural binary fashion.
2. Look to see if the number in any decade must be corrected.
3. Add (or subtract) the necessary correction factor.

In the 8421 code, a correction factor of +6 (0110) must be added whenever the sum exceeds nine (1001). Since the addition of this correction may yield a carry into the next stage, each decade must be corrected individually, beginning with the least signficant decade.

Since the sum of two numbers in Excess 3 code will be a number which is excess 6, a correction factor of −3 (1100) must be added if the sum has not exceeded nine and a correction of +3 (0011) must be added if the sum has exceeded nine. The advantage of this code, however, is that the carry signal will propagate during the first addition process. Thus, corrections for all decades may be made simultaneously.

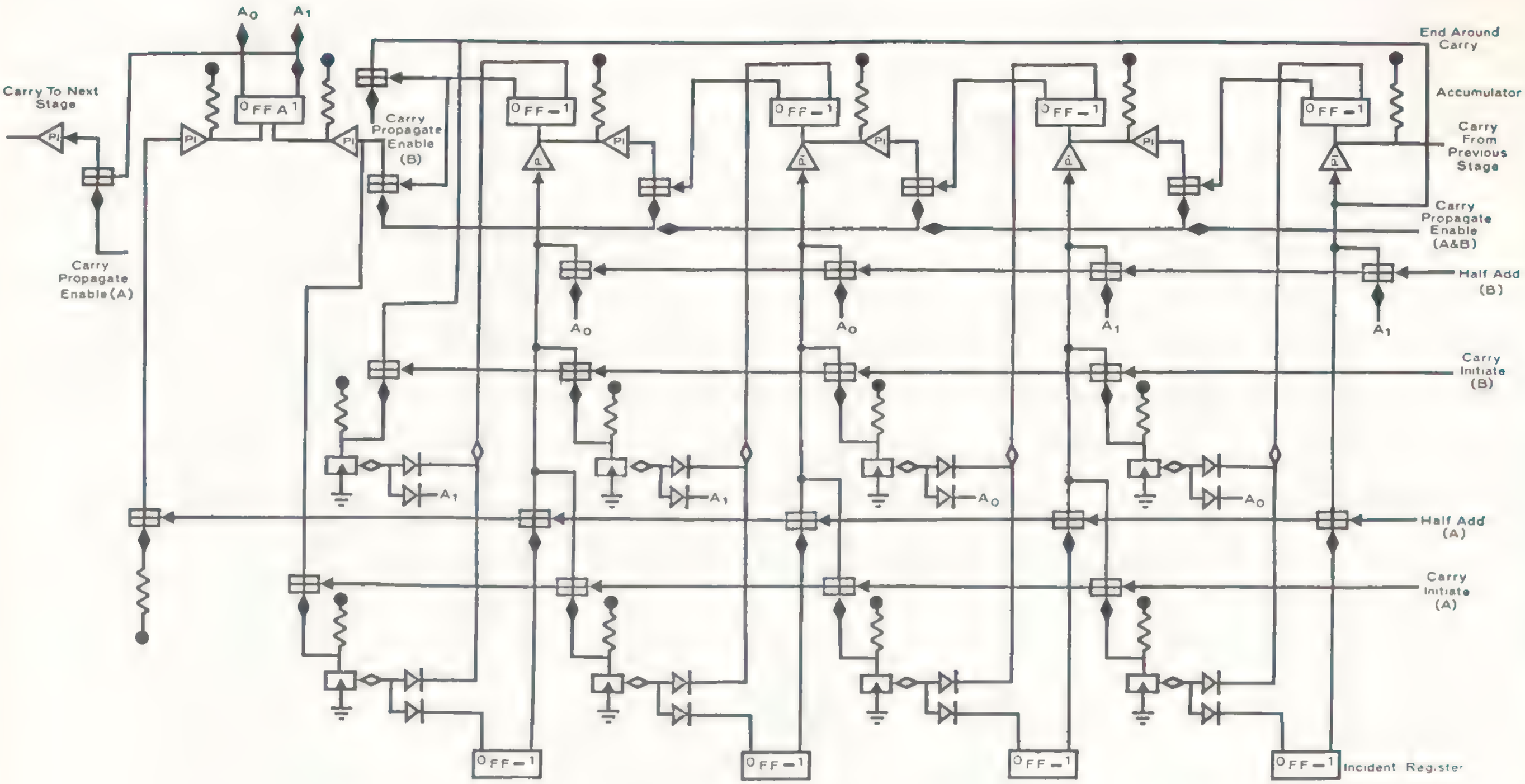


Figure 59
BCD parallel adder, Excess 3 code
(DEC Flip-Flop Type 4215 for accumulator)

Figure 59 illustrates an Excess 3 adder. The carry signal, which indicates the sign of the correction factor, is detected with a special flip-flop. This carry flip-flop automatically conditions the appropriate gates for addition of the correction factor. It is important to note that, during the initial addition, a carry signal from the decade is both recorded and propagated on to the next decade. During the addition of the correction factor, the carry flip-flop is cleared and the carry path is gated back to the first flip-flop in the decade, thus allowing an end around carry if necessary.

SUBTRACTION

The Excess 3 code is a self-complementing BCD code; that is, the NINE's complement of any number may be obtained by complementing each bit. Thus, subtraction may be implemented by complementing the incident number, adding this number to the accumulator, and generating an end around carry as with binary ONE's complement notation.

The excess 3 BCD adder illustrated may also be used for subtraction. This requires one additional carry gate,which is connected from the most significant bit of the most significant decade to the least significant bit of least significant decade. This end around carry gate operates only during the first addition process. During the correction process, the special intradecade end around carry gates operate.

COMPARATORS

Comparison of two flip-flop registers (A and B) requires an "EXCLUSIVE OR" for each corresponding pair of bits since there are two possible conditions which will produce an inequality, i.e., bit A-1 equals 0, and bit B-1, equals 1, or A-1 equals 1, and B-1 equals 0. The entire set of "EXCLUSIVE OR's" must then be OR'd together to determine when any pair of bits is unequal. Figure 60 illustrates the use of the Type 4139 Diode Gate for comparison of two 4-bit registers. When the two registers are equal, the output will be negative; when the two registers are unequal, the output will be at ground.

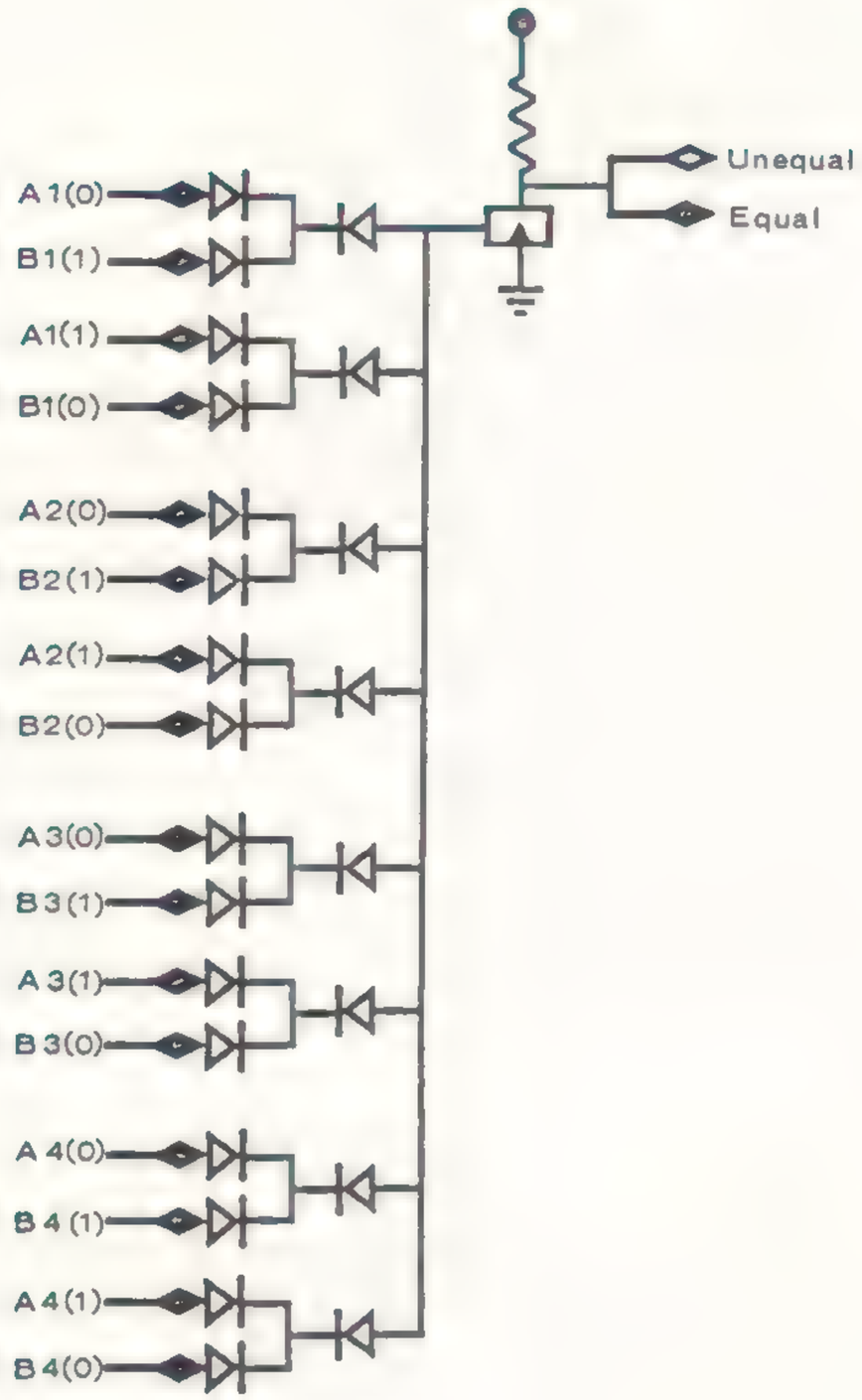


Figure 60
Comparator
(DEC Diode Gate Type 4139 or 4141)

Extending this technique to larger registers may be accomplished by placing the 4139 Gates in parallel. A single clamped load resistor is attached for all 4139's.

DEFINITIONS

LOADING DEFINITIONS

To facilitate the design of systems, a number of simple loading definitions and rules have been made. These do not cover all possible configurations, but they do serve as a useful guide.

A "BASE LOAD" is the current which must be taken from the base of a DC inverter to keep it in a saturated state. In this condition the inverter base input terminal is at −3 volts, the transistor base is at ground, and nominally 1 ma current is drawn through the 3000 ohm base resistor to ground. Inverter load resistors, when clamped at −3 volts, nominally have 12 volts across their 1500 ohms, and they can nominally accept 8 milliamperes of current. Ideally, this would drive 8 units of BASE LOAD, but tolerance considerations limit the number to 7.

A "PULSE LOAD" is the load presented to a pulse source when driving the base of an inverter. Pulse amplifiers are usually limited to driving 16 pulse bases. This number should be decreased if the bases are widely separated, and it can be increased to 18 if they are all close together. The series inductance and shunt capacity of the connecting wires can make the pulses at the end of a string of bases either large or small. Consequently, when a number near the maximum is being driven, the pulse amplitude should be carefully checked after installation. A terminating resistor in the 100-to-300 ohm range is desirable to reduce ringing on a heavily loaded pulse line.

A "PULSE LOAD" is also the load seen by a pulse source when driving one direct set or direct clear input of a flip-flop. The loading on a pulse source is approximately the same as when driving a base. One pulse source, of course, cannot drive both direct inputs of flip-flops and inverter bases because the direct input pulses are positive from a normal ground level and base input pulses are negative from a normal ground level.

A "PULSED EMITTER LOAD" is the load seen by the collector of an inverter driving the pulse input to a flip-flop, pulse amplifier or delay. The pulse current goes through all the inverters in series with the pulse input, and it should be assumed to be the load on each of the series inverters.

A "DC EMITTER LOAD" is a load seen by the collector of an inverter driving a clamped load resistor. This load is also seen by the collector of an inverter which is driving an emitter in a network of inverters which is terminated by a clamped load resistor.

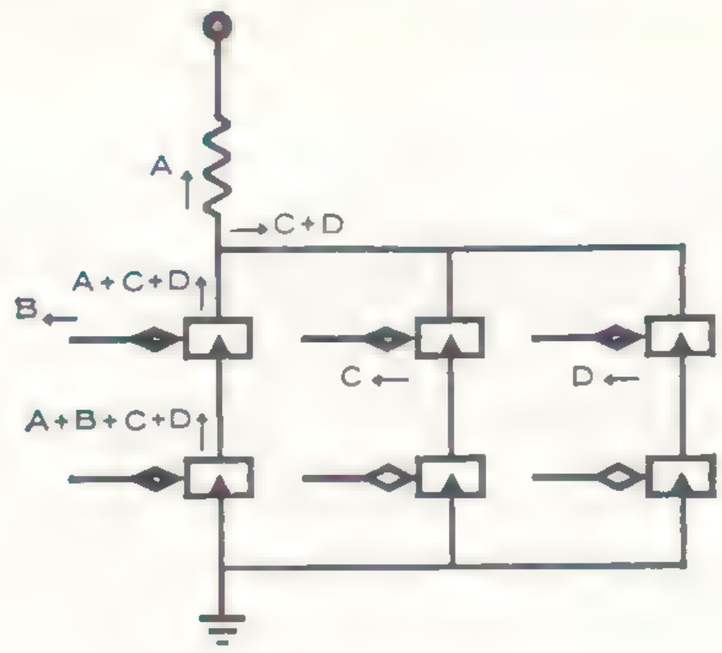


Figure 61

The collector of an inverter driving an emitter in a network of transistors must also supply the base current leaving the inverters higher in the chain. This number is normally small, but in complex networks it must be considered.

An inverter can drive no more than one clamped load resistor and six bases of "on" inverters. Since transistors are almost symmetrical, this "on" base current can also flow through the collector of a transistor whose emitter is open, as shown in Figure 61. In this case, the collector of the bottom "on" transistor must carry the current A from the load resistor and the base currents from B, C and D. Nominally, the current required is 10 ma to a negative voltage return; however, this is increased by the base current required. Most inverters can supply 15 ma collector current; 20 ma can be supplied by the inverters in Module Types 3101, 3110, 3201, 3602, 4102, 4105, 4106, 4110, 4111, 4201, and 4603.

A "CAPACITOR-DIODE GATE LEVEL INPUT" does not present any DC load. A transient load occurs when the input level changes.

TIME DEFINITIONS

"LEVEL DELAY TIME" is the time delay between the point of 10% input change and the point of 10% output change in a given circuit. The input is assumed to be the output of a DEC Flip-Flop of the same frequency line as the circuit under discussion, or a level change with similar characteristics. This is also referred to as delay for output fall or delay for output rise.

"PULSE DELAY TIME" is the time delay between the point of 10% input change and the point of 10% output change in a given circuit, when the input is a DEC Standard Pulse of the same frequency line as the circuit under discussion.

"RISE TIME" and "FALL TIME" are the time delay between the 10% and 90% points of a voltage change.

"TOTAL TRANSITION TIME" is the time delay between the point of 10% input change and the point of 90% output change in a given circuit. It is the sum of delay time and rise (or fall) time.

"SET-UP TIME" is the time required for a capacitor-diode gate to "open" or "close" after a change of input level. This time is measured from the point of 10% input change.

"SETTLING TIME" (used in digital-to-analog converter networks) is the time delay between the point of 90% input voltage and the time when the ladder has settled to within one least significant bit.

CURRENT CONVENTION

Since digital logic circuits employ two voltage levels, it is always assumed that the current is flowing from one level to the other. That is, if the output of a digital device is at its more negative level, the current will flow to the more positive level and vice versa. If a digital unit is an exception to this rule, the voltage return for the load current is stated.

On special input devices, linear amplifiers, and similar circuits, there are not necessarily two distinct possible states. For this reason, conventional current flow is used here. +ma indicates that the current is flowing from a positive voltage to a negative return and −ma indicates that current is flowing from a negative voltage to a positive return.

Power requirements for −15, −3, and +10 volts assume that the current drawn will be flowing to ground.

STANDARD SIGNALS

"DEC STANDARD LEVELS" are 0 and −3 volts. The tolerance on the more positive level is 0 to −0.3 volts. The tolerance on the more negative level is −3 volts to −4 volts.

"DEC STANDARD NEGATIVE PULSES" are −2.5 volts in amplitude with a positive overshoot of similar amplitude. These pulses are referenced to ground. The overshoot pulse is necessary to allow the transformer to recover, and also cleans out holes in the transistors, increasing the speed of logical operations.

The "DEC STANDARD POSITIVE PULSES" are identical to the Negative Pulses except that the polarity is reversed.

The timing characteristics of DEC Standard Pulses are commensurate with the speed line. For the 3000 and 4000 Series, pulses have a duration of 0.4 microseconds. For the 100 and 1000 Series, the pulse duration is 70 nanoseconds. For the 5000 and 6000 Series, pulse duration is 40 nanoseconds.

A detailed description of the requirements for external input signals which may be used as the equivalent of DEC Standard Pulses is outlined for each series under the pulse amplifier descriptions of that series.

GAIN

"GAIN" is defined as change in output voltage divided by the change in input voltage.

INVERTER USAGE

5 MC AND 500KC MODULES

DEC transistor inverters serve two functions. When used as level gates, they are placed in series and parallel configurations to perform logic. When used as pulse gates, the inverter will sample the logic performed by the level gates and read the results into a flip-flop or other active element.

When used as a pulse gate, an inverter will drive one and only one pulsed unit. Inverters serving as level gates are usually considered as simple switches when designing logical networks, but because they are not ideal switches, there are certain limitations which have to be taken into account. The voltage drop across saturated inverters is not zero; it is closer to 0.1 volt. As a result, inverters cannot be stacked indefinitely. Three inverters is the maximum which can be put in series if the output is to drive another inverter, as in Figure 62.

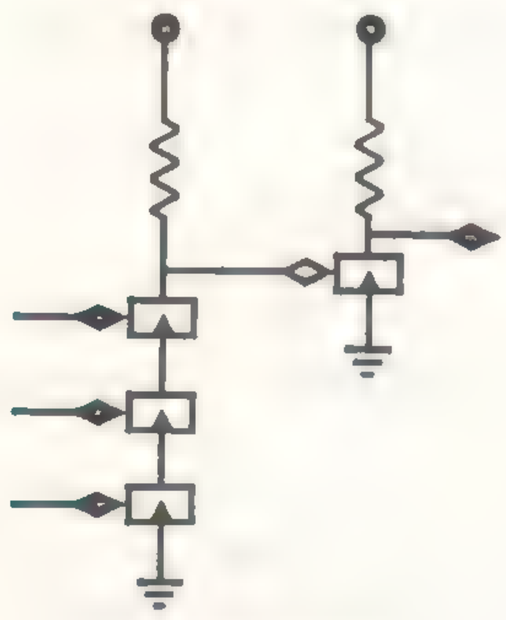


Figure 62

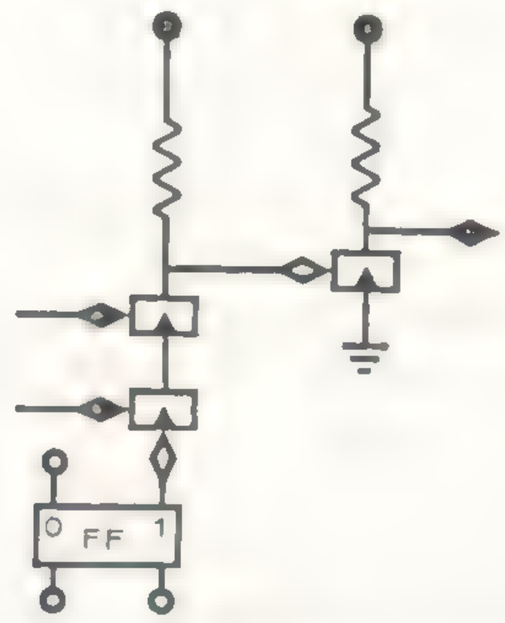


Figure 63

If inverters are in series with the output of a flip-flop, as in Figure 63, the flip-flop buffer inverter is considered to be one of the three allowed series transistors.

When the output of a series of inverters is driving the input of a pulse amplifier or delay unit or the set or clear input of a flip-flop, as in Figure 64, a fourth transistor serving as a pulse gate may be added in series. Only three may be used in series when driving the complement input of a flip-flop.

It is important to note that a clamped load resistor is tied to the emitter of each pulse transistor when it is being driven from an inverter or a network of inverters, as in Figure 64.

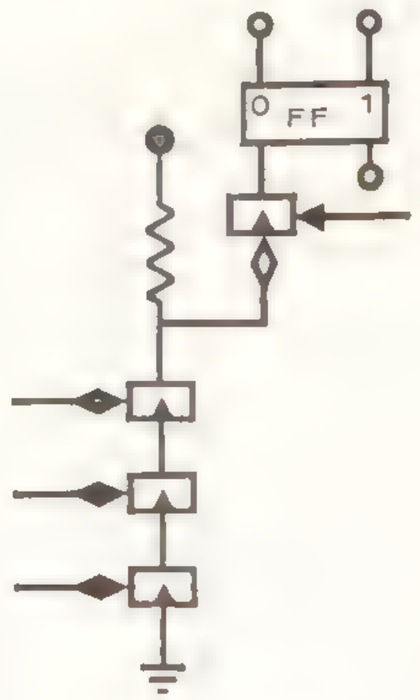


Figure 64*

Because inverters are not really ideal switches, each collector of a series string of DC inverters supplying a pulse inverter will go somewhat negative during the pulse. This means that, if a series of inverters is supplying both pulse current and a DC signal, care must be taken because a signal will occur in the DC output during the pulse.

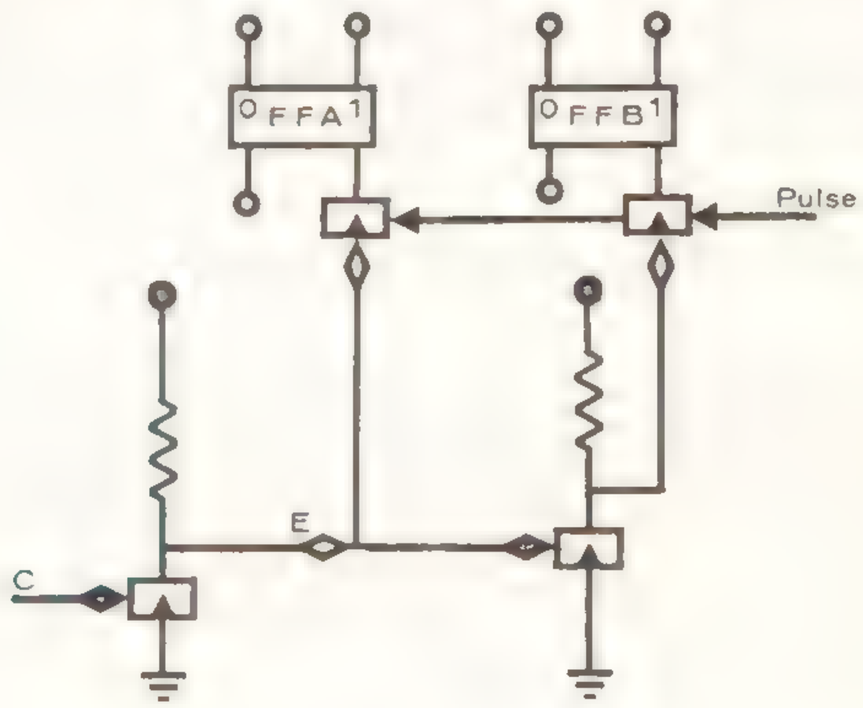


Figure 65

In Figure 65, when the input C is negative, flip-flop A should be set by the pulse, but flip-flop B should not be set. However, during the pulse, collector E of the DC inverter feeding flip-flop A will go slightly negative. It will partly turn on the

*The clamped load resistor is not needed in 5 megacycle circuitry when the pulse inverter is driven from a single series of inverters and the length of wire between inverters is short.

In the 500 kilocycle line this clamped load resistor can be replaced by a 1N276 diode from the emitter of the pulse inverter to ground, connected so as to prevent this point from going positive.

DC inverter feeding flip-flop B, and sometimes it will set flip-flop B as well as flip-flop A. This network will work only if the pulses are not simultaneous.

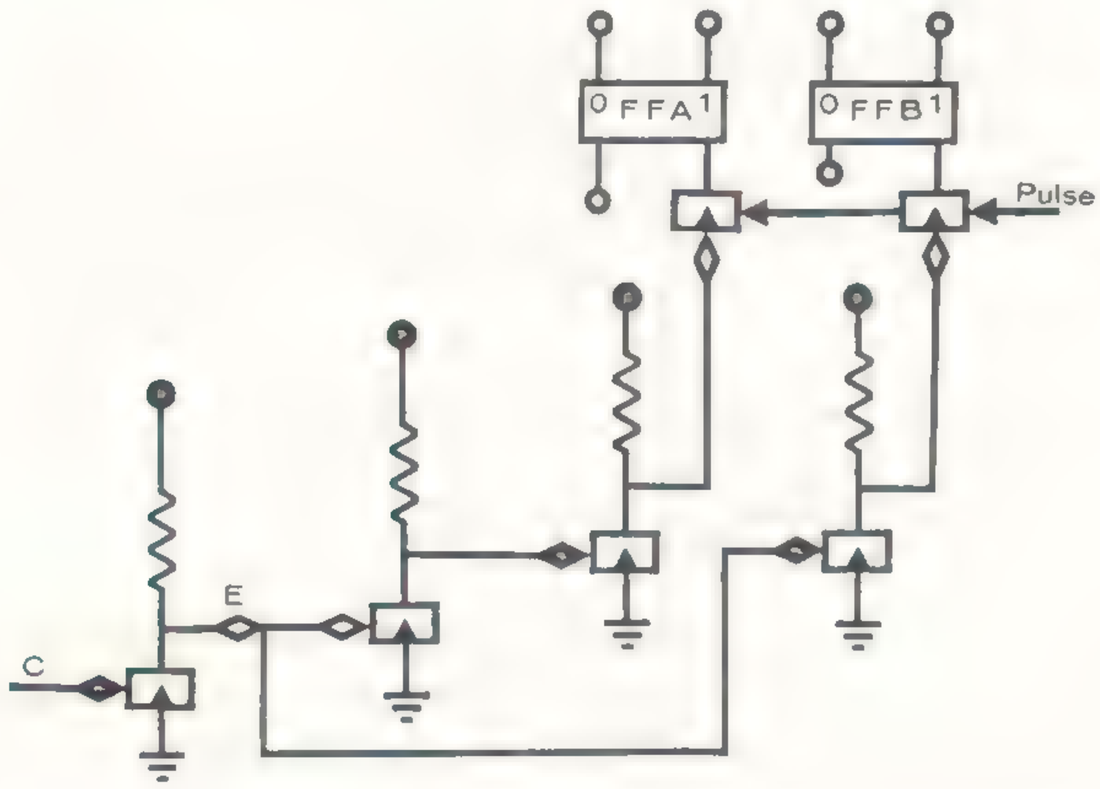


Figure 66

The network shown in Figure 66 will work whether or not the pulses are simultaneous. Two additional inverters have been added so that collector E will no longer be pulled negative by the pulse, since the pulse current will now come directly from ground instead of collector E. (If both outputs are driving the same flip-flop, the network shown in Figure 65 can be used safely because the output of the A side will be much greater than that of the B side.)

10 MC MODULES

The high speed transistors used in 10 megacycle inverters have a larger saturation voltage drop than the transistors used in the 5 megacycle and 500 kilocycle inverters. Because of this slightly larger DC drop, a maximum of two inverters may be put in series if the output is to drive another inverter. (See Figure 67). If a flip-flop output is driving an inverter emitter, this flip-flop must be counted as an inverter (See Figure 68).

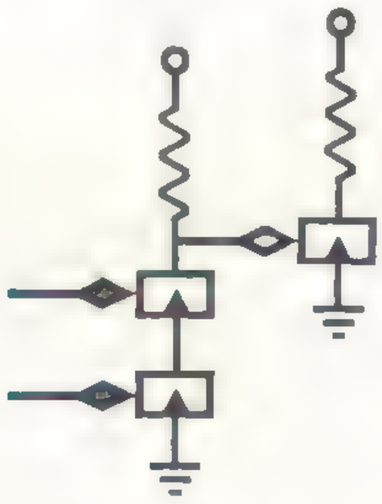


Figure 67

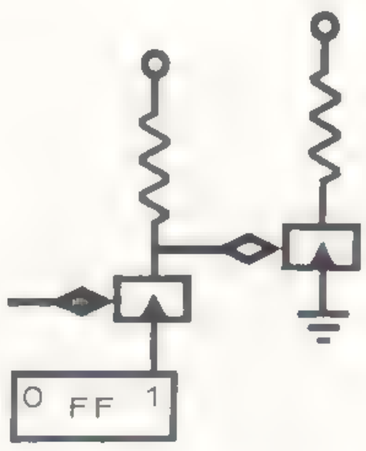


Figure 68

When the output of a series of transistor inverters is driving the input of a flip-flop or pulse amplifier, as in Figure 69, an inverter pulse gate may be added in series with the two level gates. This pulsed inverter must be placed at the bottom of the series string; that is, the end farthest from the load. The emitter may be driven by a flip-flop unless the sampling pulse is a P pulse (the carrying pulse in counters); in this case the emitter should be grounded.

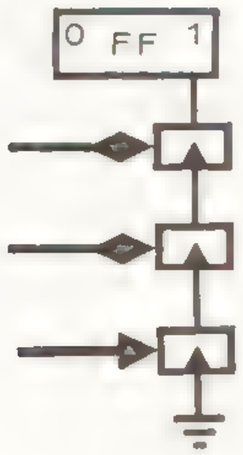


Figure 69

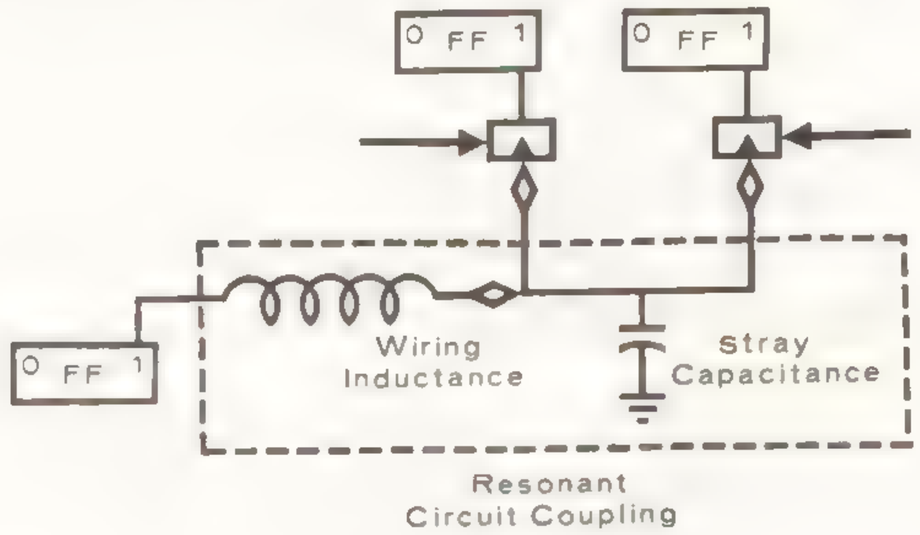


Figure 70

When connecting 10 MC inverters, the user should avoid wiring inductance and stray capacitance as much as possible. Figure 70 illustrates how a wire, which is conducting current for two pulsed inverters back to the flip-flop output, may serve as a coupling connection between the two pulsed inverters and produce ringing. This ringing may produce a positive pulse of the emitter of the other inverter, thus turning it on at the wrong time. To avoid this, each emitter must be driven by a separate wire, unless the distance is very short.

MARGINAL CHECKING

Marginal checking is used in a system to find the margin of safety between the condition of a system and the point of failure. Marginal checking is normally used in routine maintenance to find deteriorating components before they cause system failure. In many instances routine marginal checking is not necessary due to the long life of modern transistors, but it is still invaluable in debugging a new system. Without marginal checking, a system may be assembled with a number of mistakes which do not cause failure but which do not provide the system with as much margin as it should have.

In systems made with DEC Modules, the +10 volt bias on inverters is varied for marginal checking. In most Modules, the +10 inputs are broken into two groups to make possible most critical marginal checking. In large systems, like the DEC Programmed Data Processor, the +10 lines to the Modules are broken down into several groups so that small portions of the system can be marginal checked at one time.

If the inverter transistor has marginal gain, it will fail when the +10 supply is increased less than 5 volts because the drive to the base of that transistor is lessened.

Reducing the positive bias on an inverter will detect noise on the inverter input or a condition where the input does not come sufficiently close to ground. Normal margins on a system are plus and minus 5 volts on the +10 volt supply. In most systems an indicator lamp is connected to each flip-flop to show its logical state. In DEC Laboratory Modules the indicator lamps are built into the flip-flop units with their own transistor drivers.

INDICATORS

Types 1669 and 1675 plug-in units are used to drive indicators with the System Modules. The indicator drivers are power transistors in an inverter circuit, very much like a logic inverter except that the 3000 ohm resistor in the base is not bypassed with a capacitor.

The load of the inverter is the incandescent lamp, which is tied to the −15 supply. When the inverter is on, the full 15 volts is across the lamp bulb. Normally, a GE 327 aircraft-type indicator lamp bulb is used. This is a conveniently small bulb with very good life characteristics. It is rated at 24 volts, but when operated at 15 volts the light output is pleasant, and the life of the lamp is very long.

The DEC Type 4671 BCD Light Driver is designed to drive a decimal display from either a binary coded decimal register or an Excess 3 coded decimal register. This unit decodes a decade (four flip-flops) into ten lines and amplifies the output. The output will produce up to 150 milliamperes at −20 volts. This is sufficient for a GE 47 lamp, such as those used in the Industrial Electronic Engineers Model 10000-47 decimal display unit.

INTEGRATING MODULES OF DIFFERENT FREQUENCIES

No special interconnecting units are necessary for adjusting currents and voltages when mixing units from different series. Timing characteristics, however, are commensurate with the maximum speed of each series, and timing differences must be taken into account.

In the 10 megacycle lines, pulses are 40 nanoseconds wide and flip-flops have a built in delay of 30 to 75 nanoseconds. In the 5 megacycle lines, pulses are 70 nanoseconds wide and the built in flip-flop delay is 65 to 135 nanoseconds. The 500 kilocycle units use 400 nanosecond pulses; the buffered flip-flops have a delay of 0.5 to 1.3 microsecond.

Whenever it is desired to go from a higher speed unit to a lower speed unit, the pulse must be lengthened using a pulse amplifier with feedback. This method is illustrated in the technical descriptions of the pulse amplifiers in Section 3 (in the case of the 4000 Series, a 4604 pulse amplifier and standardizer).

In going from a lower speed line to a higher speed line, no changes in the pulse shape need to be made unless the long pulse is being used to complement a flip-flop or the pulse is being used to activate a unit which will be activated again while the longer pulse is still present. An example of this last case would be a counter made from 5 megacycle and 500 kilocycle equipment. It would be possible to use a 400 nanosecond pulse to clear all of the flip-flops in the counter provided that the first flip-flop would not be expected to count within 500 nanoseconds. When a narrower pulse is to be generated from a wide one, the wide pulse is appled to the input of a pulse amplifier of the higher speed series. The output of this pulse amplifier will be a standard pulse of the correct width.

A high speed flip-flop may not be changed and simultaneously sampled with a low speed pulse.

The quadruple flip-flop packages and their associated capacitor-diode gate packages use a somewhat different method of timing than the buffered flip-flop packages. In the quadruple units, the delay is contained in the capacitor-diode gates rather than in the flip-flops. Thus, if a quadruple flip-flop is to be changed and sampled simultaneously, it must be sampled with a capacitor-diode gate rather than an inverter. Any of the negitive capacitor-diode gates (Types 4125, 4127 or 4129) may be used to sample a 4000 series unbuffered flip-flop and drive a buffered flip-flop or other pulsed unit such as a pulse amplifier or delay unit. Feedback is recommended when the capacitor-diode-inverter is used to drive a Type 4603, particularly at high speeds. The Types 4125, 4127 and 4129 may be used to sample the outputs of Type 1213 Flip-Flops, provided the input timing conditions are met.

No interconnecting units are used when going from a standard buffered flip-flop to an unbuffered flip-flop. However, it is necessary to make sure that all levels are present for the required amount of time before a sampling pulse arrives.

APPENDIX A
BINARY-CODED DECIMAL CODES AND ARITHMETIC

INTRODUCTION

The digital computer can be thought of as an assemblage of two-state devices because it manipulates the ONES and ZEROS of the binary number system. People, on the other hand, are more accustomed to decimal numbers, and for this reason it is often desirable to build a computing system which can be operated in decimal.

To build a decimal computer with two-state devices, it is necessary to encode the decimal digits with binary bits. Four binary bits are needed. Although only ten of the sixteen permutations possible with the four-bit decade will be used, all are available. The number of codes that can be generated is calcuated as follows:

$$\frac{16!}{6!} = 2.9 \times 10^{10}.$$

The choice of a code is obviously important. Desirable features of the code are: ease in performing arithmetic operation, economy of storage space, economy of gating operations, error detection and correction, and simplicity. Several possible codes are shown below, followed by a detailed explanation of arithmetic operations using two especially convenient codes, the 8 4 2 1 and the Excess 3.

FOUR BIT CODES

The 8 4 2 1 code is commonly referred to simply as binary coded decimal because the weights of the positions are the same as in the binary number system. Arithmetic operations are easily performed using the same basic method as in binary since the number sequence is the same.

In the Excess 3 code, a decimal number D is represented by the binary equivalent of the number D + 3. The Excess 3 code is not a weighted code, but since it follows the same number sequence as binary, it is useful in arithmetic operations. Addition is facilitated since the need for a correction factor is easily detected and easily implemented. Because it is self-complementing, the Excess 3 code is also useful in subtraction.

The 2 4 2 1 is a self-complementing weighted code which is commonly employed in counting systems. Other examples of four-bit weighted codes include the 5 4 2 1, the 5 3 1 1, and the 7 4 -2 -1 code. All of these codes are shown in Figure A-1.

More than four bits may be used in each decade to provide additional special features such as the detection of errors and the simplification of decoding.

DECIMAL	8421	Excess 3	2421
0	0000	0011	0000
1	0001	0100	0001
2	0010	0101	0010
3	0011	0110	0011
4	0100	0111	0100
5	0101	1000	1011
6	0110	1001	1100
7	0111	1010	1101
8	1000	1011	1110
9	1001	1100	1111

DECIMAL	5421	5311	74−2−1
0	0000	0000	0000
1	0001	0001	0111
2	0010	0011	0110
3	0011	0100	0101
4	0100	0101	0100
5	1000	1000	1010
6	1001	1001	1001
7	1010	1011	1000
8	1011	1100	1111
9	1100	1101	1110

Figure A-1
Four-bit decimal codes

ARITHMETIC OPERATIONS WITH THE 8 4 2 1 OR EXCESS 3 CODE

Because the 8 4 2 1 and the Excess 3 codes follow the same number sequence as the binary number system, standard binary methods may be used. However, in binary notation sixteen states are represented with four bits. In binary-coded decimal only ten of these states are used; therefore, special correction factors must be added to account for the six unused states.

COUNTING

In a binary-coded decimal (BCD) counter, the corrective action is very simple. The counter is divided into four-bit decades and special gating is added to each decade. This gating detects the number 9 and reroutes the next count pulse so that it will reset the decade to 0 and generate a carry to the next decade.

In a down counter, the same approach is used. Starting with a standard binary down counter, the number 0 is detected and the next count input resets the counter to the appropriate 9 designation and produces a borrow.

A reversible BCD counter may be implemented by combining the techniques for the individual up and down counters. Such a counter, however, is more difficult to construct than a single direction counter since provision must be made for isolating the carry and borrow chains and for assuring that count up and count down signals do not occur simultaneously.

ADDITION

A common method of performing BCD addition is to add two numbers in the binary adder and, if necessary, add or subtract an appropriate correction factor (see Figure A-2). When addition is to be performed in a decade by decade fashion (serial addition with parallel decades) either code is useful. If addition is performed in parallel, however, the Excess 3 code is superior to the 8 4 2 1 code.

In 8 4 2 1 code the sum will be correct if it does not exceed 9. If the decimal sum is between 10 and 15, it is necessary to add +6 to the binary sum and generate a carry to the next decade. If the decimal sum exceeds 15, a carry signal is generated by the initial addition but the correction factor +6 must still be added to the binary sum.

Addition of 8 4 2 1 coded numbers has the disadvantage that a carry signal can be generated during the correction process. For this reason each decade in the adder has to be corrected individually. Therefore it is not a desirable code in a parallel adder (see Figure A-2).

No correction necessary
(Sum $\leq$ 9)

0100 = 4 dec.
0011 = 3 dec.
0111 = 7 dec.

Initial sum in forbidden state
(10 $\leq$ sum $\leq$ 15)

1000 = 8 dec.
0100 = 4 dec.
1100 = forbidden state
0110 = correction factor of +6
1 ← 0010 = 2 dec. plus carry

Initial sum in incorrect notation
16 $\leq$ sum $\leq$ 18)

1001 = 9 dec.
1000 = 8 dec.
1 ← 0001 = 1 plus carry
0110 = correction factor of +6
0111 = 7 dec. (plus cary from first addition)

Multiple decade addition

0101	0101	1000	= 558 dec.
0010	0100	0011	= 243 dec.
0111	1001	1011	
		+0110	
		1←0001	
	1		
	1010		= 801 dec.
	0110		
	1←0000		
1			
1000			

Figure A-2
Addition with the 8 4 2 1 code

When two Excess 3 numbers are added, the sum will contain an excess 6; if the decimal sum is 9 or less, it is necessary to subtract 3 in order to return to Excess 3 notation; if the decimal sum is greater than 9, the excess 6 contained in the sum cancels the effect of the six unused binary states, but it is necessary to add 3 to return to the Excess 3 notation.

Whether the correction factor is +3 or −3 is determined by whether or not a carry signal appears during the initial addition. An initial carry requires a positive correction; no carry, a negative correction. The correction process will never yield an additional carry, thus simultaneous correction of all decades is possible.

The steps for performing Excess 3 addition are:

1. Add the two BCD numbers in binary fashion
2. Check each decade for a carry signal
3. Subtract 3 from each decade in which a carry has not occurred, while simultaneously adding 3 to each decade in which the carry signal has occurred.

The +3 correction is made by adding 0011 to the appropriate decade. Subtracting 3 from a decade is done by adding 1100 and using the end around carry from the most significant bit of the decade. This is a method of 9's complement subtraction, described under subtraction below.

Sum ≤ 9

```
 0111 = 4 dec.
 0110 = 3 dec.
 1101 = uncorrected sum
-0011 = correction factor of −3
 1010 = 7 dec.
```

Sum ≥ 10

```
      1011 = 8 dec.
      0111 = 4 dec.
1 ←   0010 = uncorrected sum
      0011 = correction factor of +3
      0101 = 2 dec., plus carry from
             initial addition
```

Multiple Decade Addition

```
 1000        1000        1011  =   558 dec.
 0101        0111        0110  =   243 dec.

 1110 ←      0000 ←      0001
-0011       +0011       +0011
 1011        0011        0100  =   801 dec.
```

Figure A-3
Addition with the Excess 3 code

SUBTRACTION

Since subtraction is the inverse of addition, the same circuitry is used for both operations. Subtraction by this process is known as the system of adding complements. The 9's complement of any number is that number which is obtained by subtracting each individual digit from 9. With a self-complementing BCD code, such as Excess 3, the 9's complement of any number can be easily obtained by changing all ZEROS to ONES and all ONES to ZEROS. Figure A-4 illustrates Excess 3 code with 9's complement notation.

DECIMAL	EQUIVALENT CODE		
	sign	tens decade	ones decade
+99	0	1100	1100
+98	0	1100	1011
+10	0	0100	0011
+3	0	0011	0110
+2	0	0011	0101
+1	0	0011	0100
+0	0	0011	0011
−0	1	1100	1100
−1	1	1100	1011
−2	1	1100	1010
−3	1	1100	1001
−10	1	1011	1100
−98	1	0011	0100
−99	1	0011	0011

Figure A-4
NINE'S complement, Excess 3 code

To subtract with Excess 3, 9's complement code, the subtrahend is first complemented then added to the minuend. During the first step of the addition process the individual binary bits (in the decimal decades and in the sign bits) are added just as in binary. Carries propagate from each digit to the digit of more significance and from the most significant digit to the sign bit. If the sign bit produces a carry, it is added to the least significant decade, a process known as end around carry.

After this initial portion of the subtraction, a correction factor must be applied just as in addition. That is, a binary 3 (0011) must be added to each decade in which a carry signal has occurred and binary 3 must be subtracted from each decade in which a carry signal did not occur.

Subtraction of the correction factor may be performed in the same way as well as the overall subtraction. However, the subtraction in this case operates only on the individual digits. Thus, if a carry occurs from the most significant bit of the digit, it is not carried out to the next digit; rather, it is added into the least significant bit of the same digit.

0	1000	0100	51 dec.	+51 dec.
1	1001	1000	(complement of 34 dec.)	−34 dec.
0	0001	1100		
		1	end around carry	
0	0001	1101		
	0011	1100	correction factor	
	0100	1001		
		1	end around carry	
0	0100	1010	17 dec.	+17 dec.

0	0110	0111	34 dec.	+34 dec.
1	0111	1011	(complement of 51 dec.)	−51 dec.
1	1110	0010		
	1100	0011	correction factor	
	1010	0101		
	1		end around carry	
1	1011	0101	−17 dec.	−17 dec.

Figure A-5
Subtraction with the Excess 3 code, 9's complement notation

A second method of performing subtraction is through the use of the 10's complement notation. The 10's complement of any number may be obtained by adding 1 to the 9's complement. Operations are similar to those used in the 9's complement notation except that the end around carry is not required. Hence this is useful in systems where a feed back loop would be particularly time consuming.

CODES GREATER THAN FOUR BITS

Codes greater than four bits are often used for error detection and simplicity in decoding (Figure A-6). The biquinary code is commonly used when error detection is required. It is a seven-bit weighted code in which two ONEs and five ZEROs appear in the representation of any number, thus it is always possible to detect single errors, and it is often possible to detect multiple errors.

A ten-bit weighted code allows any number to be represented with a single ONE and nine ZEROs. This code is often used in counting operations; the counter is a 10-stage shift register with the final stage connected to the initial stage. This counter, often given the name of ring counter, requires no carrying propagate time and the numbers may be decoded into ten lines without additional gates.

The switched tail ring counter is a five stage ring counter with **reversed** feedback from the initial stage to the final stage. It is considerably more economical to build than the ring counter and has the advantage that no carry propagate time is required. Any state may be decoded by investigating only two flip-flops.

DECIMAL	BIQUINARY							RING COUNTER CODE										
	5,	0,	4,	3,	2,	1,	0	9,	8,	7,	6,	5,	4,	3,	2,	1,	0
0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
2	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
3	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
4	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
5	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
6	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
7	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
8	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
9	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DECIMAL	SWITCH TAIL RING COUNTER CODE					DECODING	
	A	B	C	D	E		
0	0	0	0	0	0	A	E
1	0	0	0	0	1	D	E
2	0	0	0	1	1	C	D
3	0	0	1	1	1	B	C
4	0	1	1	1	1	A	B
5	1	1	1	1	1	A	E
6	1	1	1	1	0	D	E
7	1	1	1	0	0	C	D
8	1	1	0	0	0	B	C
9	1	0	0	0	0	A	B

Figure A-6
Codes greater than four bits

APPENDIX B
BOOLEAN ALGEBRA

Note: As mentioned in the Introduction, a knowledge of Boolean algebra is not a prerequisite to the performance of logic design with DEC Modules. However, Laboratory Modules and System Modules can be used to implement Boolean equations quickly and easily.

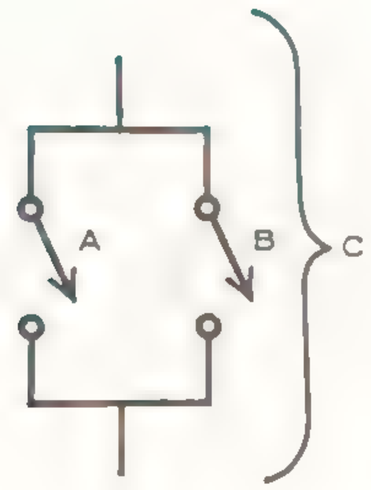
Boolean algebra was introduced in 1847 by an English mathematician, George Boole. The purpose of the algebra was to find a shorthand notation for the system of logic originally set forth by Aristotle. Aristotle's system dealt with statements which were considered to be either true or false, but never partially true or false. Boole's algebra was based on a single valued function with two discrete possible states.

Boolean algebra lay almost dormant until recent times. Today, however, it is gaining widespread recognition as an efficient method for handling any single valued function with only two possible states. When it is applied to binary arithmetic, the two states are ZERO and ONE. When discussing a switch, the two values are OPEN and CLOSED.

Figure B1

The convention used will be that the OPEN state corresponds to the ZERO state while the CLOSED state corresponds to the ONE state.

OR FUNCTION



A + B = C
0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1

Figure B2

If two switches, A and B, are connected in parallel to form a gate, inspection shows that the gate can only transmit information if A or B or both are in the transmitting state, i.e., CLOSED. This is written in equation form as

$$A + B = C$$

(A or B equals C)

Figure B2 shows the parallel combination of two switches along with a table giving the value of C for all possible values of A and B.

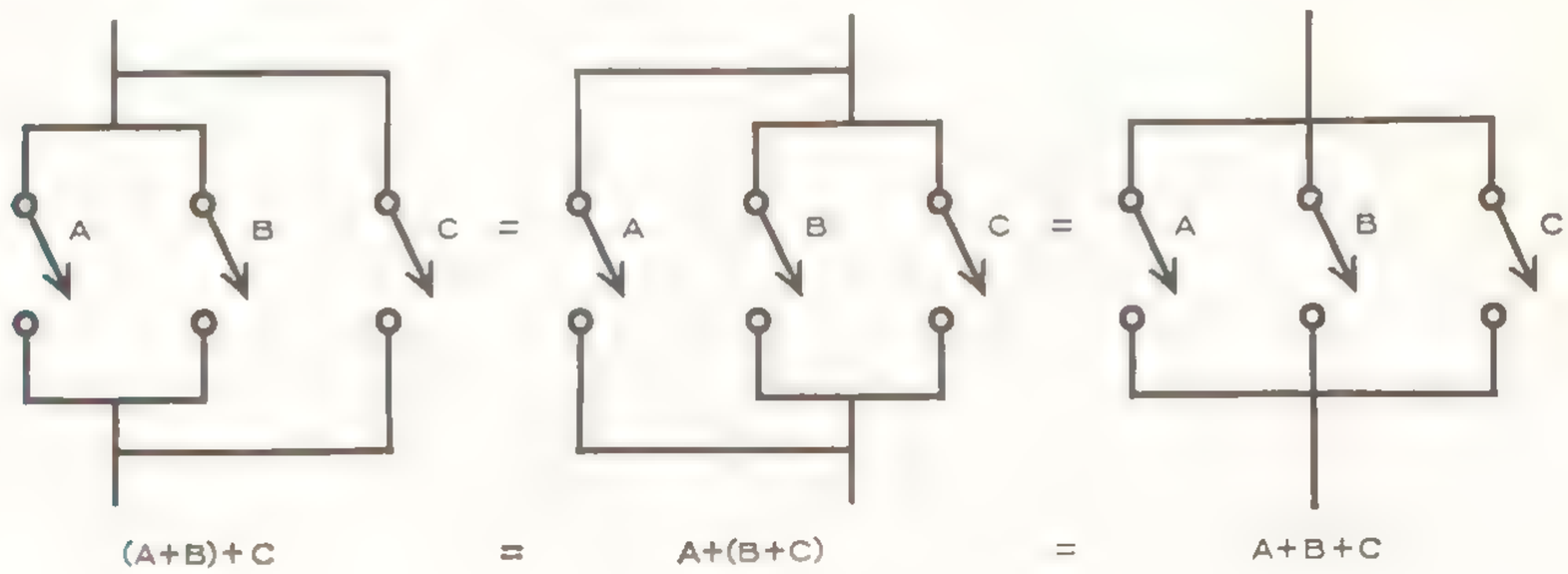


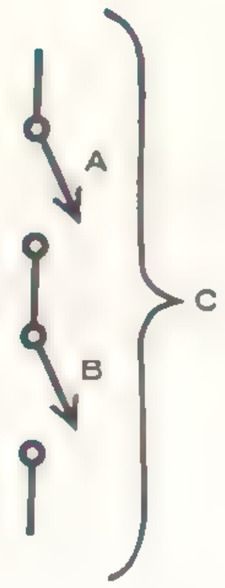
Figure B3

By adding a third gate in parallel, as in Figure B3, it becomes obvious how the OR function may be extended to any number of variables. This figure also serves to illustrate that the communicative and associative laws are valid for the OR function, i.e.,

$$A + B = B + A$$

$$(A + B) + C \equiv A + (B + C) \equiv A + B + C$$

AND FUNCTION



A	B	=	C
0	0	=	0
0	1	=	0
1	0	=	0
1	1	=	1

Figure B4

If two or more gates are placed in series, the result is known as an AND gate. Inspection of the arrangement in Figure B4 shows that the resulting gate will transmit only if both A and B are CLOSED, i.e., equal to ONE. The equivalent equation in Boolean form is

$$AB = C$$

(A and B equal C)

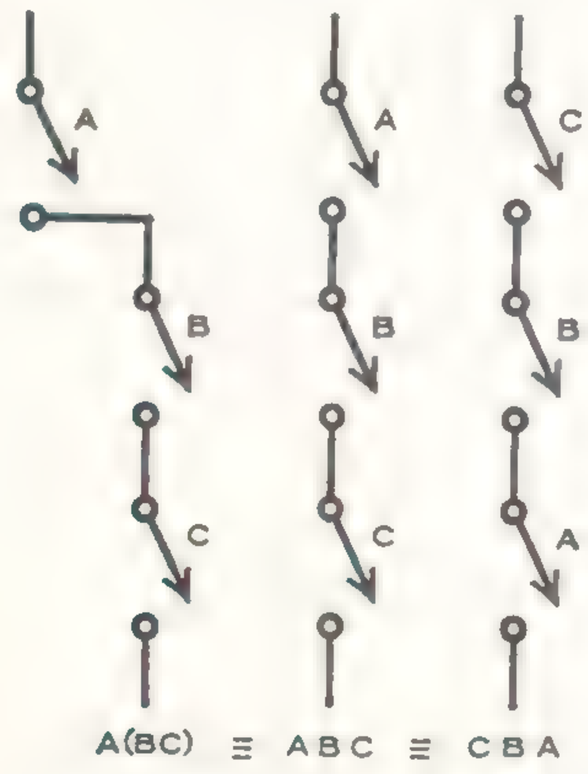


Figure B5

Figure B5 demonstrates how the AND function is applied to more than one variable. The commutative and associative laws also hold.

$$AB = BA$$

$$A(BC) \equiv (AB)C \equiv ABC$$

IDENTITIES

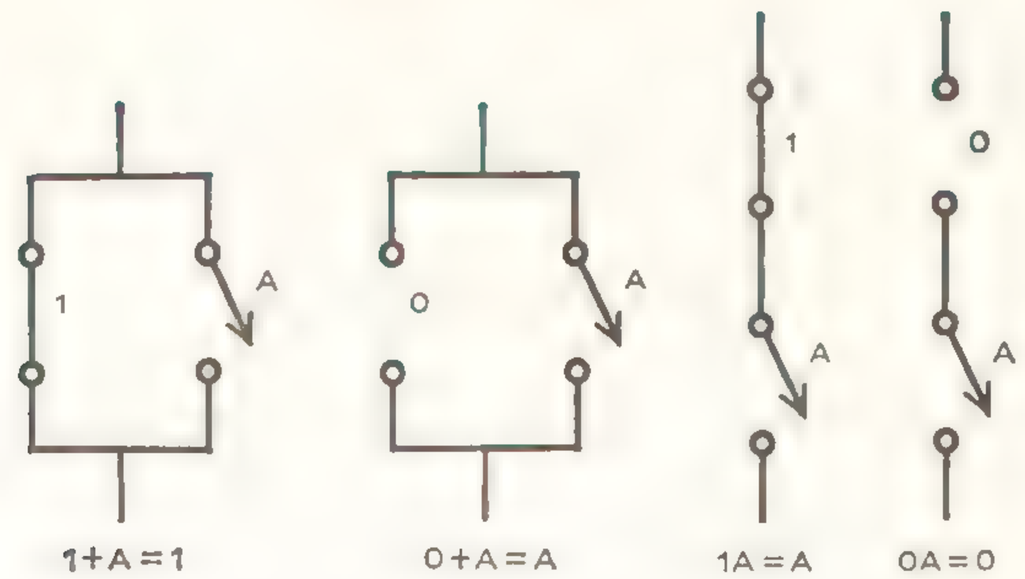


Figure B6

To enable the simplification of Boolean functions, there are many identities which are helpful. In Figure B6, the combination of switches and corresponding equations demonstrate these identities.

COMPLEMENT

If two gates are connected so that the same signal will open both of them or close both of them simultaneously, then the switches are given the same symbol. If two gates are connected so that a single signal will open one gate while closing the other gate, and vice versa, then these gates are said to be the complement of each other. Thus, if one gate is labeled A, the other gate will be labeled A (read "not A").

An entire function may also be complemented. For example,

if $C = A(B + C)$

then $C = \overline{A(B + C)}$

The use of one label for more than one gate makes the following identities helpful:

$$A + A = A \qquad A + \overline{A} = 1 \qquad \overline{\overline{A}} = A$$

$$AA = A \qquad A\overline{A} = 0$$

DE MORGAN'S LAWS

Two unique laws which can be applied only to Boolean algebra are known as De Morgan's laws.

$$\overline{A + B + C + \ldots + N} = \overline{A}\,\overline{B}\,\overline{C} \ldots \overline{N}$$

$$\overline{A\,B\,C \ldots N} = \overline{A} + \overline{B} + \overline{C} + \ldots + \overline{N}$$

These laws may be verified by constructing a table of various possible values.

BOOLEAN ALGEBRA FOR USE WITH VOLTAGE LEVELS

Since DEC voltage levels have only two possible values, Boolean algebra can also be useful in the study of these levels.

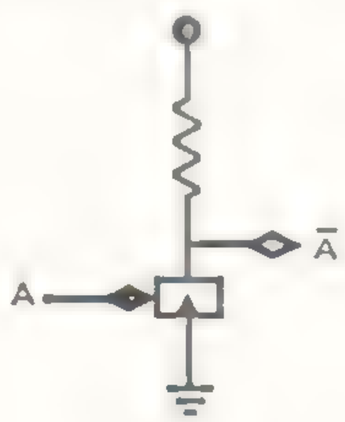


Figure B7

The basic unit of DEC Logic is the transistor inverter. The simplest use of the inverter is to perform a complement. If the emitter is at ground and a signal is applied to the base, the resulting output is the complement of the base input.

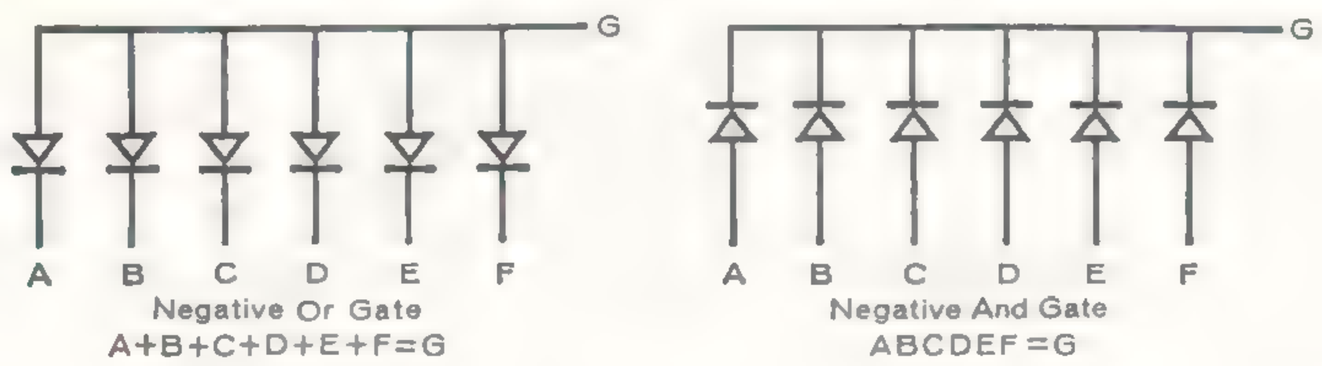


Figure B8

A simple OR gate is formed by means of diodes, as shown in Figure B8. If A or B or C or D or E or F or any combination of these is negative, the resulting output is negative.

A similar unit with the diodes reversed will form an AND gate. Only if A and B and C and D and E and F are negative will the resulting output be negative.

Inspection of these diode units shows that the AND and OR gates will be interchanged if the levels are defined in the opposite manner. That is, if ground is defined as a ONE and negative is defined as a ZERO. This is a demonstration of De Morgan's law.

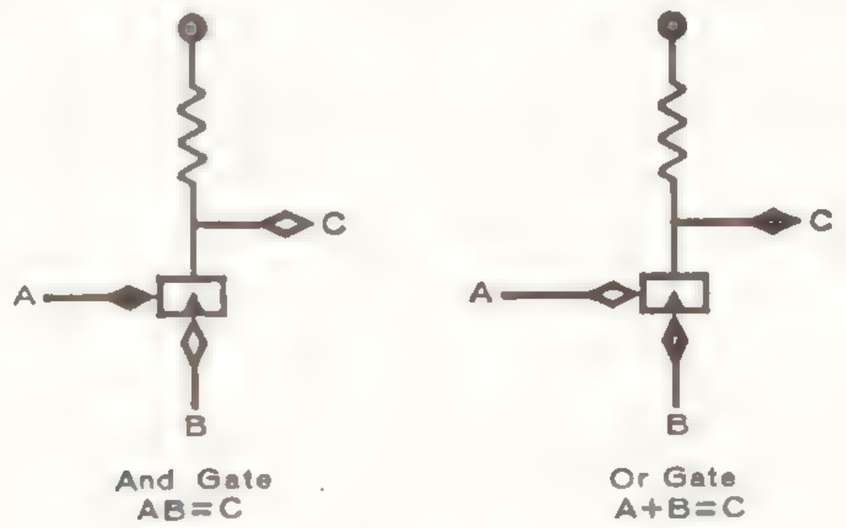


Figure B9

If the signals are manipulated without the encumbrance of a permanent sign convention, the same gate may perform many functions. Figure B9 shows an inverter which serves as an AND gate if the following definitions are used: A = 1 if negative, B = 1 if ground, C = 1 if ground. The same transistor can be used as an OR gate if the opposite definitions are made, i.e.: A = 1 if ground, B = 1 if negative, and C = 1 if negative.

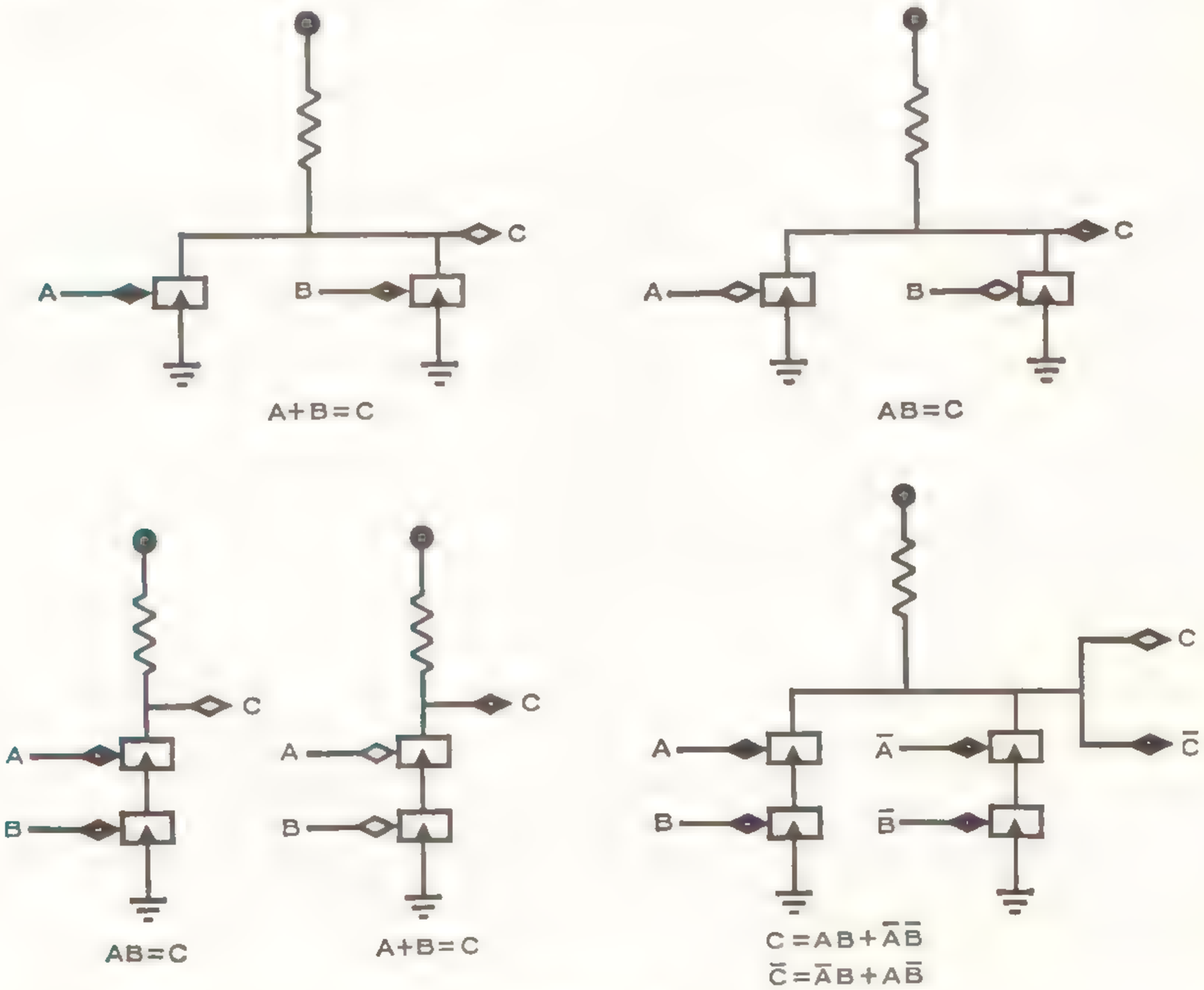


Figure B10

For this reason, DEC uses the sign convention that the diamond arrowheads on signals indicate the required polarity for the desired action. A solid diamond denotes a −3 volt level for assertion, while a hollow diamond denotes a ground level for assertion. By using this method, it is possible to combine amplification and gating without added inversions as would otherwise be necessary. Several illustrations are shown in Figure B10.

APPENDIX C

PULSE TRAIN TECHNIQUES

Pulse train techniques (also known as operational digital techniques) utilize digital components in a manner similar to that used in analog computation. Functional blocks perform specific operations such as addition, subtraction, etc. These blocks are cascaded to allow simultaneous operation of all blocks and a continuous (on-line) output. Such techniques are particularly useful in control systems where continuous inputs are required.

In operational digital systems, data is represented by unitary weighted pulse trains; each pulse represents one unit. These pulse trains may come into a system from an outside source, such as a shaft rotation encoder, or may be generated in the system by a variety of simple methods. For example, the pulse train may be generated from a binary number by transferring the number to a down counter and counting down until the number reaches zero.

If the input signifies a level with a duration proportional to the quantity of the input, a level-to-pulse synchronizer may be used to generate the desired pulse train. Such a synchronizer is shown in Figure C-1. When the input level is at a negative voltage, the flip-flop will be set and the clock pulses will be gated through the output pulse amplifier. When the input level goes positive, the flip-flop will be cleared and output pulses will not be produced.

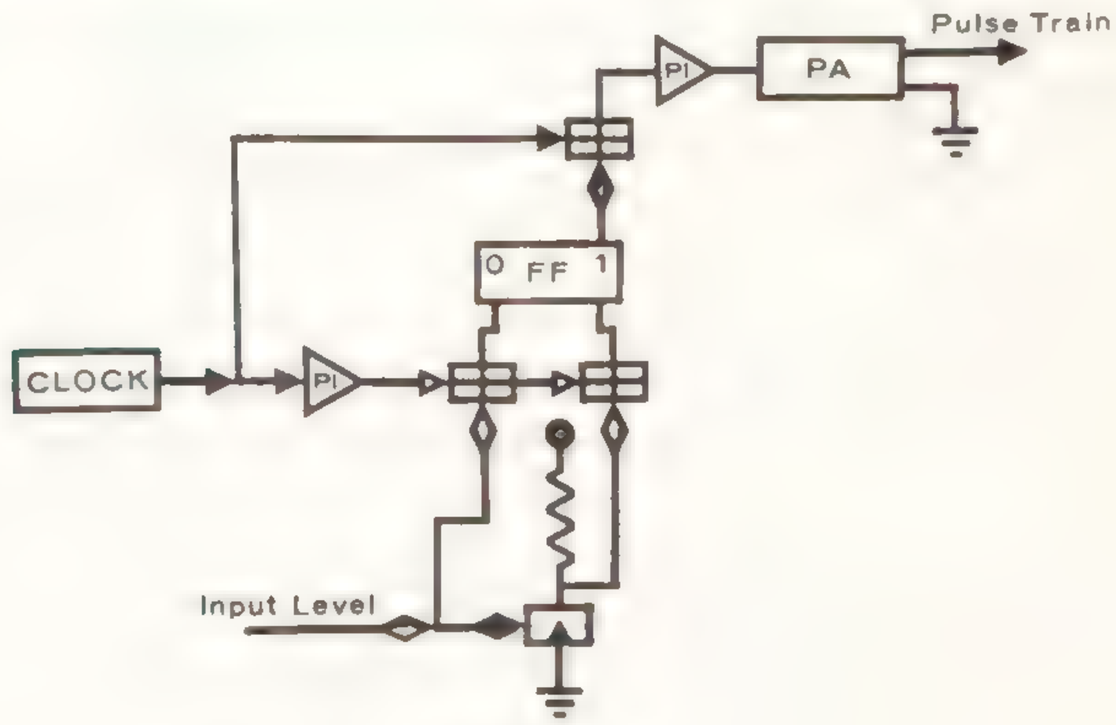


Figure C-1

Level-to-pulse generator and synchronizer. Circuit uses DEC Flip-Flop Type 4214, Pulse Amplifier Type 4604, Positive Capacitor-Diode Gates Type 4128, Negative Capacitor-Diode Gates Type 4127.

ADDITION, SUBTRACTION

Once the pulse train is generated, arithmetic operations can be performed quite easily. Addition may be performed simply by ORing together two pulse trains. Care should be taken, of course, that successive pulses do not overlap or occur too closely together for the circuitry to handle.

Figure C-2 illustrates an adder for two synchronous pulse trains. Pulse train A drives the pulse amplifier directly. Pulse train B drives a delay unit. At the end of the specified delay time, the pulse output of the delay will generate a second output pulse.

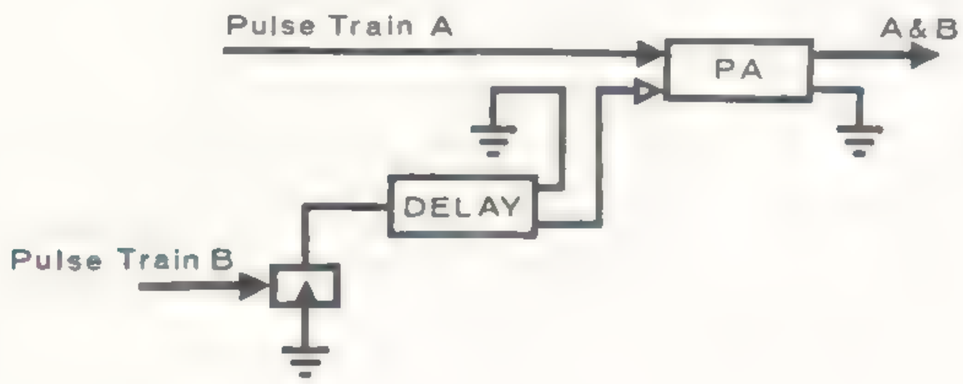


Figure C-2

Adder for synchronous pulses. Circuit uses DEC Pulse Amplifier Type 4604 and Integrating Delay Type 4301.

An operational digital subtractor is an up-down counter. The pulse train representing the minuend is applied to the count-up terminal, the pulse train of the subtrahend to the count down terminal. As in the adder, provisions must be made to assure that the counter does not receive count-up and count-down pulses simultaneously.

A subtractor designed to accept synchronous pulses is shown in Figure C-3. The "Count up" and "Count down" pulses set the appropriate control flip-flops and also trigger a delay unit. The control flip-flops are gated together so that a pulse occurring on the up line, but not on the down line, will enable the count-up control line; a count-down signal, but no count-up signal, will enable the count-down control line. If no pulses are received, or if pulses are received on both input lines, neither of the control lines will be enabled. After the control lines have sufficient time to set up, delay 1 will produce a count pulse. When the carry (or borrow) has had sufficient time to propagate to the end of the counter, the control flip-flops may be reset so that new count-up and count-down signals can be received.

For addition and subtraction, pulse trains must be synchronous, preferably by synchronizing all inputs to a master clock signal. Typical synchronizer circuits are illustrated starting on page 35 above.

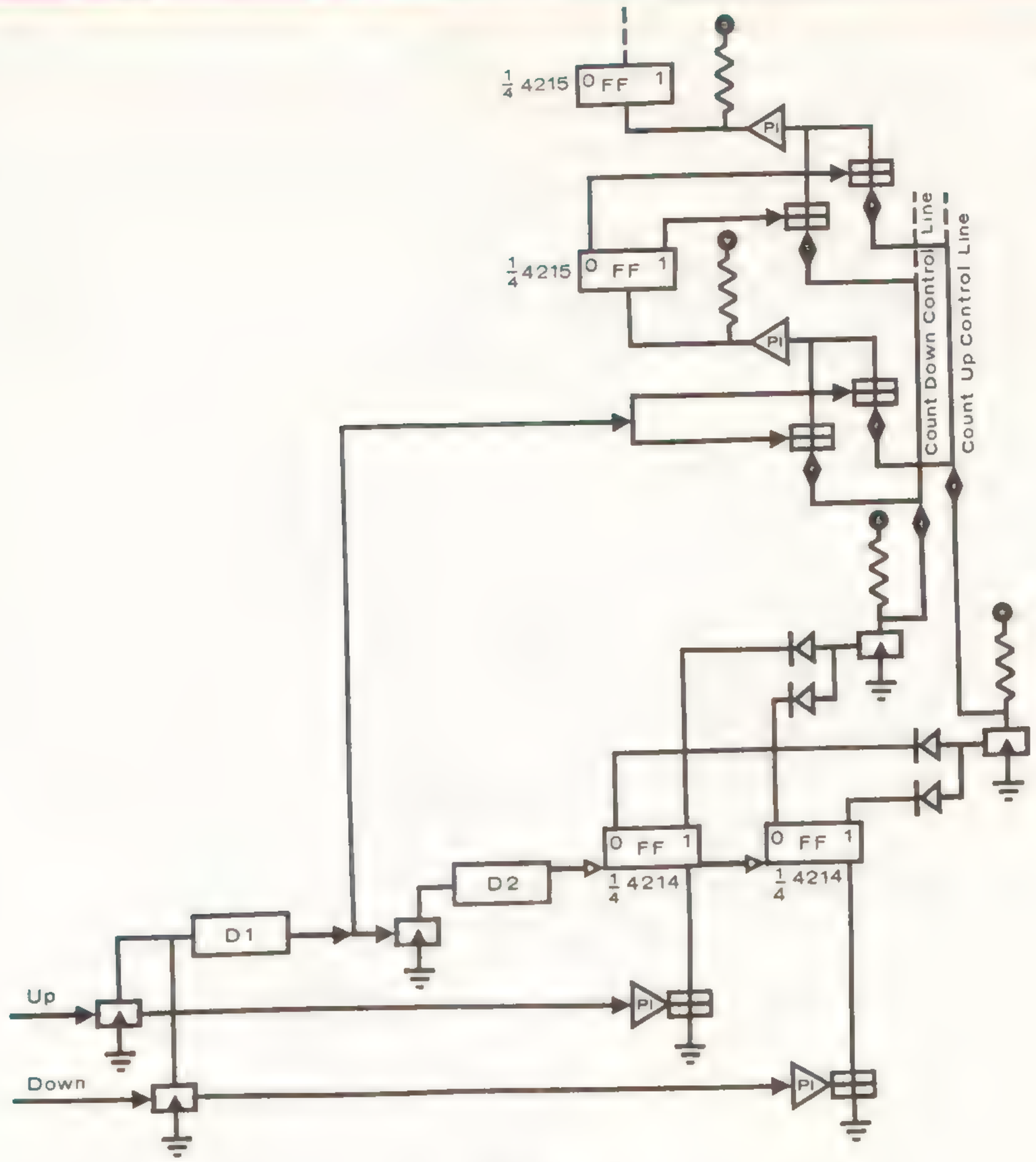


Figure C-3

Subtractor for synchronous pulses. Circuit uses DEC Counter Flip-Flops Type 4215 and Buffer Flip-Flops Type 4214.

SCALING, DIVISION

The pulse trains may be scaled with a special counter; i.e., one which will produce an output signal every time the desired number of input pulses have occurred. If the desired scale factor is an integral power of 2, the output is automatically produced by the final digit of a counter of appropriate length. If N is not a power of 2, gating must be performed to detect the desired number, generate an output signal, and reset the counter to 0.

The division of a pulse train by a binary number is similar to scaling. In this case the divisor is determined by a binary number stored in a buffer register. A circuit for implementing this is shown in Figure C-4. The 0 output of each bit in the counter is applied to a 2-input positive OR gate. The other input to

each of these OR gates is controlled from the 1 output of the corresponding bit in the buffer register. Thus, if any buffer flip-flop holds a 0, the corresponding OR gate is permanently enabled. If a buffer flip-flop holds a 1, the corresponding OR gate is enabled only when the corresponding flip-flop is in the 1 state. Thus, when the counter has 1s in all positions where the buffer register has 1s, all of the OR gates will be enabled. By ANDing together the outputs of the OR gates, it is possible to determine when the desired state has been reached. This signal releases the inhibit input on the control flip-flop so that the next input pulse will clear the flip-flop register, and generate an output signal.

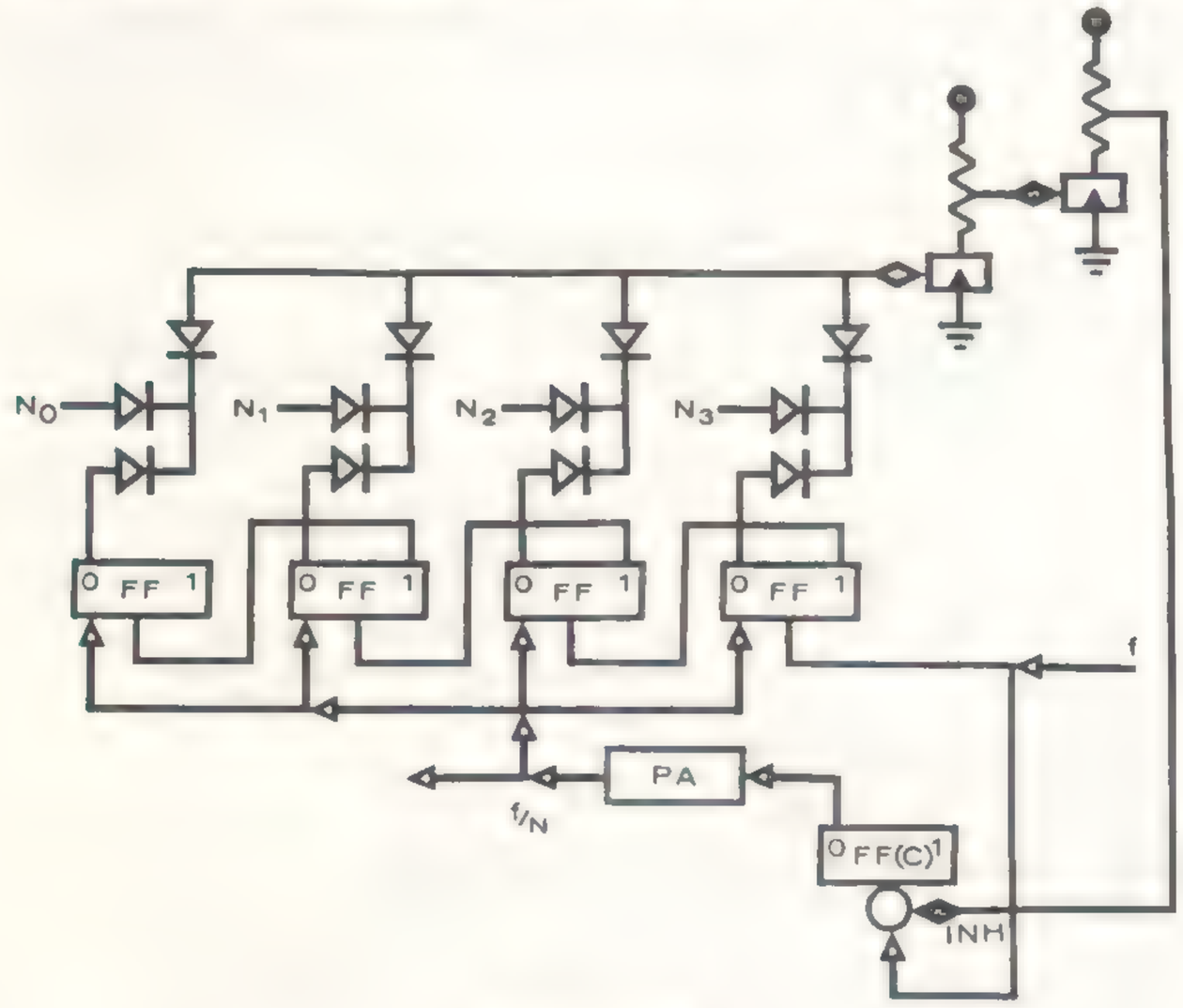


Figure C-4

Binary rate divider. Circuit uses DEC Flip-Flops Type 4215, Diode Gate Type 4139, and Pulse Amplifier Type 4604.

MULTIPLICATION

Binary rate multiplication is a method for multiplying a pulse train by a binary number. This method can best be illustrated by assuming that the input pulse train is unitary weighted and the binary number is less than 1. The pulse train enters a pulse distributor which sends one half of the pulses out the first line, one fourth of the pulses out the second line, one eighth of the pulses out the third line, etc. The binary multiplier is held in a storage register. The most significant bit of the storage register (which has a weight of one half) is ANDed with the first output line from the pulse distributor. The next most significant bit of the storage register is ANDed with the second line from the pulse distributor and so forth.

Assume that the number in the storage register is one half or, in binary, .10000. This would allow pulses only on the first line of the pulse distributor to be gated

onto the output line. Thus, the output pulse train would contain half as many pulses as the input pulse train. If the desired multiplier is one fourth (binary .01000) only those pulses on the second line of the pulse distributor would be gated onto the output line. If the multiplier is three fourths (binary .11000) pulses on both the first and the second lines of the distributor would be gated onto the output line.

This multiplication technique need not be restricted to unitary weighted pulse trains or binary numbers between 0 and 1; however, pulses yielded in the product pulse train may not be unitary weighted. The weighting of the output pulses is equal to two times the weighting of the input pulses times the weighting of the bit which is ANDed with the first output line of the pulse distributor. For example, if the input pulse train is unitary weighted and the most significant bit of the storage register represents the weight of 1, the output pulses will be weighted as two counts each.

A method for constructing a binary rate multiplier is shown in Figure C-5. The pulse distributor is built in the same manner as an ordinary counter with carries propagating whenever a 1 to 0 flip-flop transition occurs. When a 0 to 1 flip-flop transition occurs in the counter, an input will occur at the corresponding capacitor diode gate of the multiplier. If the level input of this diode gate is a logical 1, an output pulse will be generated.

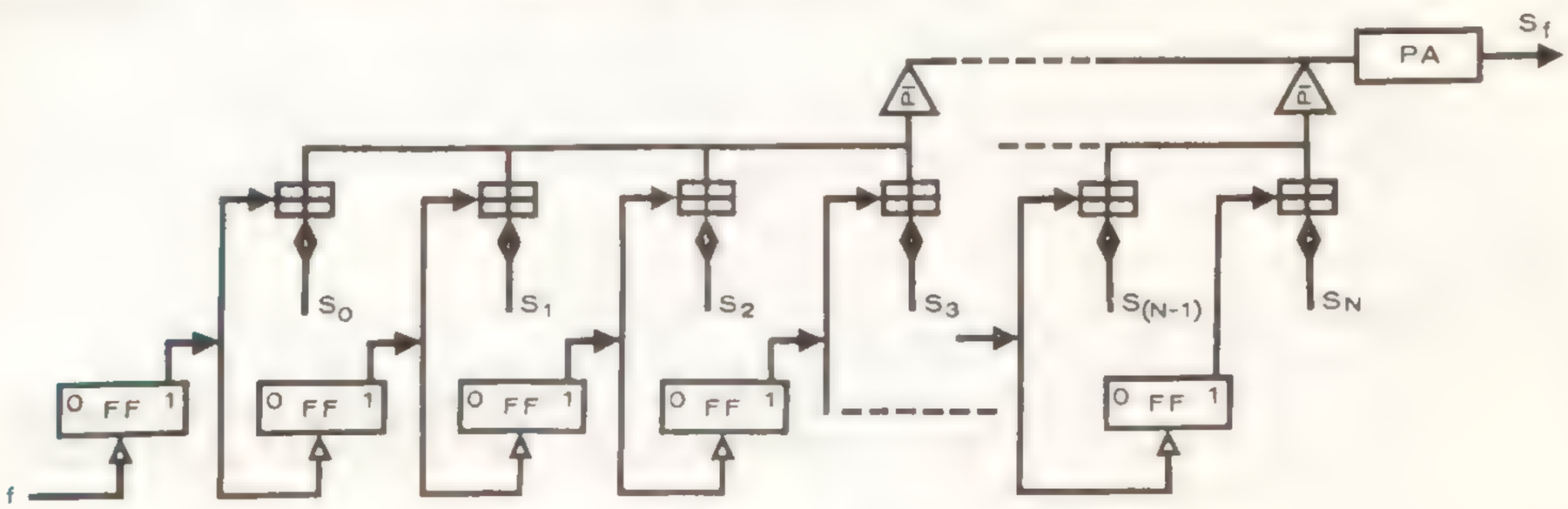


Figure C-5
Binary rate multiplier. Circuit uses DEC Flip-Flops Type 4215, Pulse Amplifier Type 4604, Capacitor-Diode Gates Type 4129.

OTHER OPERATIONS

Operational digital techniques may also be used for finding square roots, integrals, derivatives, logarithms, and exponentials. An excellent discussion of the methods involved and the accuracy of the methods can be found in Chapter 29 of Volume II of the Handbook of Automation, Computation, and Control, edited by Eugene Grabbe, Simon Ramo, and Dean E. Wooldridge and published by John Wiley and Sons, Inc.

APPENDIX D
BIBLIOGRAPHY OF DIGITAL LOGIC

INTRODUCTORY BOOKS

A large number of books are currently becoming available on the principles of digital computers and digital logic. The following four are particularly well written and concise. They are on a level which would be suitable for an undergraduate course, an industrial training course, or for self-study. Only a knowledge of algebra, trigonometry and basic electronics is assumed.

Siegel, Paul, Understanding Digital Computers
New York: John Wiley & Sons, Inc., 1961.

Discusses logic and arithmetic, components and circuits used in logical building blocks, and the functional units of the digital computer.

Bartee, Thomas C., Digital Computer Fundamentals
New York: McGraw-Hill, 1960.

Includes a discussion of computer operations, programming, number systems, basic logical circuits and logical design, and the functional elements of a general purpose computer.

Irwin, Wayne C., Digital Computer Principles
Princeton, New Jersey: D. Van Nostrand Company, 1960.

Puts slightly more emphasis on logic and less on circuitry. It includes a discussion of number systems, a brief discussion of the circuitry, timing, and digital arithmetic, as well as Venn diagrams, Karnaugh maps, and Harvard minimizing chart.

Smith, Charles V. L., Electronic Digital Computers
New York: McGraw-Hill, 1959.

Discusses digital computer arithmetic, instruction codes, basic logic circuits and functional elements of computers. It includes a variety of specific examples, principally from the parallel direct-coupled asynchronous machine developed at the Institute for Advanced Study at Aberdeen Proving Ground.

LOGICAL DESIGN

Humphrey, Watts S., Jr., Switching Circuits
New York: McGraw-Hill, 1958.

This is a more advanced text, intended both as a graduate engineering text and as an aid to the practicing design engineer. It presents a more mathematical treatment of the subject than the previously mentioned books. The introduction describes number systems, binary numbers and basic computer circuits. A more detailed treatment is given to Boolean algebra, relay networks, codes, minimization aids, logic matrices, bi-lateral networks, cascaded networks and sequential circuits.

REFERENCE WORKS

Grabbe, Ramo and Wooldridge (editors)
Handbook of Automation, Computation and Control
New York: John Wiley & Sons, 1959.

This three volume series is invaluable as a reference source. Each section is prepared by specialists in the field and contains considerable background information, as well as a discussion of the theory, analysis and applications:

Volume 1 — **Control Fundamentals.** Emphasizes mathematics including sets and relations, Boolean algebra, probability and statistics, as well as numerical analysis, operations research and information theory. It also summarizes the present status of feedback control theory.

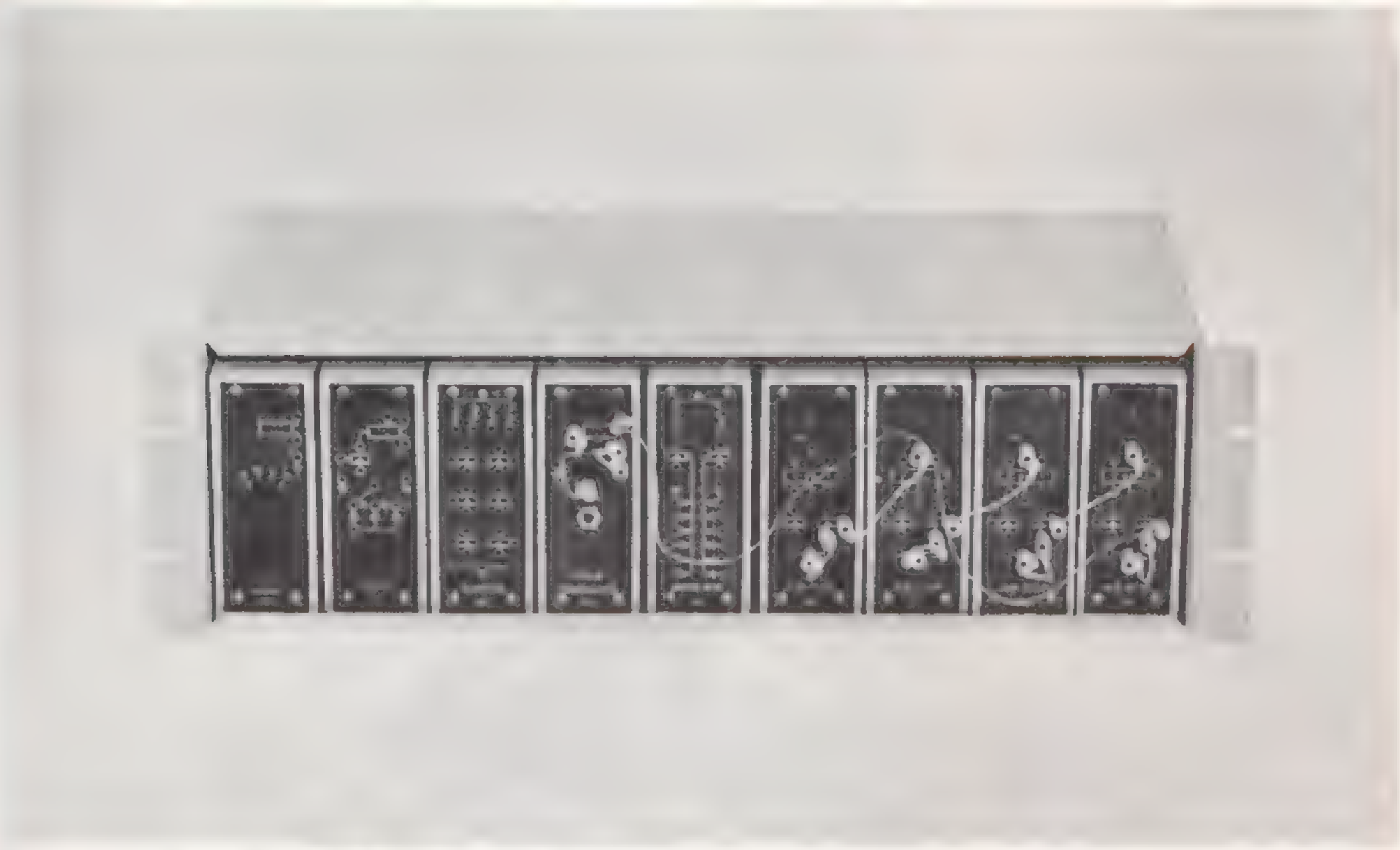
Volume 2 — **Computers and Data Processing.** Discusses computer terminology, digital computer programming, the design and use of digital computers, data processors, analog computers, and unusual computer systems. Included in this is a discussion of digital computer circuits, logical design, and techniques for reliability. The final chapter on unusual computer systems discusses the digital differential amplifier as well as pulse rate techniques.

Volume 3 — **Systems and Components.** Includes systems engineering, manufacturing process control, chemical process control, and industrial control. The component section treats selection, mathematical description and integration of components into systems. Magnetic amplifiers, semiconductors and gyroscopes are included in this section.

digital

100 SERIES
LABORATORY MODULES
5 MEGACYCLES

SERIES CHARACTERISTICS



Laboratory Modules feature graphic front panels and patch cord logic interconnections

DEC 100 Series Laboratory Modules are a coordinated set of solid state digital circuits operating at frequencies up to 5 megacycles. They are packaged in sturdy aluminum cases, measuring 1¾ x 4½ x 7 inches with graphic front panels which illustrate the logical function of each module. All logical interconnections are made on the front panels with miniature stacking banana jack patch cords. Power connections are made automatically when the modules are inserted in the Type 901 Laboratory Module Mounting Panel.

This unique method of packaging and special built-in safety features make these high quality circuits ideal for test equipment and laboratory use. Logical signals are in the range of 0 to −3 volts, which permits logical experimentation without the risk of damage to the circuitry. By following simple, well-defined loading rules, the user can quickly and easily duplicate existing systems for test or instruction purposes or implement new and unusual systems designs. The modules may be assembled and reassembled in countless combinations to meet any type of test or design requirement.

A particular advantage of all Digital Modules is their complete compatibility across speed lines. The 100 Series units are mechanically and electrically compatible with the 3000 and 5000 Series Laboratory Modules, and they are electrically compatible with the 1000, 4000 and 6000 Series System Modules. Thus systems capabilities may be readily extended, if desired, by incorporating suitable units from other lines.

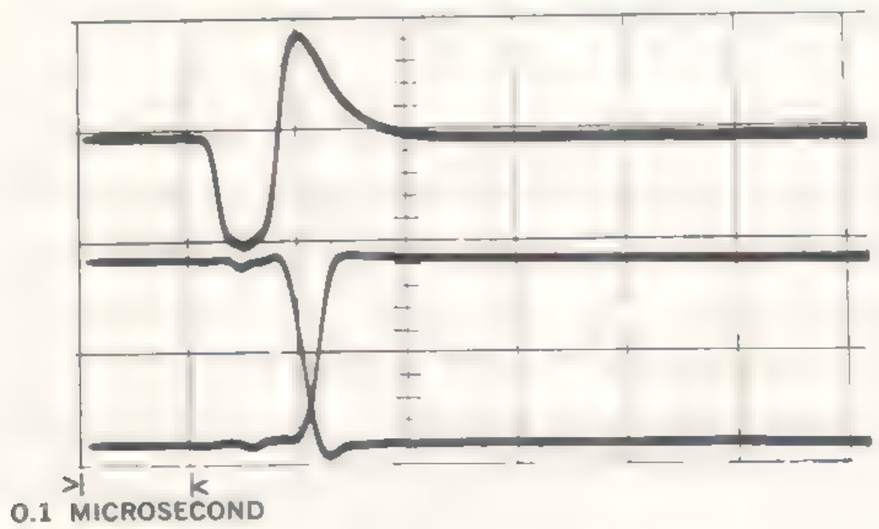
The logic employed in all DEC Laboratory Modules, as described in the Introduction, uses static flip-flops with level logic and pulse sampling. The flip-flop outputs are buffered and include a built-in delay which permits the flip-flops to be pulse-sampled while being changed. Logic gating is performed with DEC saturating transistor inverters and multiple input diode circuits internally connected to transistor inverters for signal amplification. This method of transistor gating and pulse sampling allows the construction of systems with a minimum of concern over wiring techniques and lead lengths.

The basic selection of logic modules in the 100 Series includes a six-inverter package for logical gating, a negative diode NOR, a general purpose flip-flop with buffered level outputs and built-in carry pulse output, a delay one-shot with built-in pulse amplifier, both variable frequency and stable crystal clocks, and a dual pulse amplifier package for logical gating and standardization of input pulses.

Six input-output devices are included in the Series to provide compatibility between Digital Modules and external devices. The Type 410 Pulse Generator is used to produce DEC Standard Pulses from external signals or by manual control. The Type 501 Level Standardizer allows a variety of different levels to be converted to DEC Levels. Special output devices are the Type 652 Tube Pulser, Types 667 and 668 Level Amplifiers, and Type 801 Relay.

DEC Standard Levels, used in all Digital Modules for performing logical gating functions, are 0 and −3 volts. DEC Standard Negative Pulses, used for sampling logic levels, are 2.5 volts in amplitude. The pulse width, which is commensurate with the speed line, is 70 nanoseconds in the 100 Series. Other pulses may be used if they meet the requirements described in the Type 602 Pulse Amplifier catalog sheet.

DEC STANDARD 70 NANOSECOND NEGATIVE PULSE

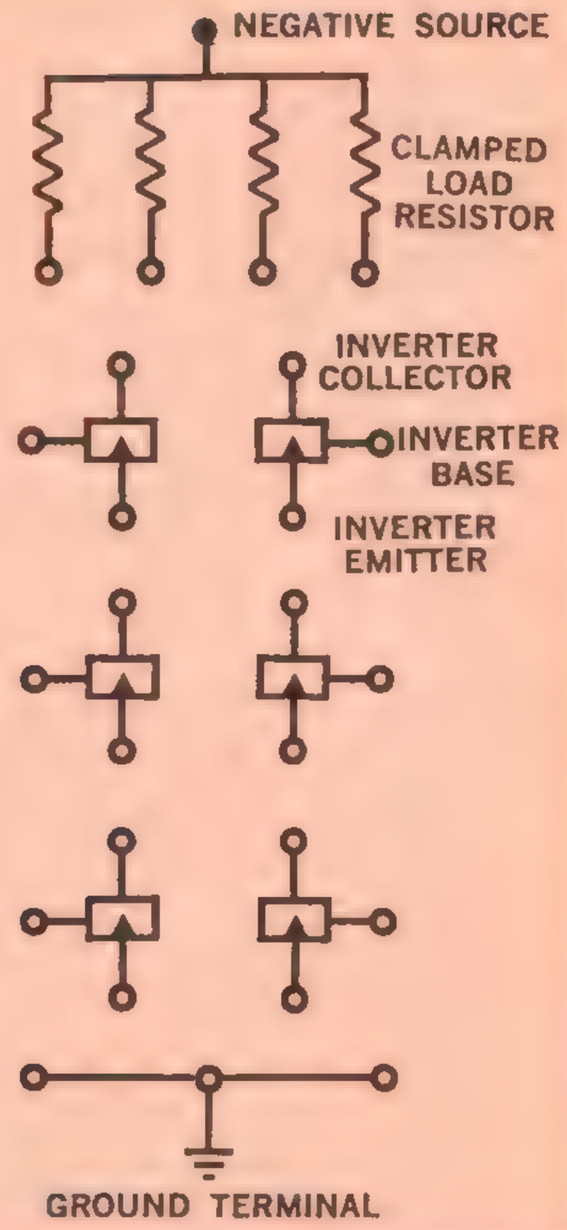


DEC TYPE 201 FLIP-FLOP OUTPUT

digital

100 SERIES
LABORATORY MODULES
5 MEGACYCLES

103
SIX INVERTERS



Type 103 contains six transistor inverters for use as pulse gates or level gates, and four load resistors clamped to −3 volts. Delay through an inverter is approximately 20 nanoseconds. Each inverter is analogous to a switch. If −3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base is brought to ground, the emitter-collector path is open.

INPUT: Base — When the inverter is used as a pulse gate, the base is driven by DEC Standard 70 nanosecond Negative Pulse, at any frequency up to 5 megacycles (1 unit of Pulse Load). When the inverter is used as a level gate, the input is driven by DEC Standard Levels or equivalent (1 unit of Base Load).
Emitter — The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitted Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem) and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.
A collector with no clamped load resistor can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: −15 volts/40 ma; −3 volts/36 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

INVERTER USAGE

DEC Transistor Inverters serve two functions. When used as level gates, they are placed in series and parallel configurations to perform logic. When used as pulse gates, the inverter will sample the logic performed by the level gates and read the results into a flip-flop or other active element.

When used as a pulse gate, an inverter will drive one and only one pulsed unit. Inverters serving as level gates are usually considered as simple switches when designing logical networks, but because they are not ideal switches, there are certain limitations which have to be taken into account. The voltage drop across saturated inverters is not zero; it is closer to 0.1 volt. As a result, inverters cannot be stacked indefinitely. Three inverters is the maximum which can be put in series if the output is to drive another inverter, as in Figure 1.

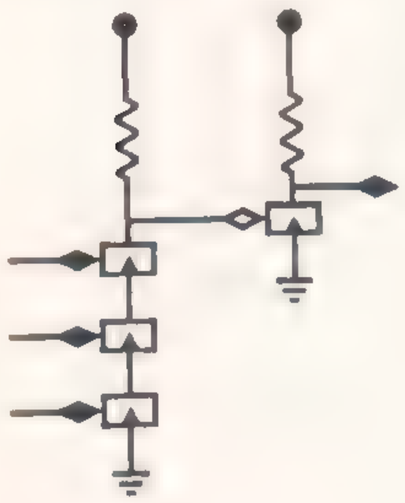


Figure 1

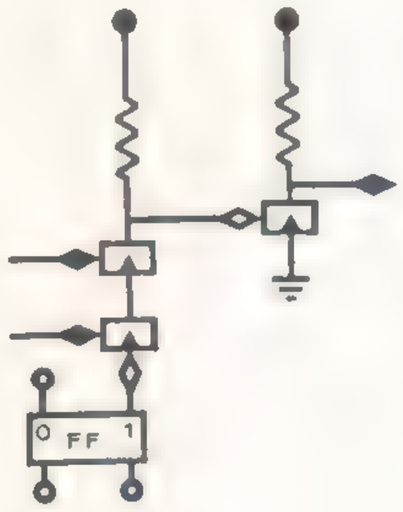


Figure 2

If inverters are in series with the output of a flip-flop, as in Figure 2, the flip-flop buffer inverter is considered to be one of the three allowed series transistors.

When the output of a series of inverters is driving the input of a pulse amplifier or delay unit or the set or clear input of a flip-flop, as in Figure 3, a fourth transistor serving as a pulse gate may be added in series. Only three may be used in series when driving the complement input of a flip-flop.

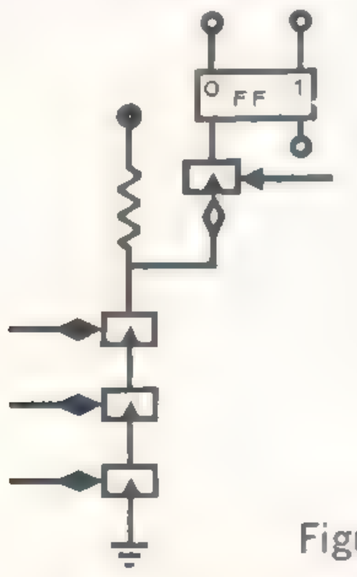


Figure 3

It is important to note that a clamped load resistor is tied to the emitter of each pulse transistor when it is being driven from an inverter or a network of inverters, as in Figure 3. (The clamped load resistor is not needed when the pulse inverter is driven from a single series of inverters and the length of wire between inverters is short.)

Because inverters are not really ideal switches, each collector of a series string of DC inverters supplying a pulse inverter will go somewhat negative during the pulse. This means that, if a series of inverters is supplying both pulse current and a DC signal, care must be taken because a signal will occur in the DC output during the pulse.

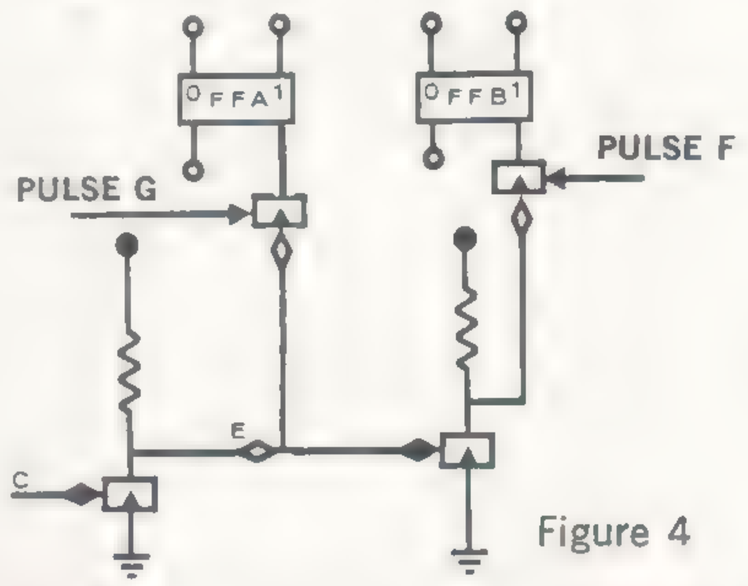


Figure 4

In Figure 4, if pulses F and G are simultaneous and the input C is negative, flip-flop A should be set by the pulse, but flip-flop B should not be set. However, during the pulse, collector E of the DC inverter feeding flip-flop A will go slightly negative. It will partly turn on the DC inverter feeding flip-flop B, and sometimes it will set flip-flop B as well as flip-flop A. This network will work only if the pulses F and G are not simultaneous.

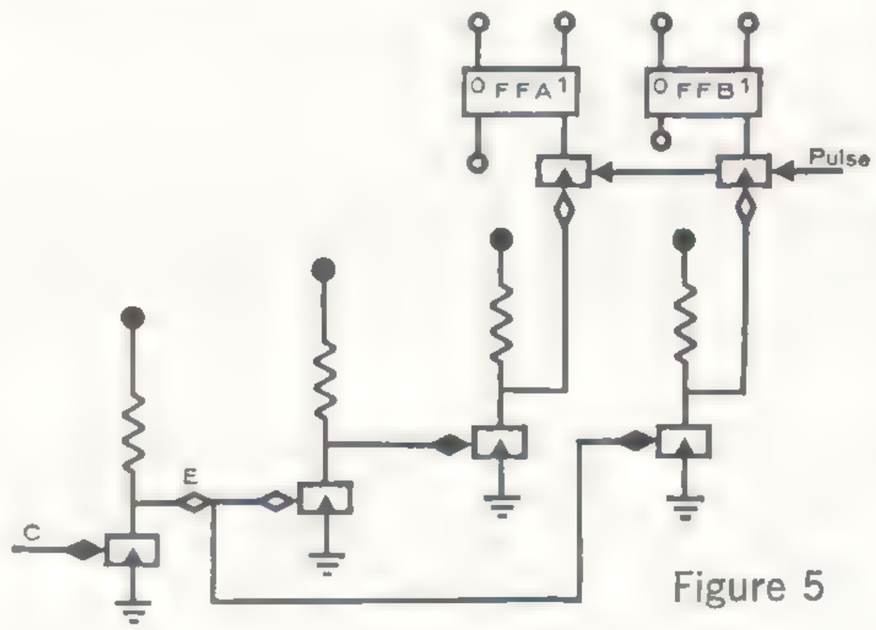
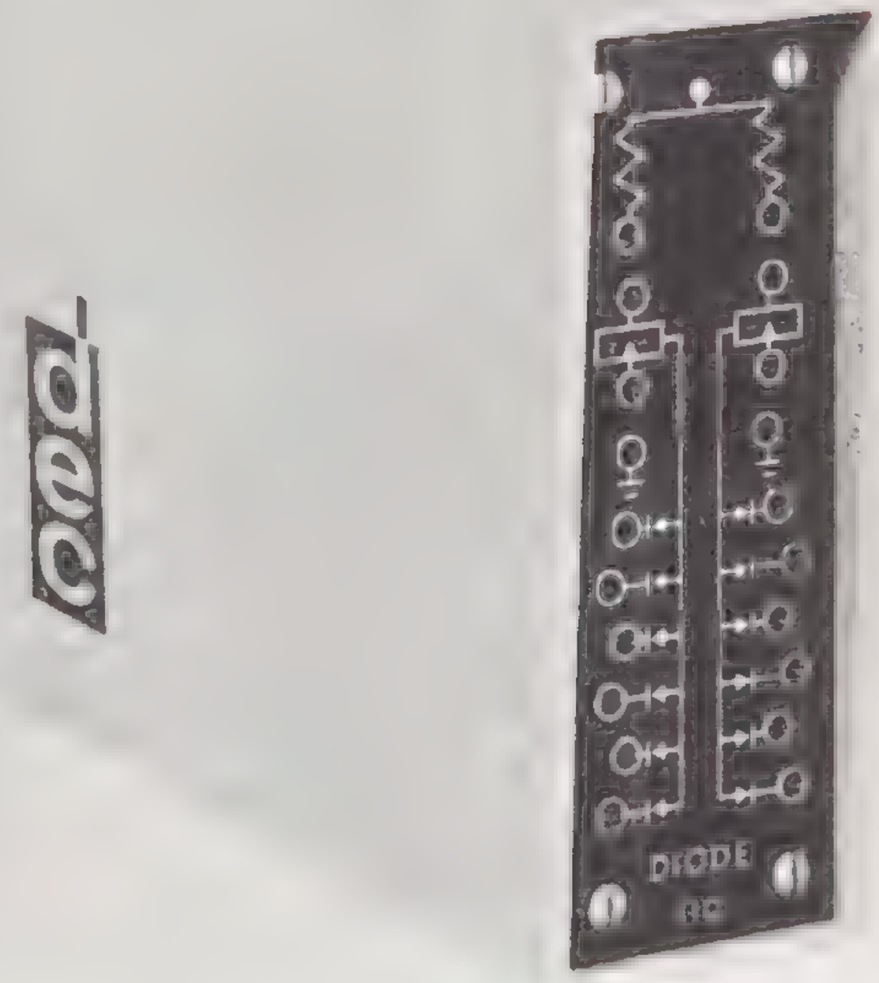
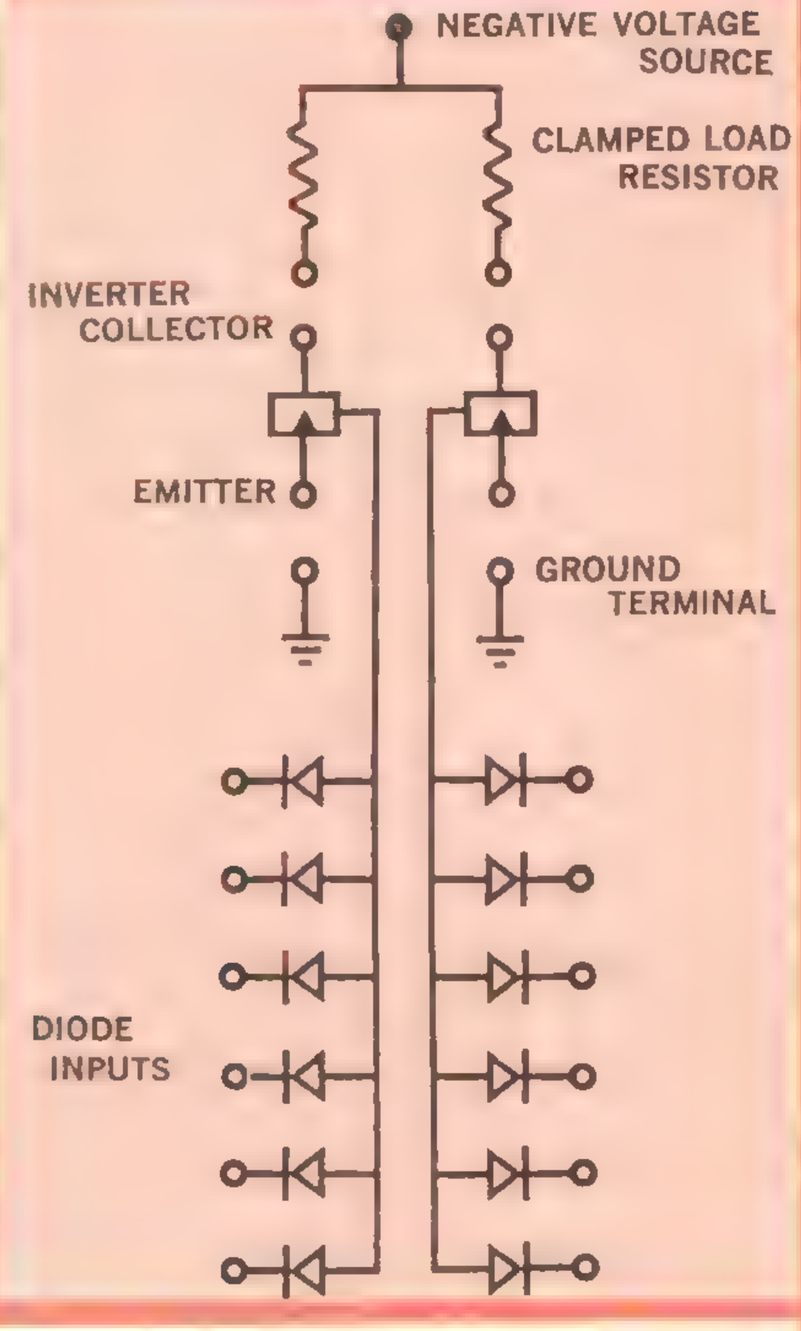


Figure 5

The network shown in Figure 5 will work whether or not the pulses are simultaneous. Two additional inverters have been added so that collector E will no longer be pulled negative by the pulse, since the pulse current will now come directly from ground instead of collector E. (If both outputs are feeding the same flip-flop, the network shown in Figure 4 can be used safely because the output of the A side will be much greater than that of the B side.)

110
DIODE NOR





The Diode NOR contains 2 six-input diode gates that are OR circuits for negative level inputs and AND circuits for ground inputs. This unit may also be used for mixing Negative Pulses. Each diode gate is connected to the base of a transistor inverter which is similar to those in the DEC Inverter Type 103. The emitter and collector are available for external connections. Delay of a level through a diode and its inverter is approximately 30 nanoseconds.

[illegible] — DEC Standard Levels or equivalent (3 units of Base Load shared among the negative inputs) or DEC Standard 70 nanosecond Negative Pulses (1 unit of Pulse Load) may be used to drive the NOR Diodes. [illegible] — DEC Standard Levels or equivalent, including grounding if emitter gating is not desired, may be applied to the emitter. If the collector is connected directly or through another inverter to a clamped load resistor, the emitter represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, the emitter represents 1 unit of Pulsed Emitter Load.

[illegible] The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles or 7 where speed is not a problem: (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

A collector with no clamped load resistor can drive one unit of DC Emitter Load. (A collector can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time.) No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: −15 volts/20 ma; −3 volts/36 ma; +10 volts (A) 1.3 ma; +10 volts (B) 1.3 ma.

SPECIAL COUNTER

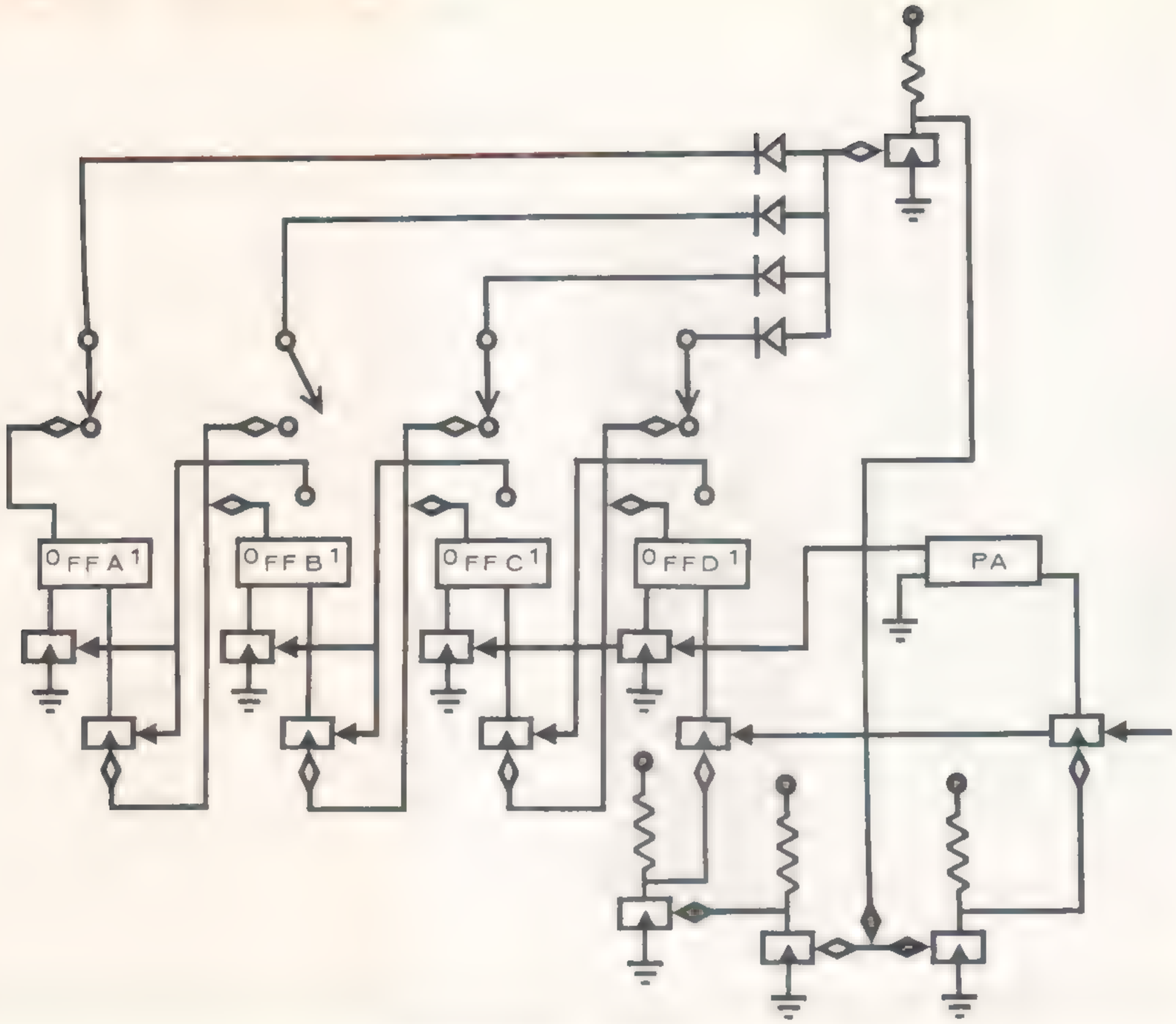
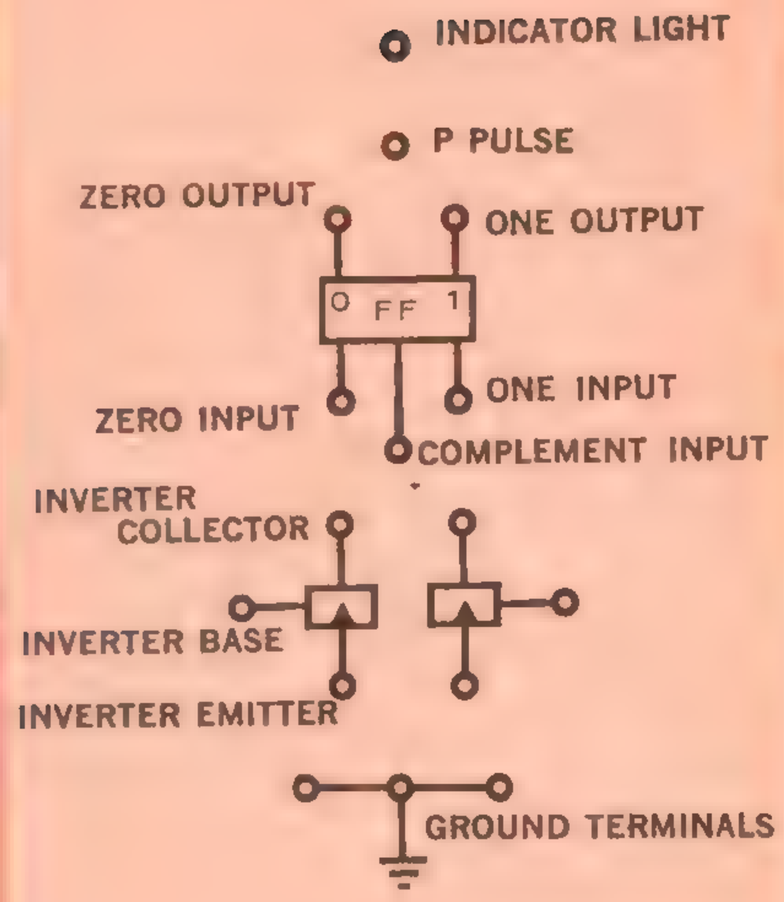


Figure 1 — SPECIAL COUNTER (12 illustrated)

Often it is desirable to build a counter that will produce a signal after a particular number (N) of events have occurred. If N is an integer power of 2, the output is automatically produced by the final digit of a counter of appropriate length. If N is not a power of 2, gating must be performed to detect the desired number, generate a signal, and reset the counter to 0. Diode gates may be used to sense the number N-1, close the input to the counter, and re-route the Nth input pulse so that it will clear the counter and generate an output signal. This is a completely general method which will work for any value of N.

The system in Figure 1 counts to 12. On the 11th count the NOR gate activates its inverter which in turn closes the counter to the incoming 12th pulse and connects the circuitry that will permit the pulse amplifier to clear the counter on the 12th pulse.

201
FLIP-FLOP



The Flip-flop Type 201 is basically a two-transistor static flip-flop with built-in output amplifiers, indicator light, source of counting carry pulses (P Pulse), complement input and two inverter gates. It has sufficient built-in gating to be used as one digit of a shift register, or one digit of a binary counter. It can also be used for all general type logical operations. It has a built-in delay of about 90 nanoseconds, so that its output terminals can be sensed at the same instant that an input terminal is being pulsed. The output voltage swing is diode clamped at −3 volts, to provide a constant output voltage independent of loading, within the given restrictions.

INPUT: ZERO input, ONE input and complement input each must come from the collector of a pulse gate. More than one pulse gate can be connected to the same terminal. The above signals can occur in any sequence, at any frequency, and at any time intervals which have a minimum of 0.2 microsecond between any two signals (5 megacycles). The two inverters are similar to those included in the DEC Inverter Type 103.

OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving: (a) 10 units of Base Load at 5 megacycles or 14 units where speed is not a problem; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. The output signals have built-in delays so they can be sensed reliably at the same time that the input is being pulsed. This is very useful in counter, shift register and adder applications.

Each time the complement terminal is pulsed, a DEC Standard 70 nanosecond Negative Pulse, capable of driving 1 unit of Pulse Load, will occur on the P terminal. Delay from the time the input inverter is pulsed to the time the P Pulse occurs is approximately 20 nanoseconds.

POWER: −15 volts/94 ma; −3 volts/19 ma; +10 volts (A)/1.4 ma.

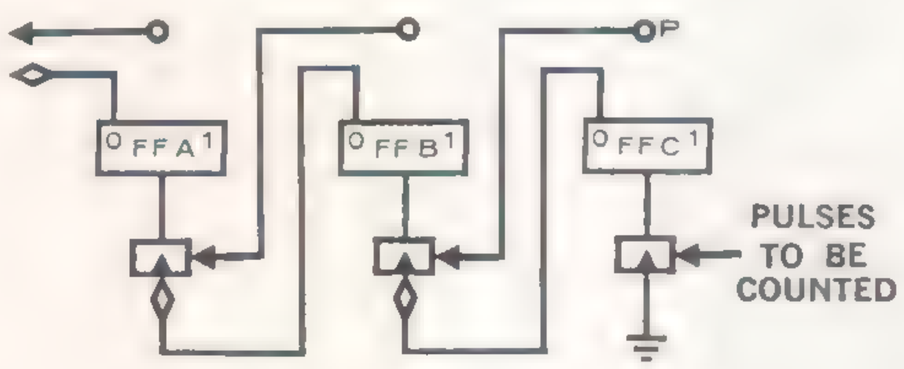
BINARY COUNTERS

A typical counter arrangement using DEC Complementing Flip-flops is shown above. The pulses being counted enter on the right. They always complement flip-flop C and generate a standard pulse at P. This P Pulse complements flip-flop B when flip-flop C holds a ONE. When this P Pulse gets through the gate and actually complements B, it will generate a P Pulse out of B. The process is continued down the length of the counter. Only one inverter and one flip-flop are needed for each bit in the counter.

The series connection of P Pulses and gates forms a high-speed carry chain. The carry propagate time per digit (20 nanoseconds) is much less than the flip-flop's total transition time.

To assure that flip-flop C will not be in the process of changing state while flip-flop B is receiving its carry pulse, a delay has been built into each flip-flop package. This insures that the ONE and ZERO output terminals will not change until after the carry pulse has been gated.

A down counter may be constructed by conditioning each pulse gate from the ONE terminal of the previous flip-flop (instead of the ZERO terminal).

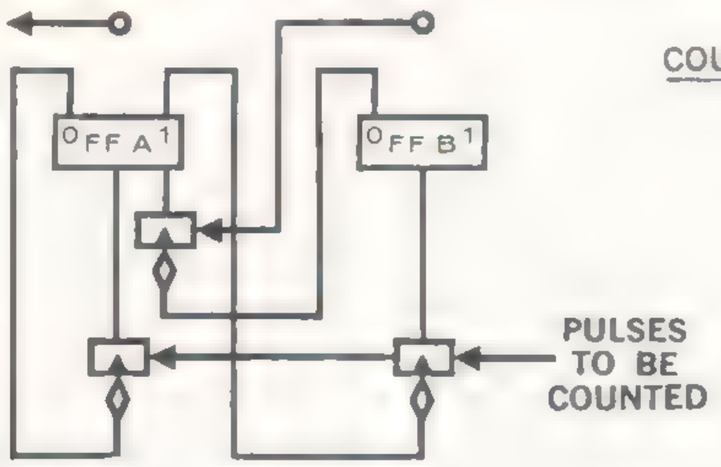


COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 1 — BINARY COUNTER

SPECIAL COUNTERS

The extra inverters included in the 201 package allow additional flexibility for performing special counts, such as the "count of three" illustrated. The inverters are connected to assure that the counter will reset after the count of two. Since only one pulse in three will enter the complement input of flip-flop A, the P Pulse output of that flip-flop provides a convenient carry signal.



COUNTING SEQUENCE	
0	00
1	01
2	10

Figure 2 — COUNT OF THREE

SHIFT REGISTERS

Each 201 package will make one stage of a shift register. DEC shift registers employ simultaneous jam transfer. As illustrated in Figure 3, the contents of all flip-flops are simultaneously moved to the right when the shift pulse occurs. Since the flip-flop outputs do not change until after the shift pulse has passed, no logical delays are needed between flip-flops.

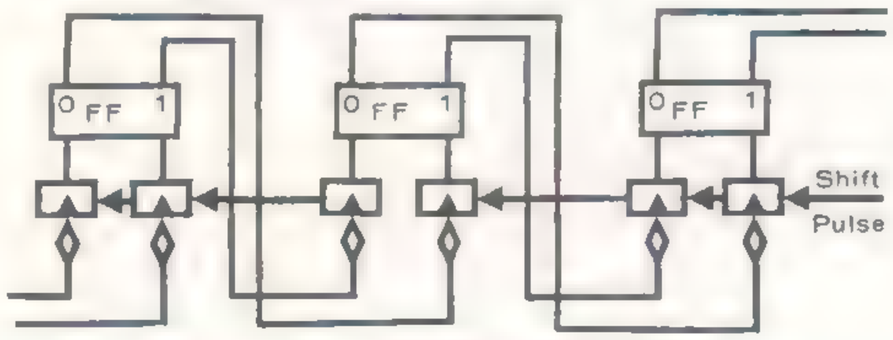


Figure 3 — SHIFT REGISTER

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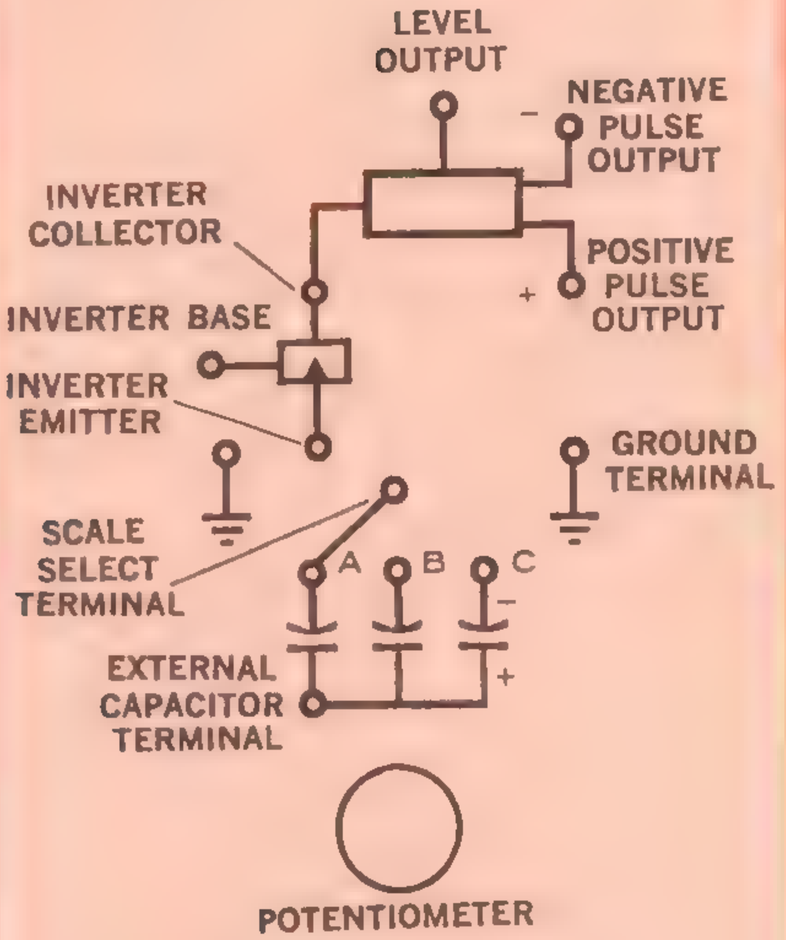
100 SERIES
LABORATORY MODULES
5 MEGACYCLES

302
DELAY (ONE SHOT)



The Type 302 Delay unit is a mono-stable multivibrator. When the input terminal is grounded, either through the inverter or externally, the level output terminal will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time and then back to ground. A pulse transformer generates a DEC Standard 70 nanosecond Pulse at the pulse output during the final transition. The pulse transformer has both positive and negative terminals so that either polarity pulse may be obtained. Typical output and input wave forms are shown in Figure 1.

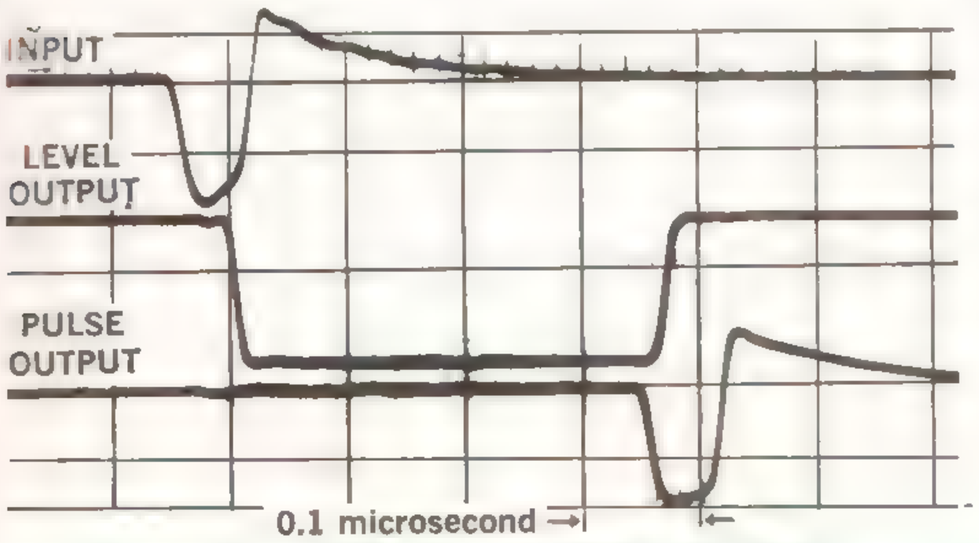


Figure 1 — INPUT AND OUTPUT VS TIME

The delay interval is determined primarily by the capacitor connection. An internal potentiometer provides for the fine adjustment. The capacitor A will permit adjustment from approximately 0.2 microsecond to 2.5 microseconds; B, from approximately 2.2 microseconds to 34 microseconds; and C, from approximately 32 microseconds to 550 microseconds. A longer delay may be accomplished by installing an additional capacitor at the external capacitor terminal.

Circuit recovery time is equal to 20% of the maximum delay available on that particular circuit's capacitor connection. A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.3%.

INPUT: The input to the delay is a DEC Standard 70 nanosecond Negative Pulse on the base of a pulse gate, such as the one included in the delay module. The base of the built-in pulse gate represents 1 unit of Pulse Load. If more logical inputs are desired, they can be provided by connecting pulse gate collectors to the collector of the built-in pulse gate.

Mixing of several pulses can also be accomplished by using half of a DEC Diode Type 110 with DEC Standard 70 nanosecond Negative Pulses applied to the diodes and the collector tied to the collector of the built-in pulse gate.

OUTPUT: Level — When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval and is capable of simultaneously driving: (a) 8 units of Base Load if speed is important, otherwise 12 bases; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. Pulse — at the end of the delay interval, a DEC Standard 70 nanosecond Pulse of either polarity occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/80 ma; −3 volts/0 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0 ma;

TYPICAL APPLICATION

WAVE FORM GENERATOR

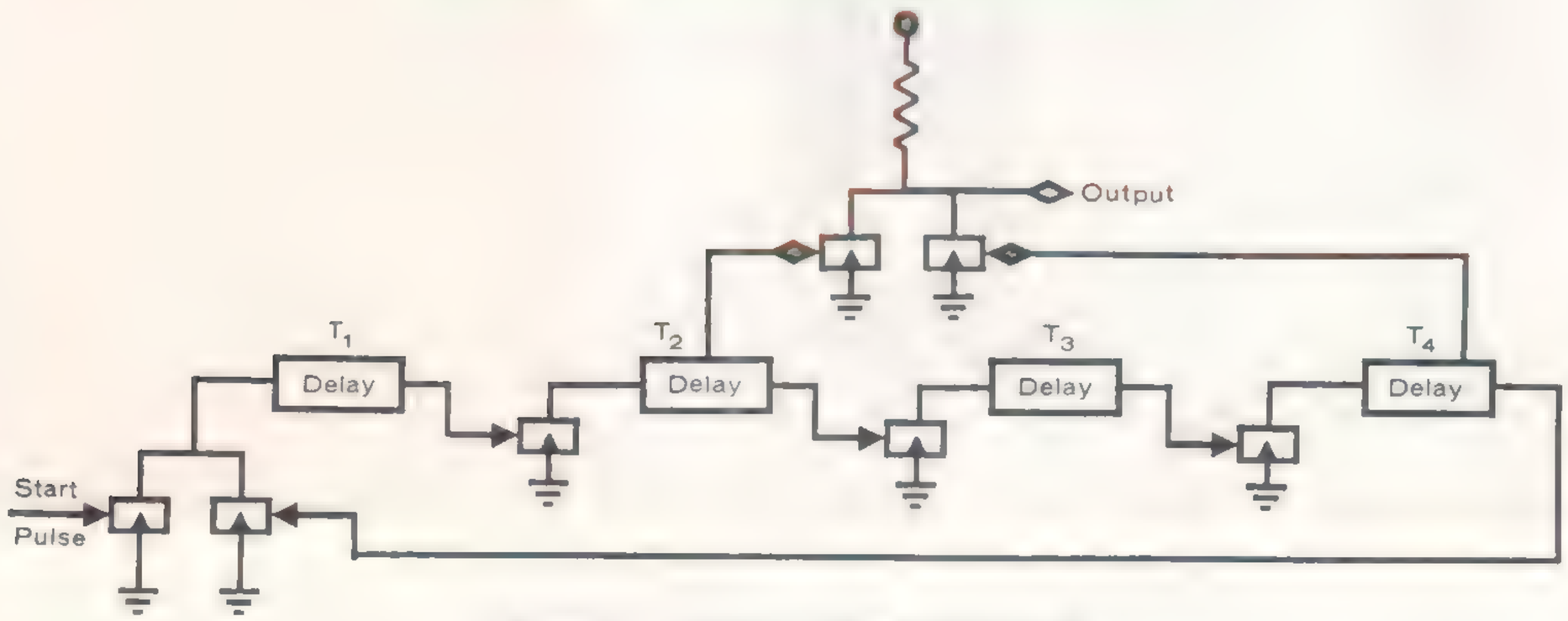


Figure 2 — WAVE FORM GENERATOR

Delay units are particularly useful in generating signals of arbitrary width. The network of delays in Figure 2 will produce the waveform in Figure 3.

The 1st and 3rd delays, not being connected to the output inverters, will produce no signal during their delay period. The 2nd and 4th, however, will produce a ground output for the duration of their respective delays. The wave form is periodic, since the pulse output from T_4 goes back to T_1. Due to delay recovery time, more than one delay unit is necessary to recycle the pulse.

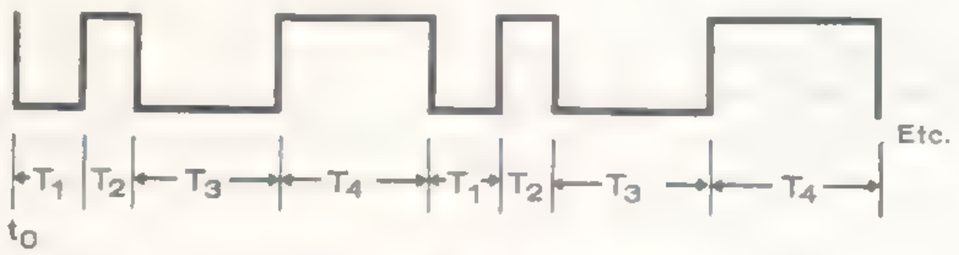


Figure 3 — OUTPUT WAVE FORM

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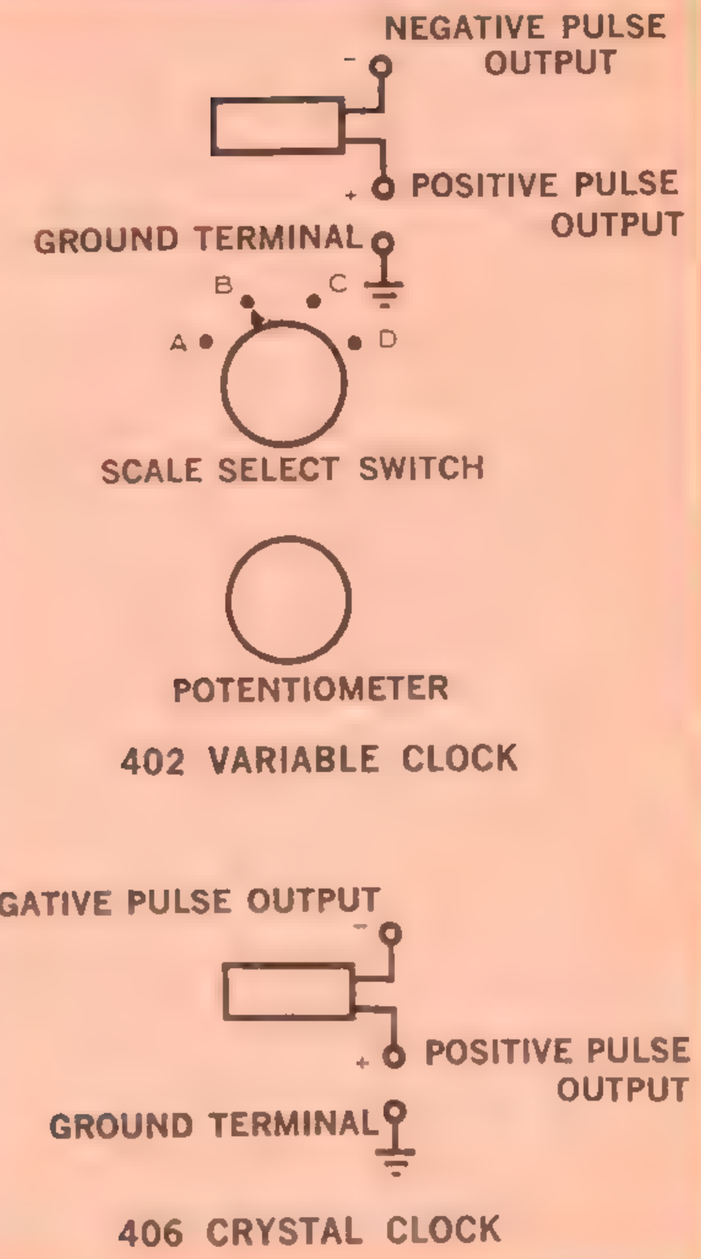
100 SERIES
LABORATORY MODULES
5 MEGACYCLES

402-406
CLOCKS



DEC variable clocks produce standard pulses from stable, RC-coupled oscillators which have a wide range of frequencies available. These clocks are often used as a primary source of timing for large systems. Where very precise timing is needed, crystal clocks which contain a single-frequency crystal oscillator are available.

The Type 402 contains a multi-vibrator type, variable frequency oscillator with a pulse output for use as a source of timing pulses for DEC System Modules. The frequency is variable from 500 kilocycles to 5 megacycles. Four scales provide magnitude control and a built-in potentiometer permits fine adjustment. Lower frequencies may be obtained by adding a capacitor internally in parallel with the capacitor for the lowest scale.

The Type 406 employs a series resonant crystal oscillator circuit and pulse shaping buffer amplifiers to provide very precise timing. The amplifiers produce DEC Standard 70 nanoseconds Pulses in the 500 kilocycle to 5 megacycle range. The clock frequency, specified by the customer, is stamped on the module.

OUTPUT: The output is a DEC Standard 70 nanosecond Pulse which occurs at the preselected frequency. The pulse may be made either positive or negative by grounding the appropriate output terminal. The signal can drive 8 units of Pulse Load. **Crystal Clock:** The stability of the crystal clock's output frequency is 0.01% over a temperature range of −20 to +55 degrees centigrade. **Variable Clock:** A 20% change in the power supply voltage of the Type 402 clock will change the prf less than 1% and its pulse to pulse jitter is less than 0.2%.

POWER: Type 402 −15 volts/66 ma; −3 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. **Type 406** −15 volts/47 ma; −3 volts/0 ma; +10 volts (A)/3.8 ma; +10 volts (B)/3.8 ma.

TYPICAL APPLICATION

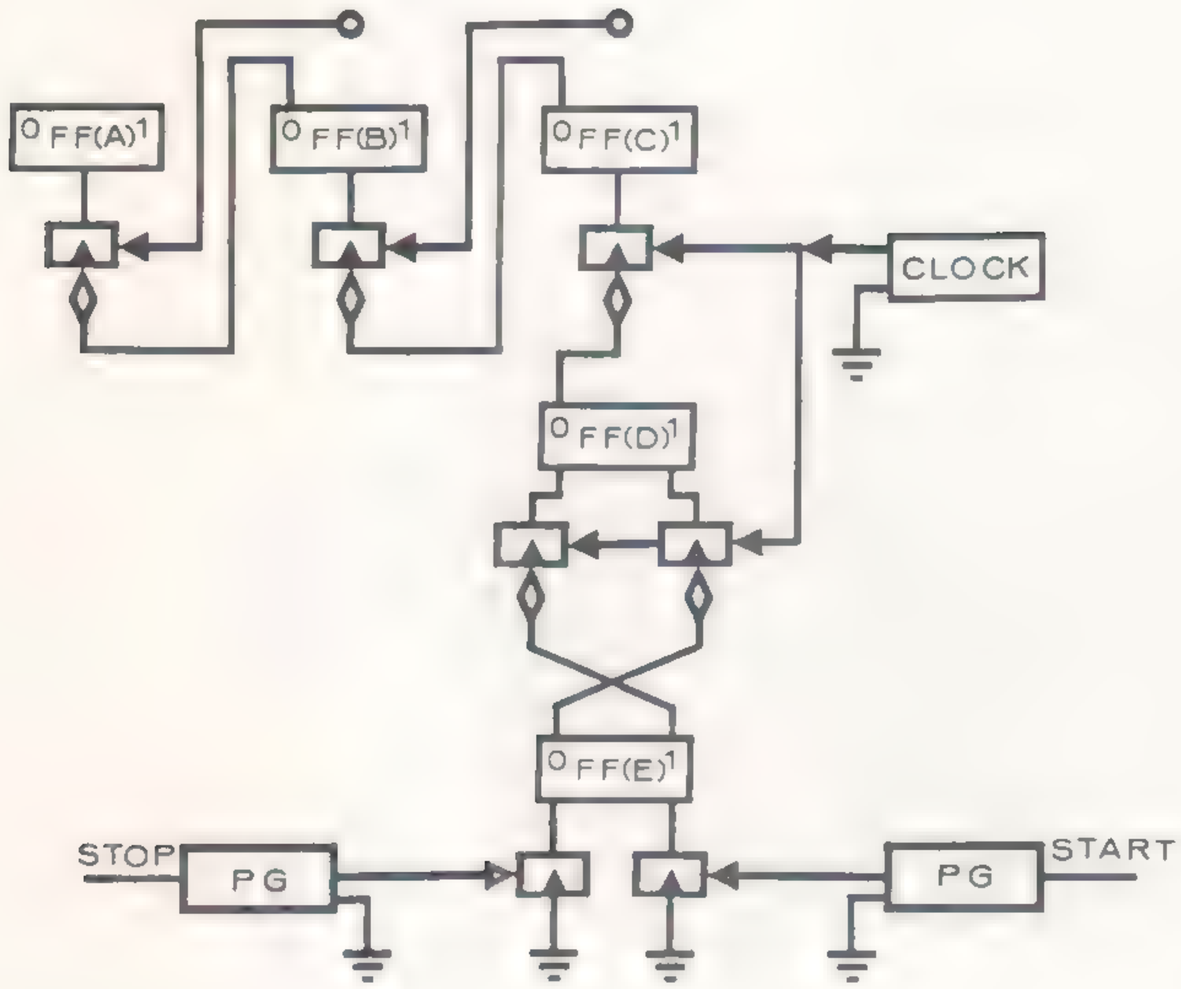


Figure 1

Either the Type 402 or the Type 406 could be used as part of the timer circuit shown in Figure 1. The start of an event triggers the pulse generator which grounds the ONE input of flip-flop E through an inverter. This brings the ZERO output of flip-flop E to a ground level which permits the next clock pulse to set flip-flop D. All following clock pulses will be gated into the counter. When a stop pulse arrives, the same procedure is used in stopping the counter.

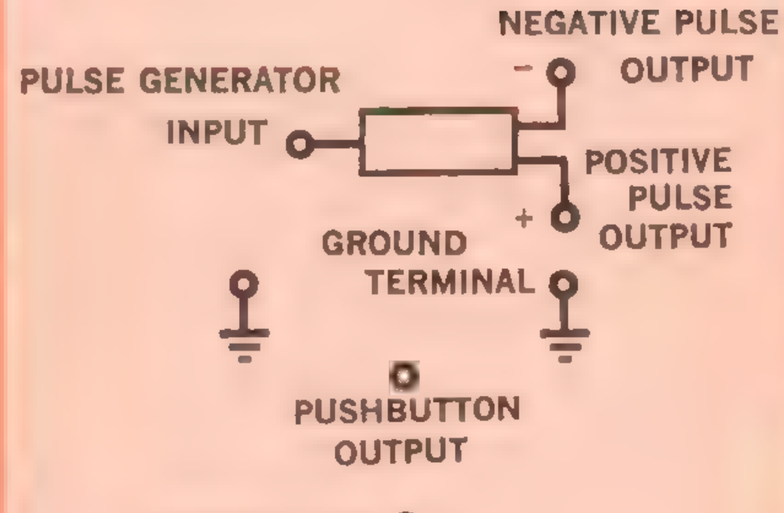
The purpose of flip-flops D and E is to change the randomly occurring start, stop pulses into a synchronous level for gating the counter. The input pulses are converted to asynchronous levels by flip-flop E. Flip-flop D converts these asynchronous levels into synchronous levels. This assures that a split or partial pulse will never enter the counter, such a pulse could propagate only part of the way down the carry chain and result in an erroneous number.

The timer circuits such as shown in Figure 1 are useful in counting the delay between the occurrence of two events. A variation of the timer circuit is to replace the individual start, stop inputs with a single input going to the complement terminal of flip-flop E. This would allow the measurement of the time between the occurrence of two events on the same line.

digital

100 SERIES
LABORATORY MODULES
3 MEGACYCLES

410
PULSE GENERATOR



The Type 410 converts external signals to DEC Standard Pulses. The Schmitt multivibrator produces a DEC Standard 70 nanosecond Pulse at the output every time the input voltage goes more negative than −2.5 volts after having been more positive than −1.0 volts. This unit contains a push button and an integrating circuit which filters contact bounce.

INPUT: The input is a DC connection, thereby eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. The input signal should stay between +10 volts and −10 volts.

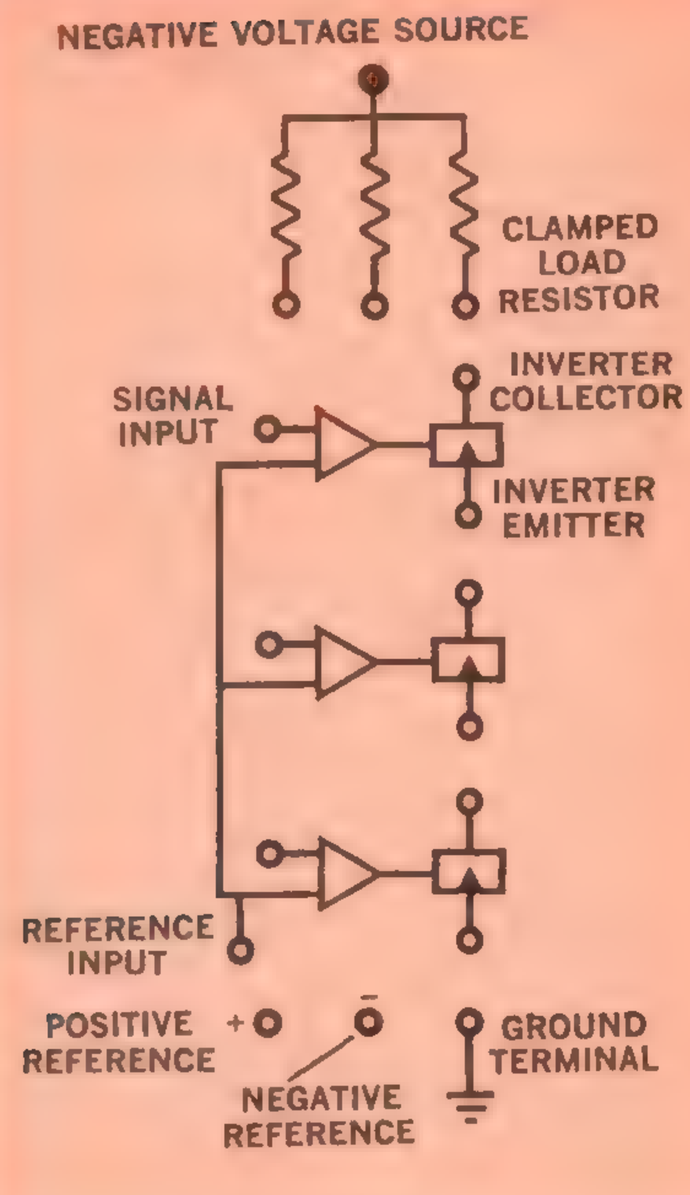
OUTPUT: The output of the Pulse Generator is a DEC Standard 70 nanosecond Pulse of either polarity. The pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. The maximum prf is 2 megacycles. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/34 ma; −3 volts/0 ma; +10 volts (A)/5 ma; +10 volts (B)/5 ma.

d g t l

100 SERIES
LABORATORY MODULES
5 MEGACYCLES

501
LEVEL STANDARDIZER



Three difference amplifiers convert signals in the range of ±10 volts to DEC Standard Levels. Reference levels may be between +10 and −1.5 volts. The maximum ZERO offset is 0.1 volt and the minimum dynamic range is 0.1 volt. Three reference voltages are provided in the package. These are: +1.2 ±0.1 volts, −1.5 ±0.1 volts, and ground. The output is from a transistor inverter similar to the DEC Inverter Type 1105. If the transistor collector is connected to the load resistor (available in the package) and its emitter is grounded, the output will be at −3 volts when the input is positive with respect to the reference voltage and at ground when the input is negative with respect to its reference.

INPUT: Reference — An external reference voltage in the range of +10 to −1.5 volts may be used. The current required per standardizer circuit is +0.1 ma if the reference is more positive than the input, and −0.2 ma if the reference is more negative than the input. When the reference is more negative than +3.0 volts, and also more negative than the input, the load is 1800 ohms to +3.3 volts. Signal Input — Voltages may be in the range of ±10 volts. If the input is more positive than the reference, the load is +0.1 ma. If the input is more negative than the reference, the load is −0.2 ma. If the input is more negative than −2.7 volts, the load is 800 ohms to −2.5 volts.

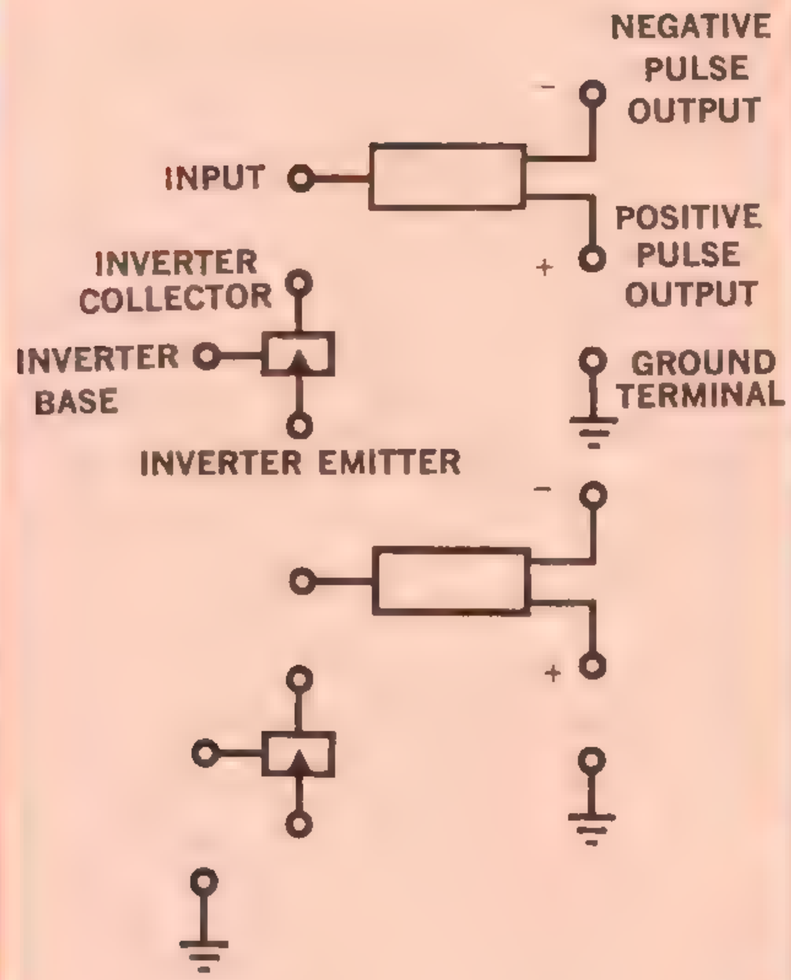
OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of a flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem); and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters, provided there is not more than one simultaneous emitter-collector path to a DC Emitter Load. No more than 3 level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, 4 gates may be connected in series.

POWER: −15 volts/68 ma; −3 volts/30 ma; +10 volts (A)/0.5 ma; +10 volts (B)/18 ma.

d g t a l

100 SERIES
LABORATORY MODULES
0 MEGACYCLES

602
PULSE AMPLIFIER



The Type 602 contains two pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Two standard inverters are included for gating the inputs. The inverters are similar to those in the DEC Inverter Type 103. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 5 megacycles. The DEC Diode Type 110 may be used in conjunction with the pulse amplifier for conveniently mixing pulses from several sources.

INPUT: The input must come from the collector of one or more pulse gates. The signal on the base of the pulse gate is normally a DEC Standard 70 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 50 nanoseconds, can be used. Input pulses of less than −0.5 volts will not generate an output pulse. Many pulse gate collectors can be connected together to mix pulse sources. The two pulse gates are inverters like those included in the DEC Inverter Type 103.

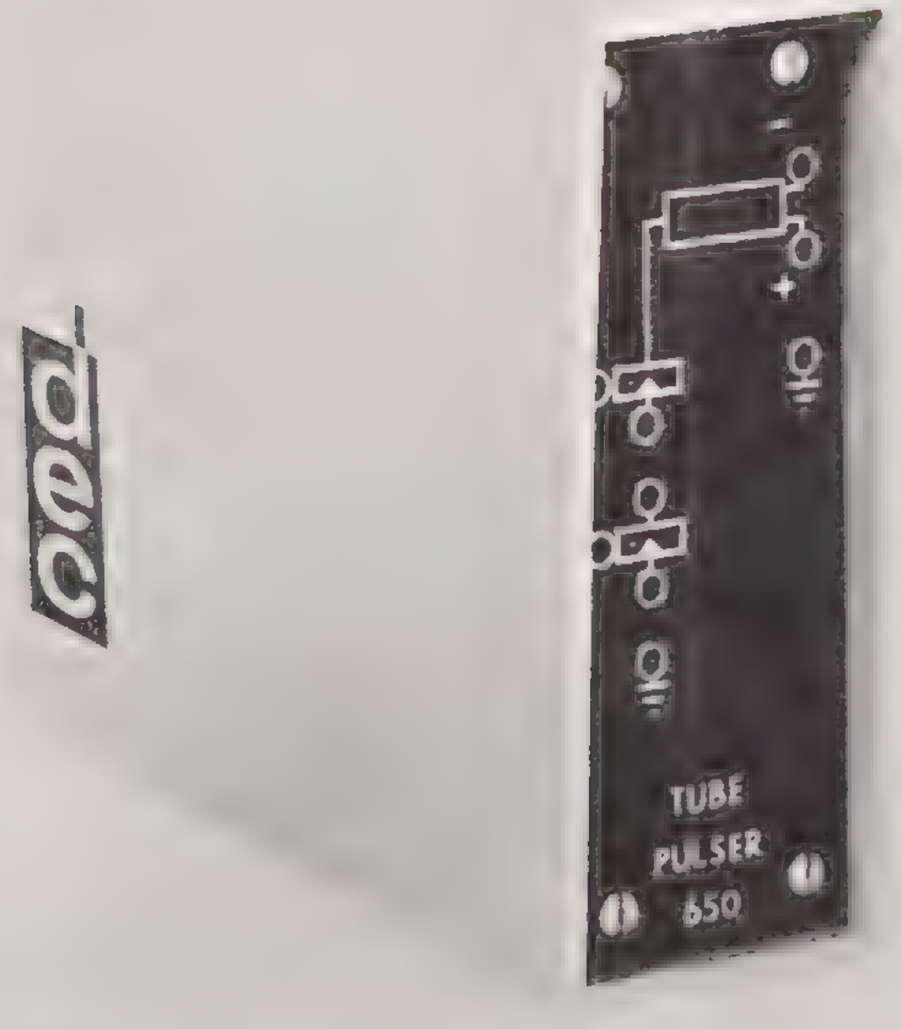
OUTPUT: The output is a DEC Standard 2.5 volt 70 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. The pulse will be negative if the positive output is grounded; it will be positive if the negative output is grounded. Each output is capable of driving 16 units of Pulse Load.

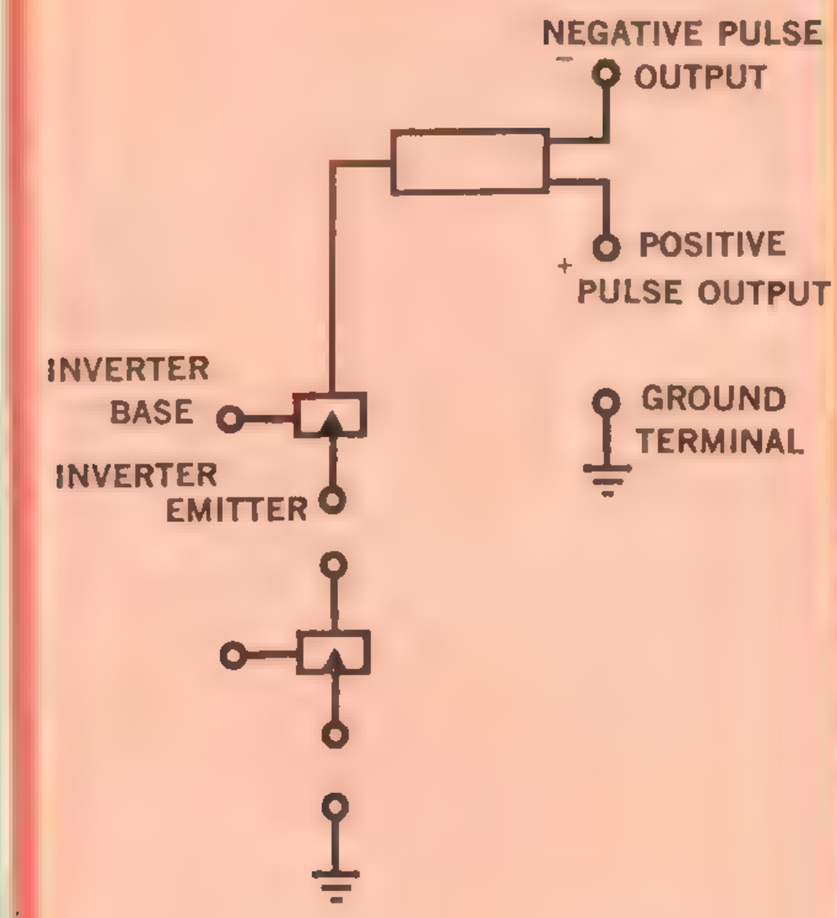
POWER: −15 volts/88 ma; −3 volts/1.4 ma; +10 volts (A)/0.14 ma; +10 volts (B)/0.14 ma.

digital

100 SERIES
LABORATORY MODULES
5 MEGACYCLES

650
TUBE PULSER





The Tube Pulser Type 650 is used for providing signal compatibility between DEC Standard 70 nanosecond Negative Pulses and other types of digital circuits requiring larger signals such as vacuum tube circuits.

The Tube Pulser contains a power amplifier and two inverters for gating the input: one inverter is permanently connected. The second inverter may be used for level gating the input pulses to the Tube Pulser. Delay through the Tube Pulser is approximately 30 nanoseconds. Input pulses may occur at any frequency up to 1 megacycle.

INPUT: The input to the inverter base should be a DEC Standard 70 nanosecond Negative Pulse or equivalent. Input pulses of less than −0.5 volts will not generate an output pulse.

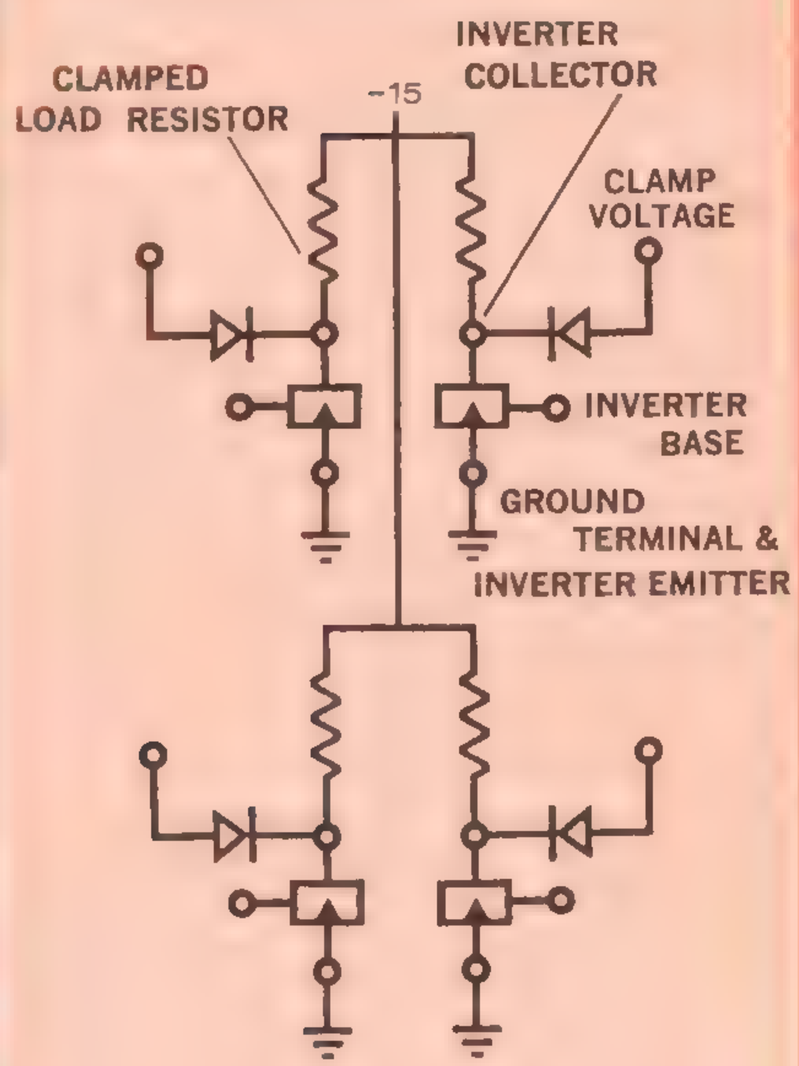
OUTPUT: A 15 volt 0.1 microsecond pulse occurs at the output every time the input signal meets the input requirement. The output can deliver 10 volts into a 200 ohm load resistor. Negative Output Pulse connection: take output from negative terminal and ground positive terminal. Positive Output Pulse connection: take output from positive terminal and ground negative terminal.

POWER: −15 volts/13.5 ma; −3 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0.3 ma.

digital

100 SERIES
LABORATORY MODULES
5 MEGACYCLES

667
NEGATIVE LEVEL AMPLIFIER



Four grounded emitter inverters amplify DEC Standard Levels into negative levels, up to −15 volts. Clamping diodes connected to each inverter collector are brought out to the front panel and may be returned to any voltage between ground and −15 volts to obtain any desired output level within this range. Delay through an amplifier is approximately 50 nanoseconds.

INPUT: DEC Standard Levels or equivalent drive the base input (1 unit of Base Load). When the base is at ground level, the output is at the clamp voltage. When the base is at −3 volts, the output is at ground level.

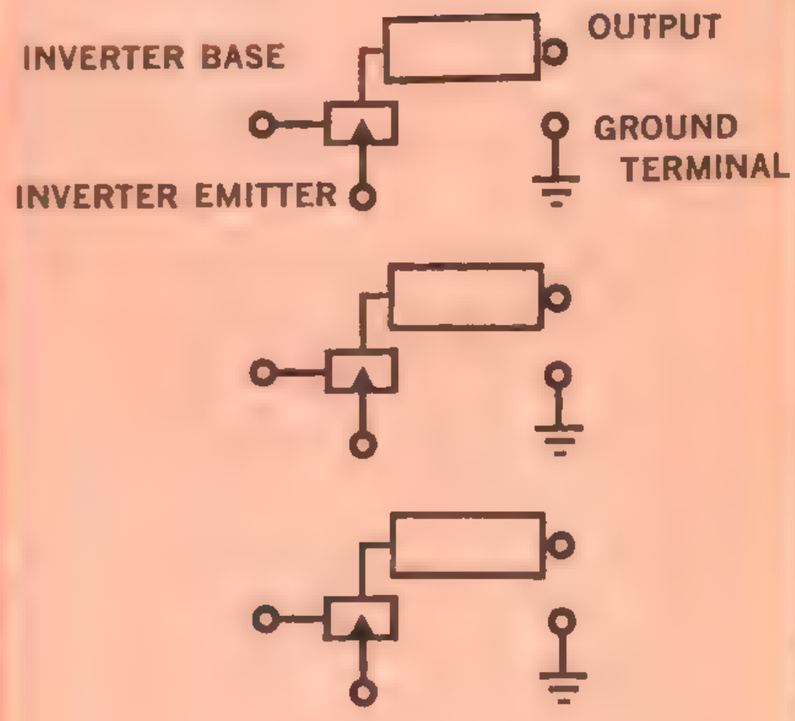
OUTPUT: The upper output level is ground. The lower output level is determined by the external supply attached to the clamp diodes, and must be in the range of ground to −15 volts. When the output signal is at ground, each inverter will supply up to 5 ma. When the output level is negative, the maximum current which can be accepted is determined by the 1500-ohm resistor to −15 volts.

POWER: −15 volts/40 ma; +10 volts (A)/0.28 ma; +10 volts (B)/0.28 ma.

digital

100 SERIES
LABORATORY MODULES
3 MEGACYCLES

668
POSITIVE LEVEL AMPLIFIER



The Type 668 contains three amplifiers which produce positive output signals (0 and +4.5 volts) for driving external circuitry. Maximum prf is 1 megacycle. Each amplifier has one inverter.

INPUT: DEC Standard Levels or equivalent drive the amplifiers. The base input represents one Base Load; the emitter represents one unit DC Emitter Load.

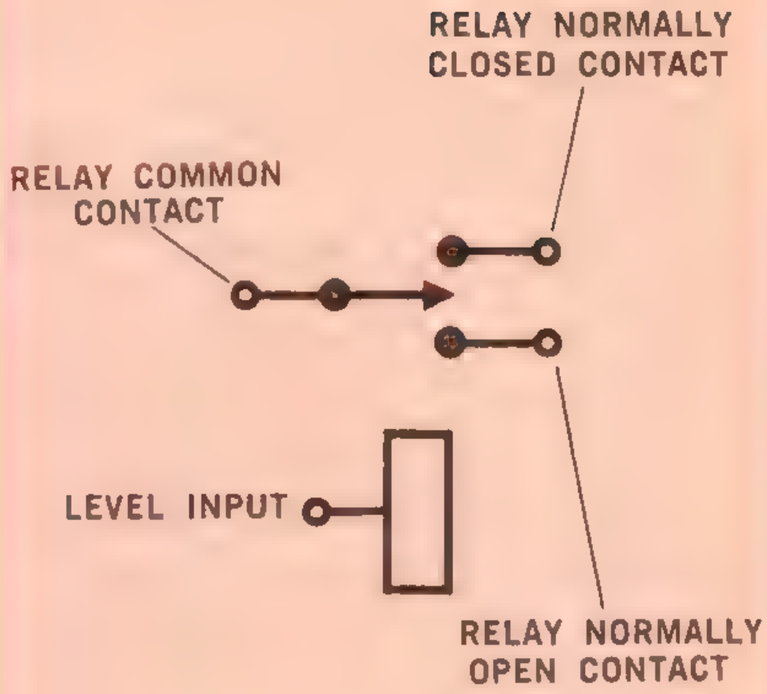
OUTPUT: The output is through a 100-ohm series resistor. If the base input is −3 volts and the emitter input is ground, the output will be +4½ volts; in this state the amplifier can supply 1 ma. If the base input is ground or the emitter input −3 volts, the output will be ground; however, the drop across the 100-ohm resistor must be taken into account. The amplifier can draw 14 ma in this state.

POWER: −15 volts/30 ma; −3 volts/0 ma; +10 volts (A)/0.5 ma; +10 volts (B)/15 ma.

d i g i t a l

100 SERIES
LABORATORY MODULES
5 MEGACYCLES

801
RELAY



The Type 801 contains a relay driver amplifier and a single pole double throw relay. This unit enables DEC Module circuitry to drive electromechanical units requiring power beyond the driving capabilities of regular transistor circuitry.

INPUT: The input is a DEC Standard Level (1 unit of Base Load). If other input signals are used, they should stay between limits of +5 volts and −10 volts. The relay is not energized when the input level is ground or absent.

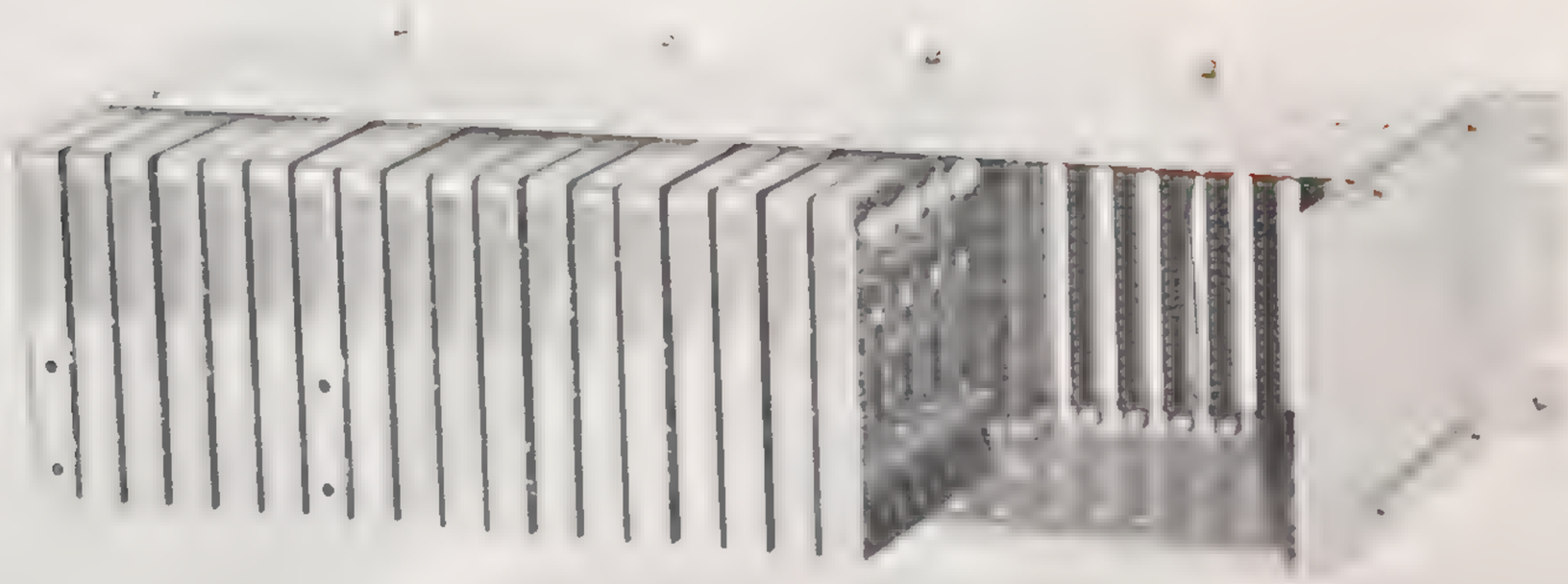
OUTPUT: The relay contacts are single-pole, double-throw and are rated at 2 amperes.

POWER: −15 volts/20 ma; −3 volts/0 ma; +10 volts (A)/0.15 ma; +10 volts (B)/0 ma.

digital

1000 SERIES
SYSTEM MODULES
& MINICYCLES

SERIES CHARACTERISTICS



DEC System Modules and Mounting Panels are designed for high-density packing

DEC 1000 Series System Modules are a coordinated set of solid state digital circuits operating at frequencies up to 5 megacycles. They are mounted on protective aluminum frames measuring ½ by 4½ by 7 inches overall. All logic and power connections are through 22-pin Amphenol plugs electrically connected to the circuit boards by flexible wires to minimize strain. Plug-in mounting panels for System Modules are available in various widths, capacities and wiring options.

System Modules offer a unique combination of advantages for the design and construction of all types of digital systems. They are built for long, dependable service, whether used interchangeably in different applications or installed in permanent systems. In addition, they are available in a wide choice of circuits to meet various systems requirements.

General purpose circuits permit systems to be implemented with a minimum number of different types of modules. Special purpose units provide economy in the construction of large-scale systems. Input-output units enable DEC circuits to accept a variety of different input signals, such as analog voltages, and to drive many types of special output equipment, such as electro-mechanical devices.

Since all Digital Modules are compatible across speed lines, it is possible to extend system capabilities or to achieve important savings in systems construction by incorporating units from other lines. The 1000 Series units are electrically and mechanically compatible with 4000 and 6000 Series System Modules, and they are electrically compatible with 100, 3000 and 5000 Series Laboratory Modules.

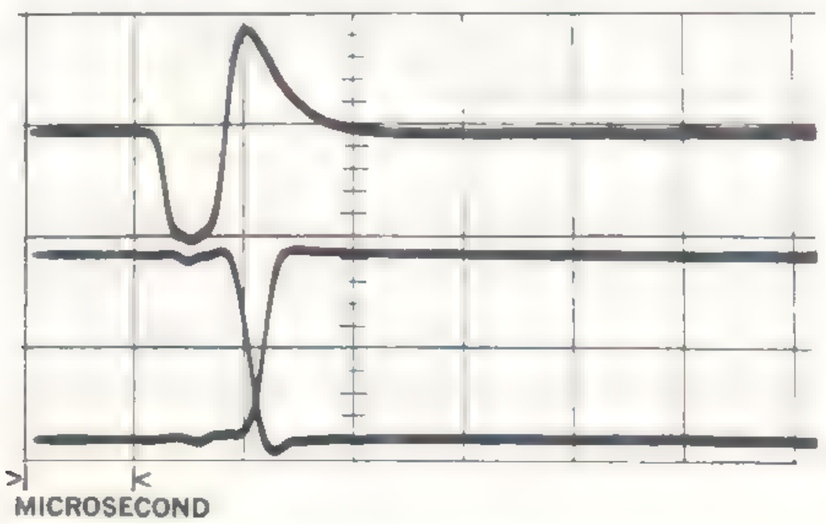
The logic employed in all DEC System Modules, as described in the Introduction, uses static flip-flops with level logic and pulse sampling. Except in the Type 1213, flip-flop outputs are buffered and include a built-in delay which permits the flip-flops to be pulse-sampled while being changed. Logic gating is performed with DEC saturating transistor inverters and multiple-input diode circuits internally connected to transistor inverters for signal amplification. This method of transistor gating and pulse sampling allows the construction of systems with a minimum concern over wiring techniques and lead lengths.

The basic selection of general purpose logic modules in the 1000 Series includes inverter packages for logical gating, negative and positive diode NORs, a flip-flop with buffered level outputs and built-in carry pulse output, a delay one-shot with built-in pulse amplifier, a variable frequency clock, and a three pulse amplifier package for logical gating and standardization of input pulses.

Among the special purpose units available in the 1000 Series are dual and quadruple flip-flop packages for register applications, several different diode gates and special gates (such as the binary-to-octal decoder and parity circuit), delay lines, a crystal clock, and multiple-output pulse amplifiers. There are also a number of signal conversion devices and special amplifiers in this speed line.

DEC Standard Levels, used in all Digital Modules for performing logical gating functions, are 0 and −3 volts. DEC Standard Negative Pulses, used for sampling logic levels, are 2.5 volts in amplitude. The pulse width, which is commensurate with the speed line, is 70 nanoseconds in the 1000 Series. Other pulses may be used if they meet the requirements outlined in the Type 1607 Pulse Amplifier catalog sheet.

DEC STANDARD 70 NANOSECOND NEGATIVE PULSE



DEC TYPE 1201 FLIP-FLOP OUTPUT

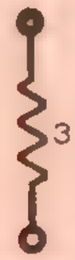
digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

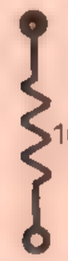
1000-1001-1002
CLAMPED LOAD RESISTORS

−3 VOLT CLAMP LOAD RESISTORS

1000 (PINS E - T)



1001 (PINS E - Z)



1002 (PINS E - Z)

The Types 1000, 1001 and 1002 are for use where extra standard loads, special lighter loads, or −3 volt sources are required.

The Type 1000 contains twelve standard clamped load resistors of 1500 ohms each. These may be used for clamping the voltage at the output of inverter collectors. A standard clamped load resistor presents 1 unit of DC Emitter Load when held at ground by an inverter. When not held at ground, the load resistor can drive 7 units of Base Load. (Output pins are E-T.)

The Type 1001 contains eighteen light clamped load resistors of 3000 ohms each. The load presented by a 3000-ohm resistor is ½ unit of DC Emitter Load. The driving capabilities are 3 units of Base Load. (Output pins are E-Z.)

The Type 1002 contains eighteen light clamped load resistors of 10,000 ohms each. These are particularly useful where a clamp which presents a light load is required, as in exclusive OR circuits. The load presented is 1/6 unit Emitter Load. The driving capability is 1 unit Base Load. A DEC inverter or diode gate can supply two Type 1002 resistors as well as a full unit of DC Emitter Load, providing this is in accordance with the rules for maximum series configurations for the specific gate used.

POWER: Type 1000: −15 volts/142 ma; Type 1001: −15 volts/134 ma; Type 1002: −15 volts/40 ma.

CLAMPING LOGIC LEVELS

Standard clamped load resistors are used to establish the voltage level whenever a level gate output is required to drive inverter base inputs. They are also used whenever a level gate or a number of level gates are used to condition the emitter of a pulse gate. The 3000-ohm or 10,000-ohm clamped load resistor may be used for this latter purpose with 1000 Series Modules, if desired. A 1500-ohm load must be used with the 4000 Series Modules. Figures 1 and 2 illustrate these uses.

Any of the clamped load resistors may be used to permanently enable the level input to a negative capacitor-diode gate, Types 4125, 4127 and 4129. A 10,000-ohm clamped load resistor is used whenever it is desired to have the output of a level gate drive both an Emitter Load and a Base Load. Figure 3 illustrates how the 10,000 clamped load resistor is used in a parity circuit. The maximum series configuration is three inverters or one inverter and one two-input diode gate. When the emitter of an inverter is driven by a flip-flop output, the flip-flop must be counted as an inverter.

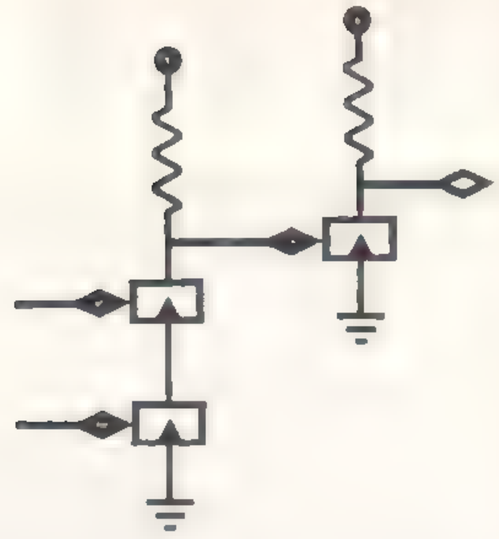


Figure 1 — SERIES INVERTER STRING DRIVING INVERTER BASE

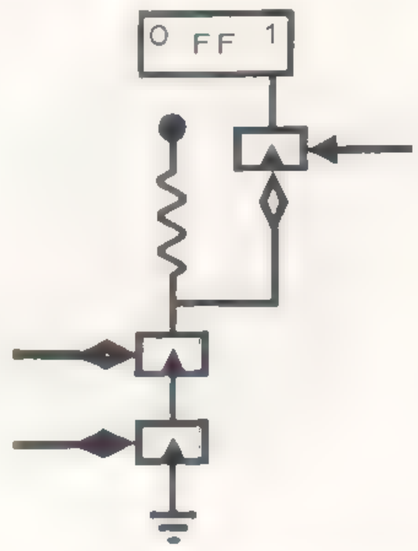


Figure 2 — SERIES INVERTER STRING DRIVING EMITTER OF PULSE GATE

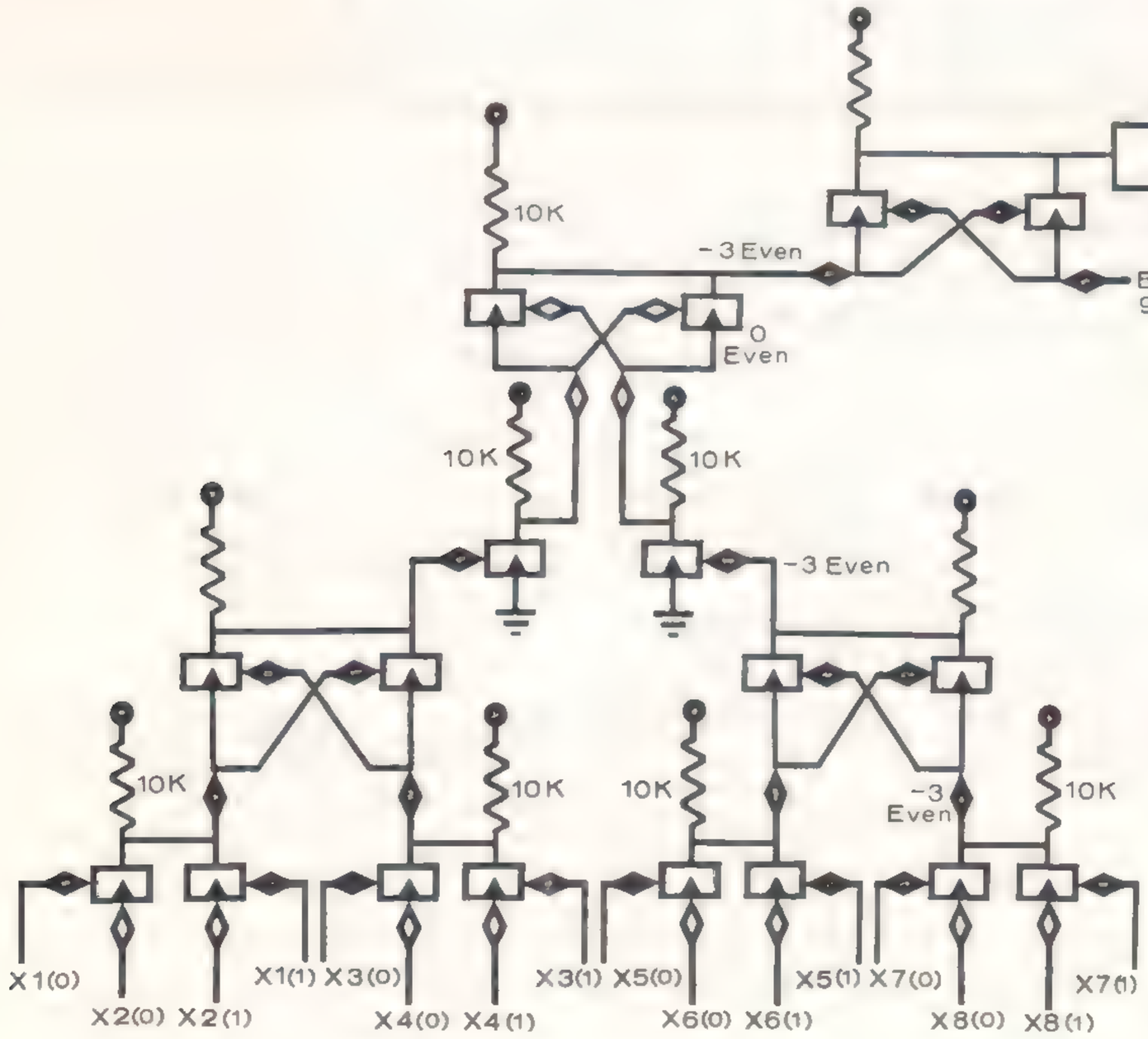
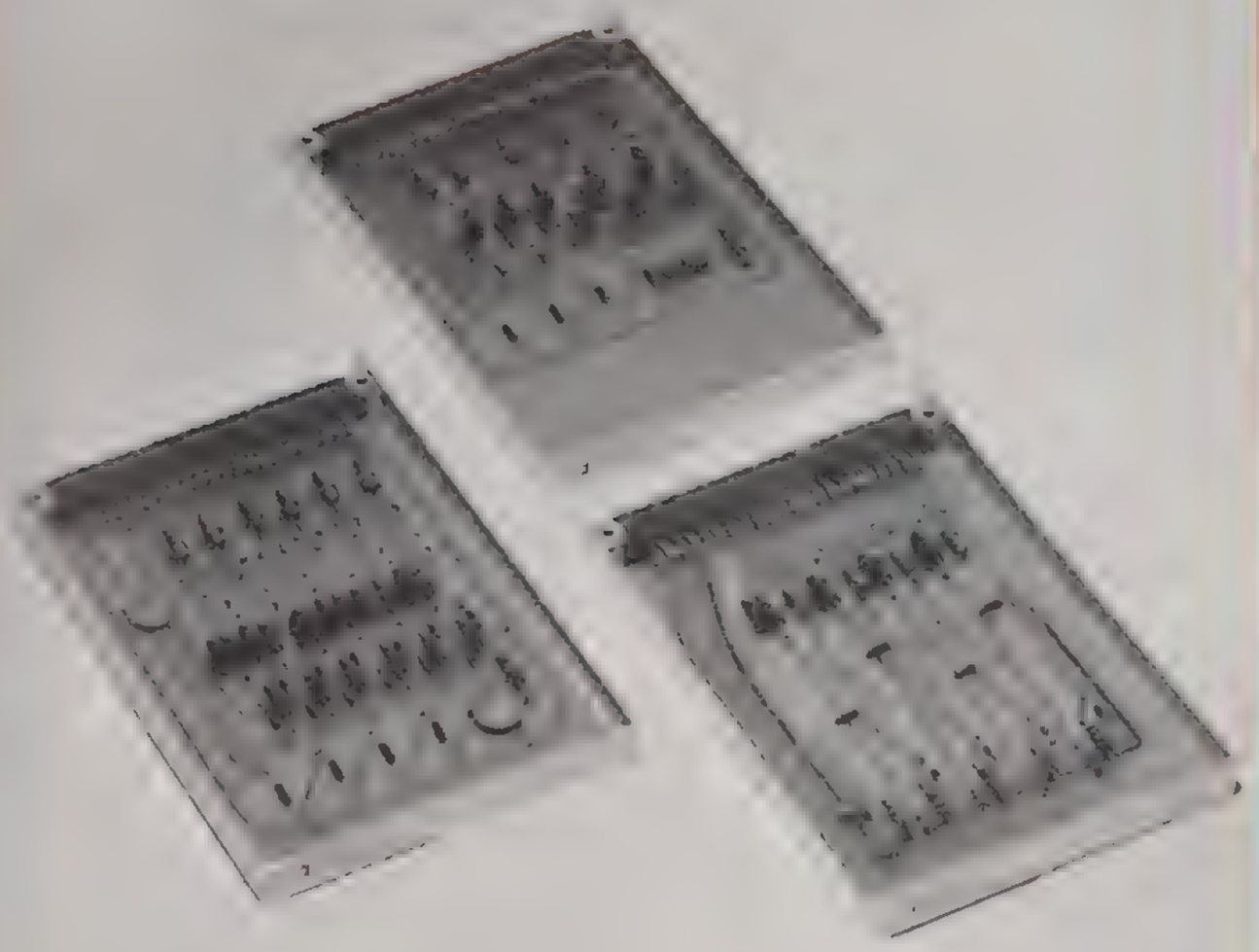


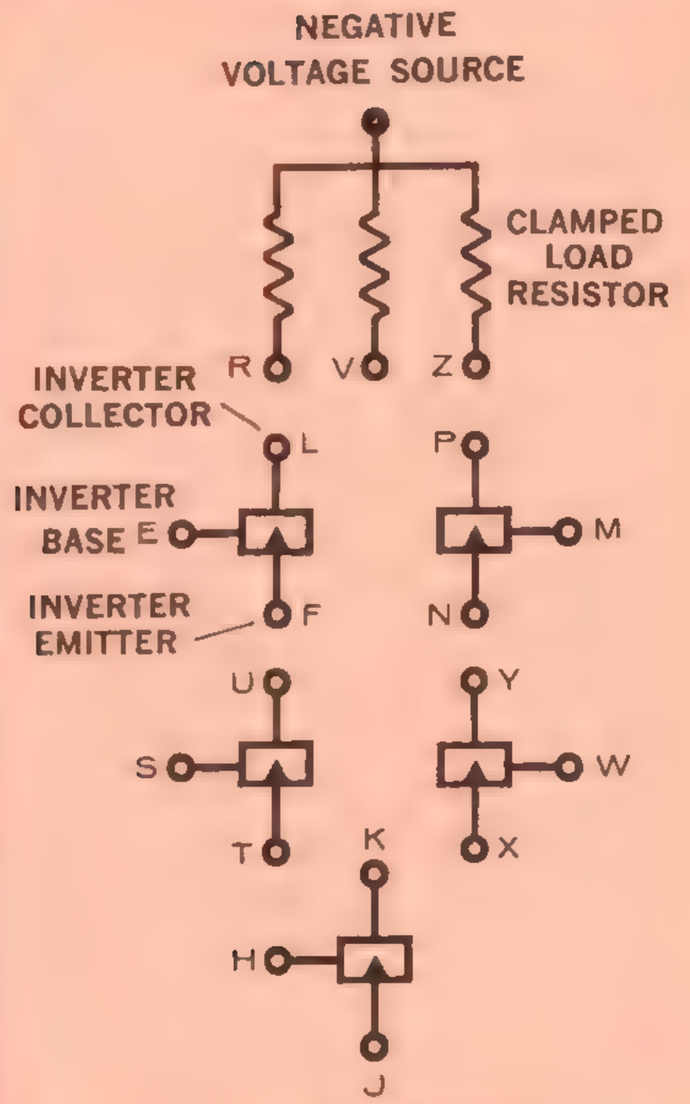
Figure 3 — PARITY CIRCUIT

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1103 -1104 -1105
INVERTERS





1105 INVERTER

The Types 1103, 1104 and 1105 contain transistor inverters for use as pulse gates or level gates. The Type 1103 has six inverters; the Type 1104 has four; and the Type 1105 has five. The clamped load resistors are available at output pins of the Types 1104 (4 resistors) and 1105 (3 resistors). The six clamped load resistors in the Type 1103 may be internally jumpered to the inverter collectors as needed. The load resistors are all clamped to −3 volts. Delay through each inverter is approximately 20 nanoseconds.

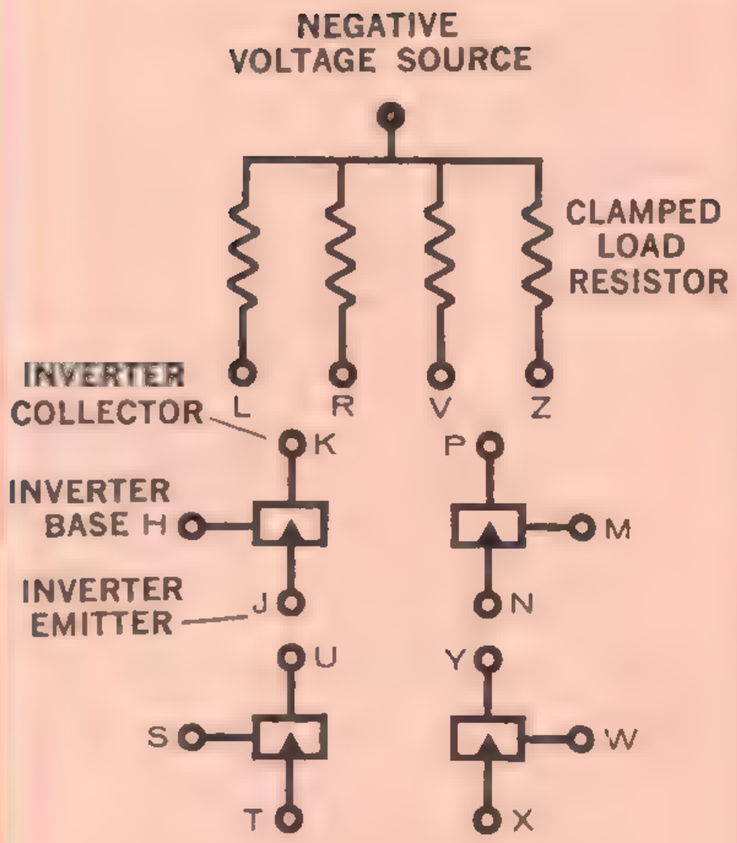
INPUT: Base — DEC Standard 70 nanosecond Negative Pulses drive the inverter at any frequency up to 5 megacycles (1 unit of Pulse Load) when it is used as a pulse gate. As a level gate (1 unit of Base Load), the inverter uses DEC Standard Levels or the equivalent. **Emitter** — The inputs are DEC Standard Levels or the equivalent, including ground if emitter gating is not desired. When the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles, or 7 where speed is not a problem, and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters, providing there is not more than one simultaneous emitter-collector path to a DC Emitter Load or to the pulse input of a flip-flop or other unit being pulsed. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

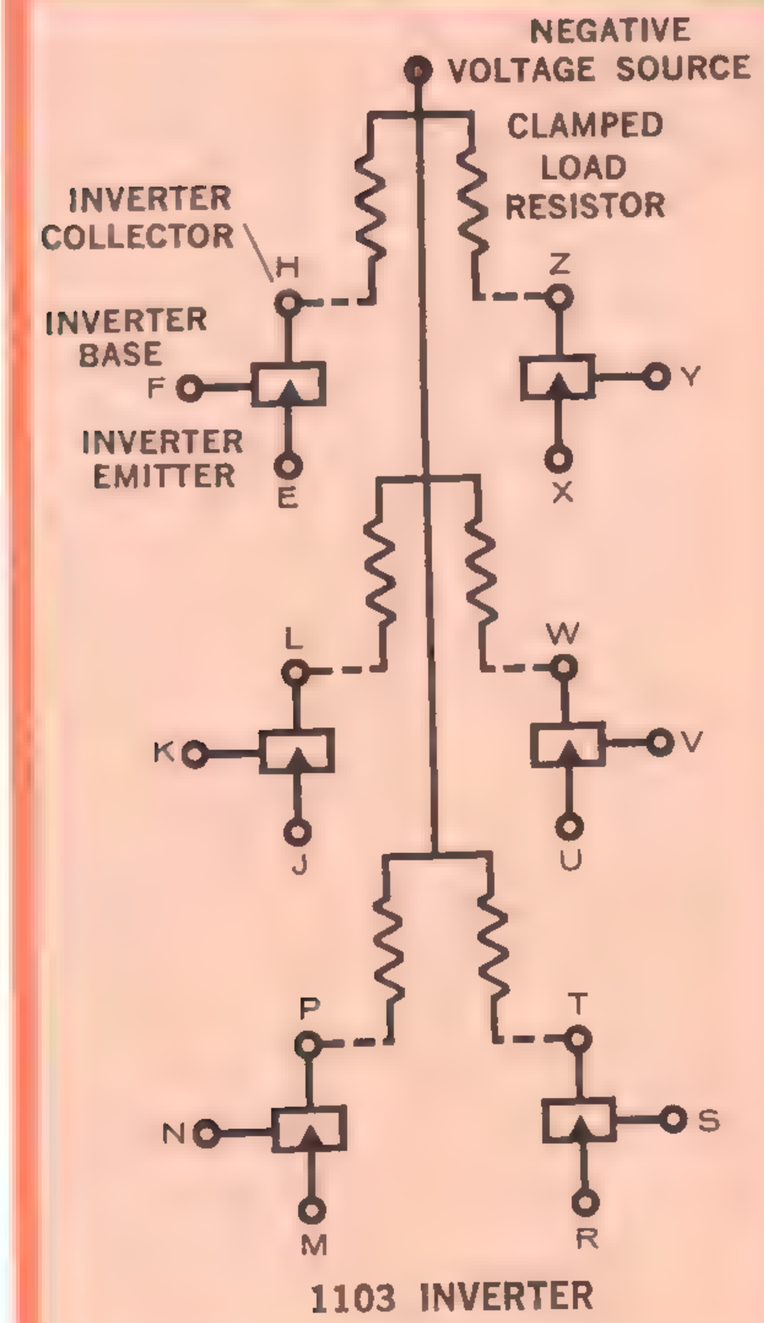
POWER: Type 1103: +10 volts (A)/0.9 ma; +10 volts (B)/0 ma; −15 volts/82 ma.

Power Type 1104: +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma; −15 volts/62 ma. Type 1105: +10 volts (A)/0.3 ma; +10 volts (B)/0.5 ma; −15 volts/52 ma.

Additional information on 5 megacycle inverter usage is included on the Type 103 catalog sheet.



1104 INVERTER

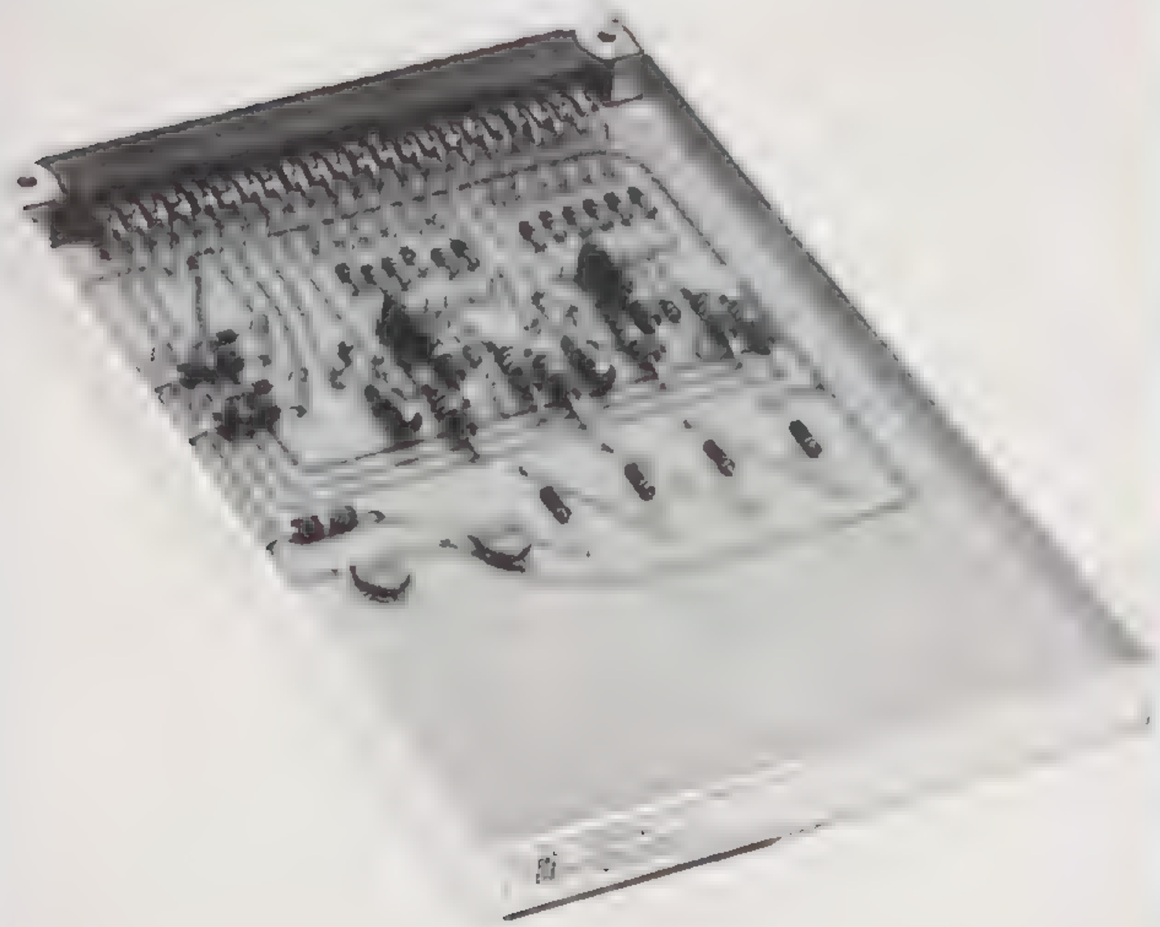


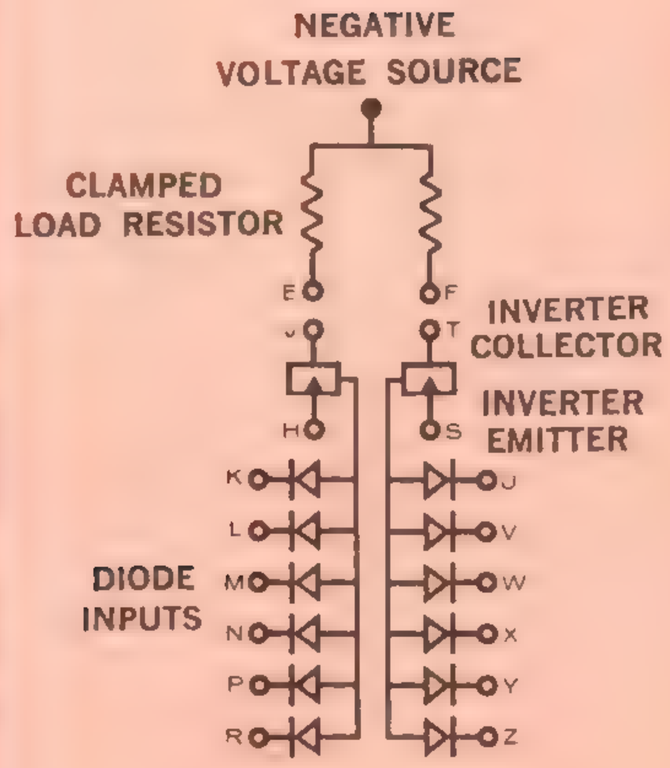
1103 INVERTER

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1110
DIODE





The Type 1110 consists of 2 six-input diode gates, each gate being connected to the base of a transistor inverter similar to a DEC Inverter Type 1105. The gates serve as OR circuits for negative level inputs and AND circuits for ground inputs. The gates may also be used to mix pulses. The emitter and collector of each transistor are available for external connections. Delay of a level through a diode and its inverter is approximately 30 nanoseconds.

INPUT: Diodes — DEC Standard Levels, DEC Standard 70 nanosecond Negative Pulse or the equivalent, will supply the input. When the diodes are used as a level gate, the load is three units of Base Load shared among those inputs which are at a negative voltage. When the diodes are used for pulse mixing, each input is 1 unit of Pulse Load. Emitter — DEC Standard Levels or equivalent drive the inverter emitter; the emitter may be grounded if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, the load on the emitter is 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, the load on the emitter is 1 unit of Pulsed Emitter Load.

OUTPUT: The inverter collector may be connected directly to a clamped load resistor, to the emitter of an inverter, or to the gated input terminal of a flip-flop or other unit being pulsed. When used as a pulse mixer, a diode gate can drive one input to a flip-flop or other pulsed unit. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem); and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

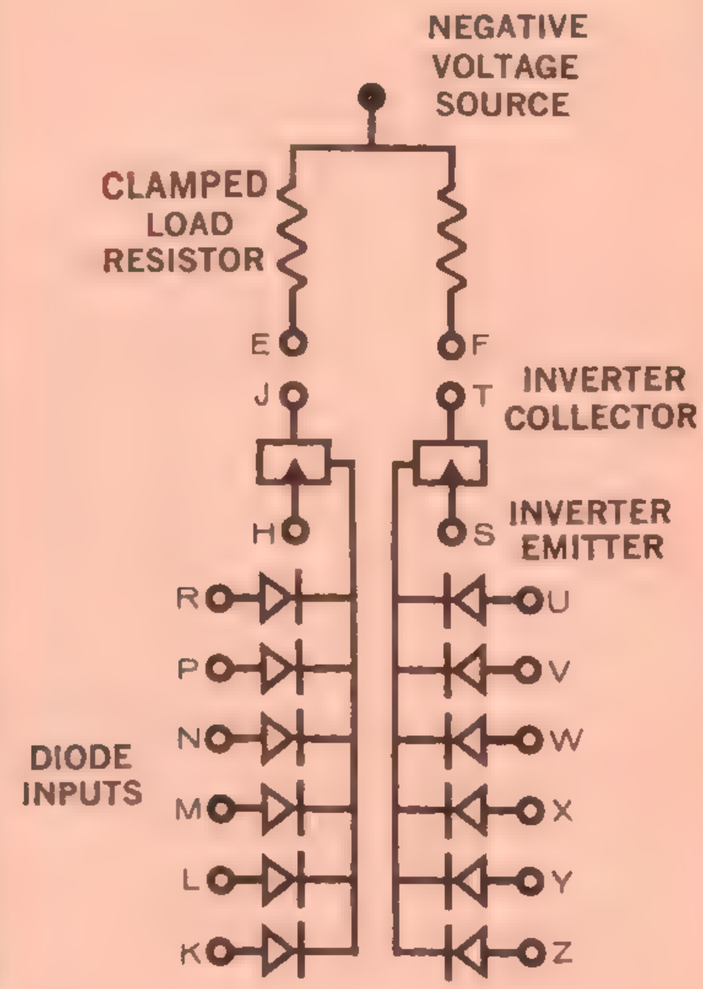
A collector with no clamped load can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: −15 volts/42 ma; +10 volts (A)/1.3 ma; +10 volts (B)/1.3 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1111
DIODE



The Type 1111, like the Type 1110, contains 2 six-input diode gates, each connected to the base of a transistor inverter; however, this unit is an OR circuit for ground level inputs and an AND circuit for negative inputs. The emitter and collector of each inverter are available for external connections. Delay of a level through a diode and its inverter is approximately 30 nanoseconds.

INPUT — DEC Standard Levels or equivalent supply the input to the diodes; the load is ⅛ unit of DC Emitter Load shared by the ground inputs. This unit may not be used for gating pulses. Emitter — DEC Standard Levels or equivalent drive the inverter emitter; the emitter may be grounded if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, the load on the emitter is 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, the load on the emitter is 1 unit of Pulsed Emitter Load.

OUTPUT The inverter collector may be connected directly to a clamped load resistor or to the emitter of another inverter. A collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem) and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

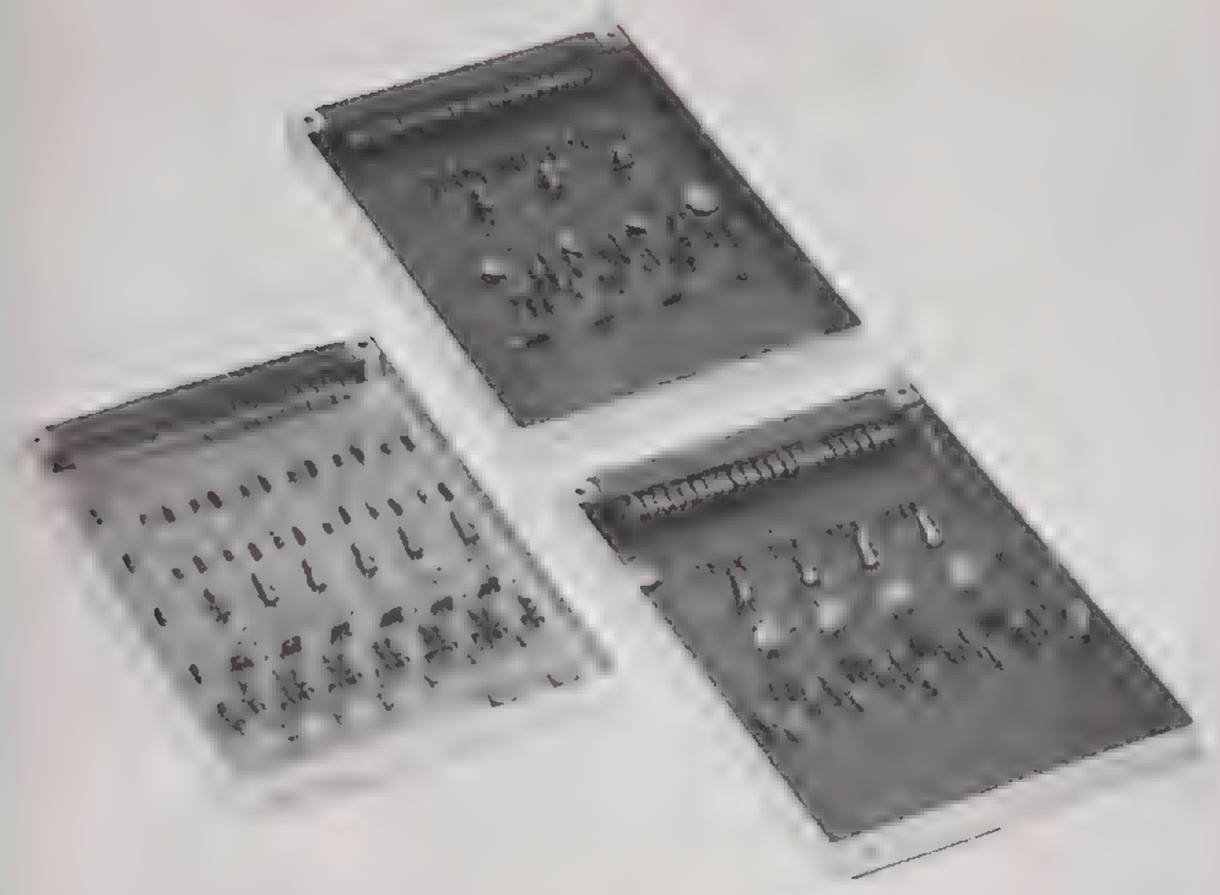
A collector with no clamped load can be connected to several emitters simultaneously, provided not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected inverters is used as a pulse gate, four gates may be connected in series.

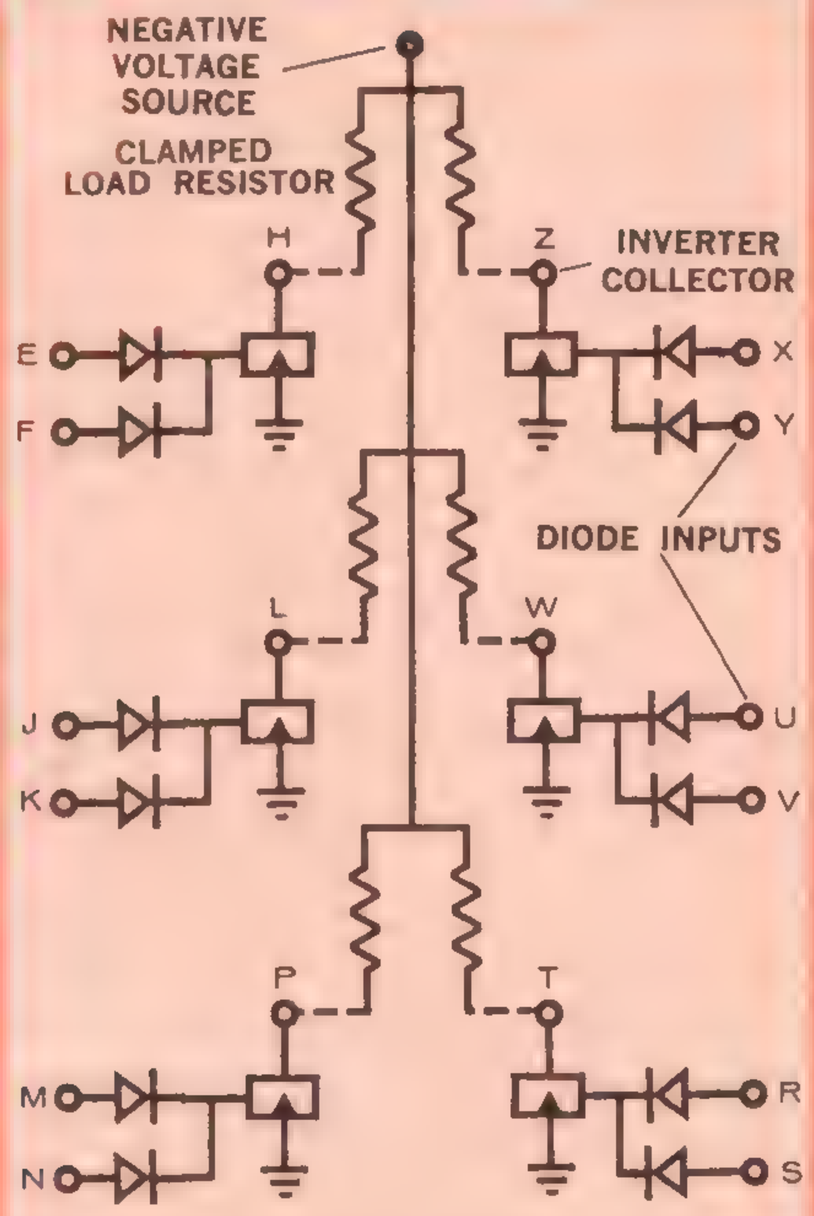
POWER: −15 volts/45 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1113-1115-1117
DIODE





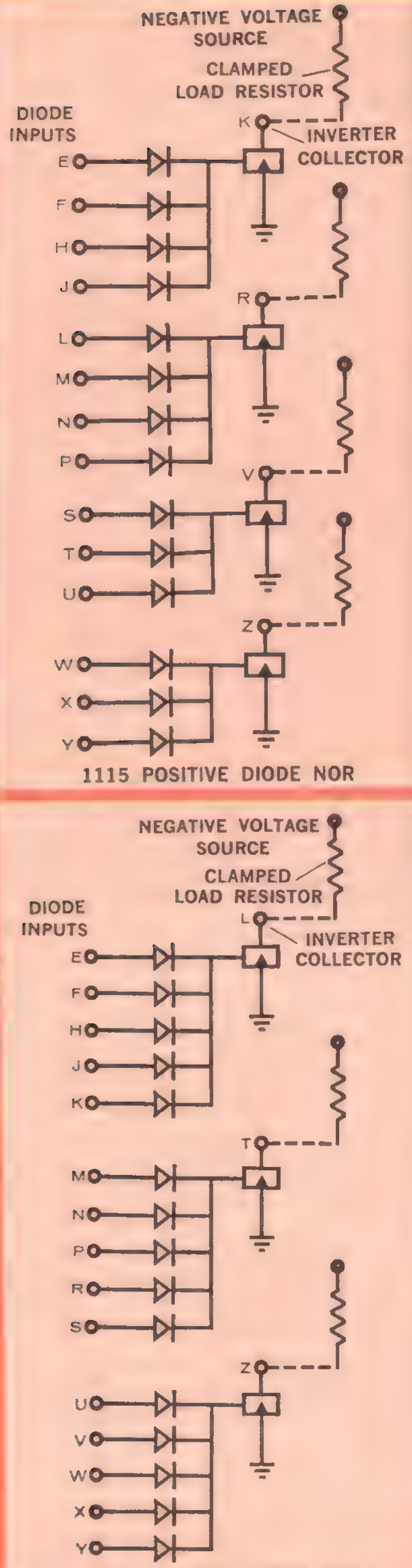
1113 POSITIVE DIODE NOR

These diode gates are OR circuits for ground level inputs and AND circuits for negative level inputs. Each diode gate is connected to the base of a transistor inverter with a grounded emitter. Clamped load resistors are available and may be internally jumpered to the transistor collectors. Total transition time for output fall is 90 nanoseconds; for output rise, 50 nanoseconds. The Type 1113 contains 6 two-input diode gates; the Type 1115, 2 three-input, and 2 four-input diode gates; and the Type 1117, 3 five-input diode gates.

INPUT: DEC Standard Levels or equivalent are used for the inputs. The DC load presented by the inputs is ⅛ unit of DC Emitter Load. This load is shared by those inputs which are at ground.

OUTPUT: The collector may be connected directly to a clamped load resistor or to the emitter of another inverter. When used as a level gate, a collector connected to a clamped load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem;) and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters, provided there is not more than one simultaneous emitter-collector path to a DC Emitter Load or to the pulse input of a flip-flop or other unit being pulsed. No more than 2 level gates can be connected in series with a diode gate. When one of the series-connected gates is used as a pulse gate, 3 gates may be connected in series.

POWER: Type 1113 −15 volts/88 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma. Type 1115 −15 volts/67 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. Type 1117 −15 volts/55 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.15 ma.



1115 POSITIVE DIODE NOR

1117 POSITIVE DIODE NOR

GE
OR
INVERTER
OLLECTOR
OR
VERTER
LECTOR
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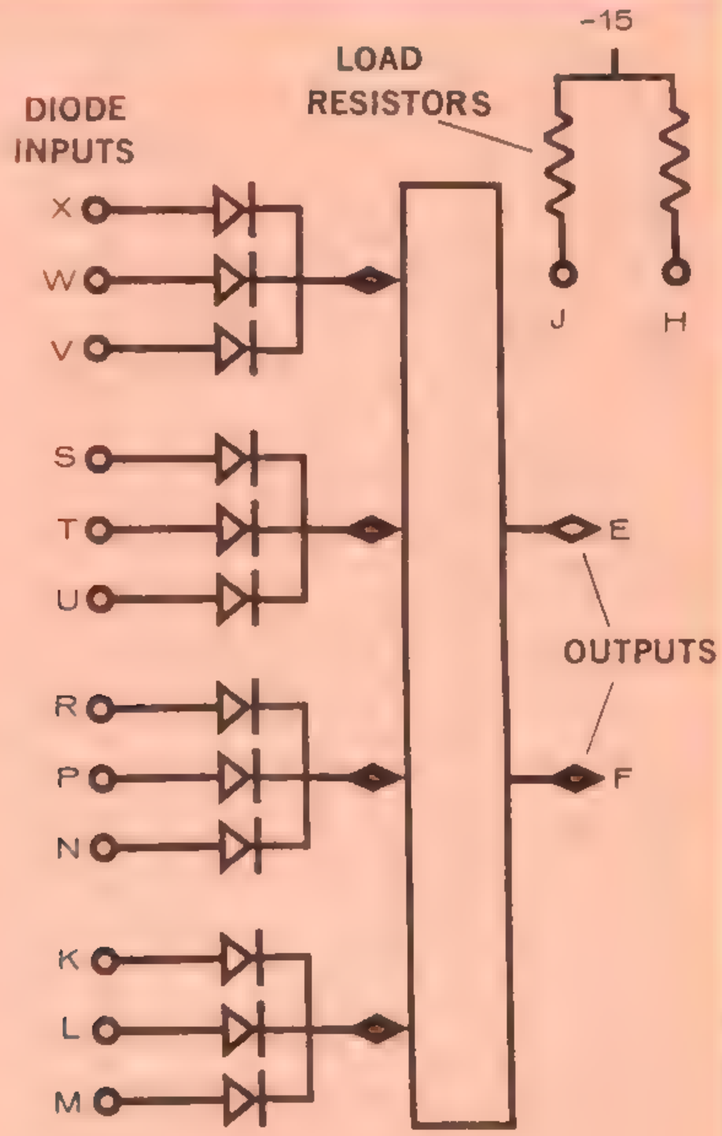
digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1130
THREE-BIT PARITY CIRCUIT



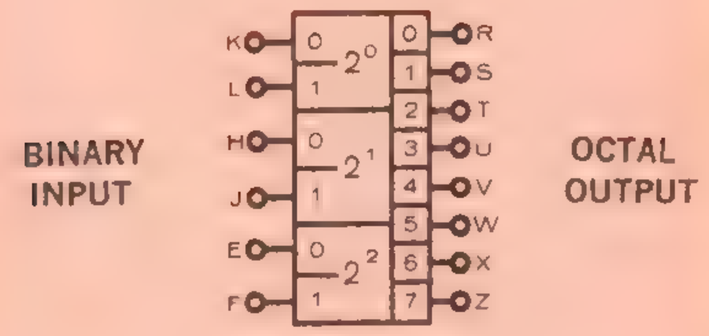
Four three-input negative AND gates are OR'ed together to produce a circuit that is principally used for determining the parity of three binary bits. Units may be cascaded in a pyramid arrangement to determine parity of larger number of bits. Both polarity outputs are available. Delay is approximately 25 nanoseconds with light output loading.

INPUT: The inputs used are DEC Standard Levels or equivalent. Each three-input AND gate represents ½ unit of DC Emitter Load shared among those inputs which are at ground. (When this unit is used as a parity circuit with three sets of complementary level inputs, the maximum load presented to any input is ¾ unit of DC Emitter Load.)

OUTPUT: The Complementary DEC Standard Levels are produced at the output. When all inputs to any AND gate are negative, output pin F will be −3 volts and output pin E will be ground. Each output is capable of driving the input to Type 1130 used as a parity circuit, plus 7 units of Base Load, if speed is no problem. For maximum speed, the load should be restricted to one Type 1130 used as a parity circuit and 4 units of Base Load. If no Type 1130's are driven by the output, the two resistors available on the package may be connected to the outputs to increase the base driving ability. Each output is then capable of driving 12 units of Base Load where speed is no problem, or 7 units at high speed operation.

POWER: −15 volts/77 ma; +10 volts (A)/16 ma; +10 volts (B)/30 ma. The +10 volt (B) terminal should be connected to a fixed voltage supply. To avoid extreme power dissipation, the +10 volt (B) terminal voltage should not be increased significantly (as in marginal checking).

1150-1151
BINARY-TO-OCTAL DECODER



These units enable binary information in three flip-flops to be decoded into octal form. For the Type 1150, the selected output line is at −3 volts, and the other seven outputs are at ground. For the Type 1151, the selected output line is at ground, while the other seven outputs are at −3 volts.

Decoding is accomplished with 8 three-input diode gates arranged so that each diode gate has a unique set of inputs. For the Type 1150, the diode gates are similar to those in the Type 1110. For the Type 1151, the diode gates are similar to those in the DEC Type 1111.

The total transition time is less than 60 nanoseconds for the Type 1150 and less than 90 nanoseconds for the Type 1151.

INPUT: Type 1150: DEC Standard Levels or equivalent drive the decoder which represents 5 units of Base Load. If inputs L, J and F are at ground, output R is selected and is at −3 volts. **Type 1151:** DEC Standard Levels or equivalent drive the decoder which represents 0.3 unit of DC Emitter Load. If inputs K, H and E are at −3 volts, output R is selected and is at ground.

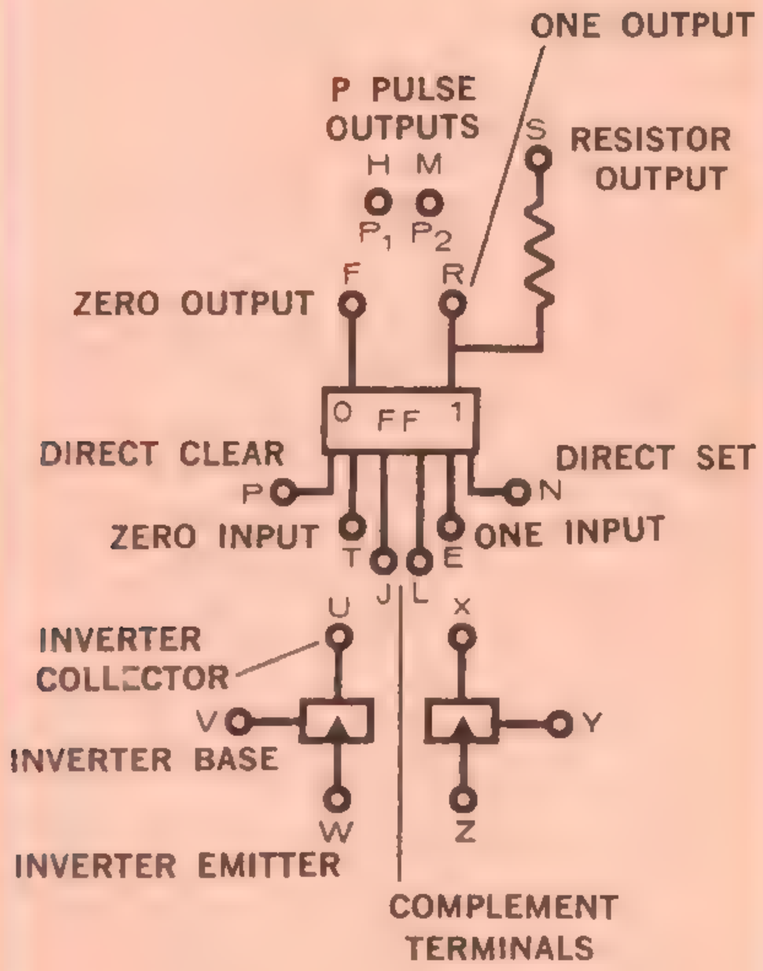
OUTPUT: Each output is a standard inverter collector, connected internally to a clamped load resistor. Each output can simultaneously drive: (A) 4 units of Base Load at 5 megacycles (7 where speed is not a problem), and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

POWER: Type 1150 — −15 volts/100 ma; +10 volts (A)/7 ma; +10 volts (B)/5.5 ma. **Type 1151** — −15 volts/88 ma; +10 volts (A) 1.2 ma; +10 volts (B)/0 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1201
FLIP-FLOP



The Flip-flop Type 1201 is basically a two-transistor static flip-flop with built-in output amplifiers, Direct Set and Clear inputs, Gated Set and Clear inputs, two sources of counting carry pulses (P Pulse), two Complement inputs, and two inverter gates. It has sufficient built-in gating to be used as one digit of a shift register, or one digit of a binary counter. It can also be used for all general type logical operations. It has a built-in delay so that its output terminals can be sensed at the same instant that an input terminal is being pulsed, which is very useful in counter, shift register, and adder applications. A resistor coupled output suitable for driving a transistor indicator amplifier is available.

INPUT: Direct Clear and Direct Set require DEC Standard 70 nanosecond Positive Pulses (1 unit of Pulse Load). ZERO input, ONE input, and the Complement inputs each must come from the collector of a pulse gate. More than one pulse gate can be connected to the same terminal. The above signals can occur in any sequence, at any frequency, and at any time intervals which have a minimum of 0.2 microsecond between any two signals. (Maximum frequency is 5 megacycles.) The two inverters are similar to those included in the DEC Inverter Type 1105.

OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving: (a) 10 units of Base Load at 5 megacycles or 14 units where speed is not a problem; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

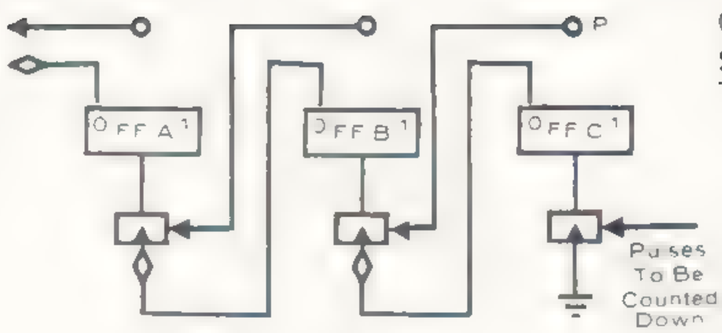
Each time the C_1 complement terminal is pulsed, a DEC Standard 70 nanosecond Negative Pulse, capable of driving 1 unit of Pulse Load, will occur on the P_1 terminal. P_2 and C_2 work the same way with respect to each other. Delay from the time the input inverter of either complement terminal is pulsed to the time the corresponding P Pulse occurs is approximately 20 nanoseconds.

POWER: −15 volts/64 ma; +10 volts (A)/1.3 ma; +10 volts (B)/1.3 ma.

TYPICAL APPLICATIONS

UP COUNTERS

A typical up counter arrangement is shown in Figure 1. The pulses being counted enter on the right. They always complement flip-flop C and generate a Standard Pulse at P. This pulse complements flip-flop B whenever flip-flop C's state previous to its complement was a ONE. When B is complemented, a P Pulse is generated out of B that complements A if B held a ONE before it was complemented. This process is continued up the length of the counter until a flip-flop in the ZERO state is reached.



COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 1 UP COUNTER

UP-DOWN COUNTERS

The binary up-down counter, shown in Figure 2, subtracts as well as adds, using the two independent sets of complement and P Pulse terminals. The C_1 and P_1 terminals are connected to form an up counter with a high speed carry chain, while the C_2 and P_2 form a down counter with a high speed borrow chain. Add and subtract pulses may arrive at any rate up to 5 megacycles. (i.e. There must be 0.2 microsecond between two pulses on either the same or opposite terminals.)

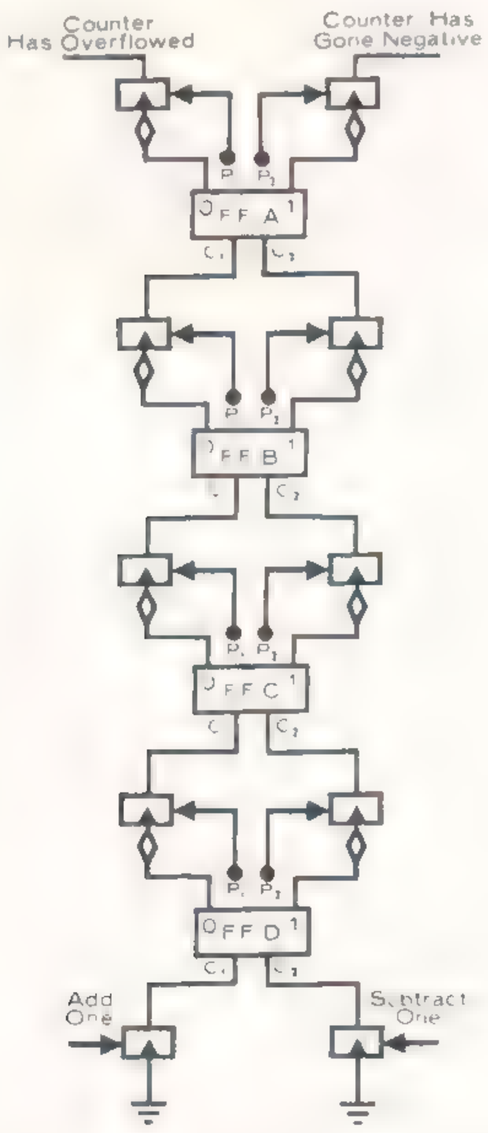
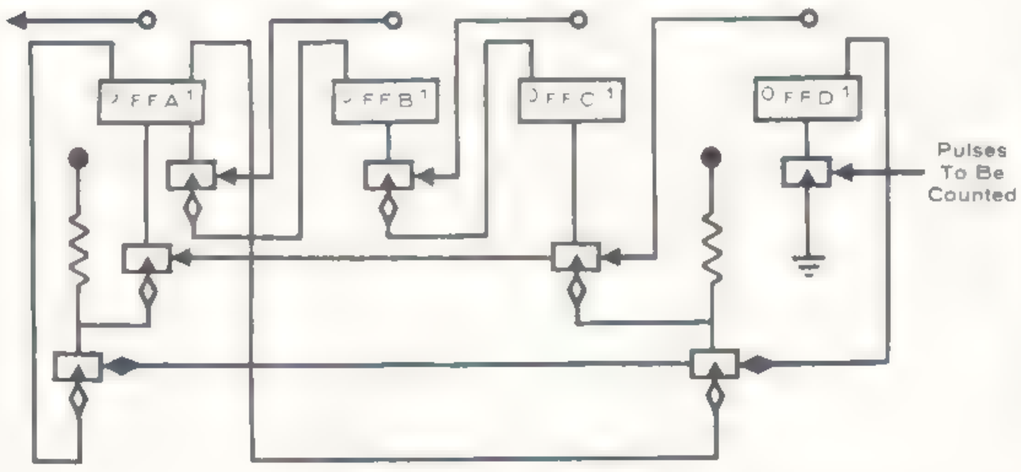


Figure 2 BINARY UP-DOWN COUNTER

BINARY CODED DECIMAL COUNTERS

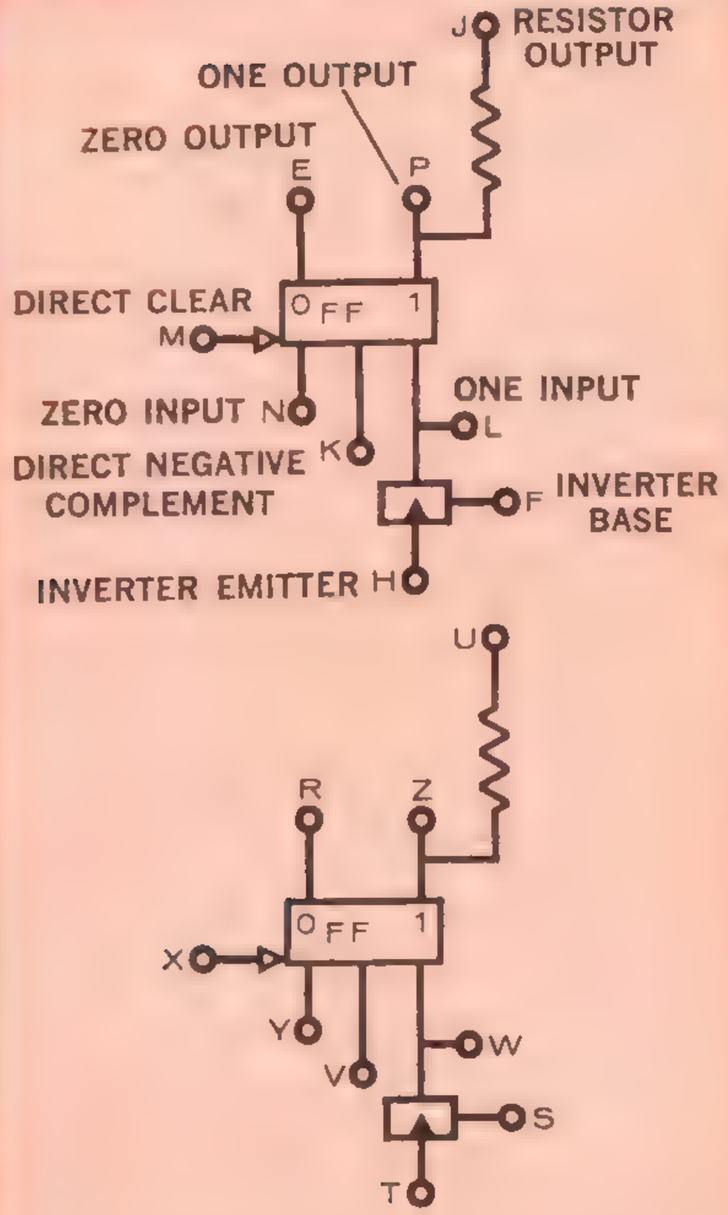
The binary coded decimal counter, shown in Figure 3, converts the inherent binary count of a counter to decimal digits. The counter counts to 8, as in a standard up counter, except no P Pulse is produced from flip-flop A. The count of 8 cuts off the path from flip-flop D to flip-flop C. The count of 9 establishes a path from the P output of flip-flop D to the complement terminal of flip-flop A. The 10th count complements both flip-flop D and flip-flop A; the P Pulse of flip-flop A indicates a count of 10, and all the flip-flops in the counter are in the ZERO state ready to count to 10 again.



COUNTING SEQUENCE	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Figure 3 BINARY CODED DECIMAL COUNTER

1204
DUAL FLIP-FLOP



The Type 1204 contains two identical flip-flops with built-in output amplifiers. Each flip-flop has a gated input to both the ZERO and ONE sides, a Direct Clear input, and a Direct negative Complement input. Each flip-flop has one pulse gate internally connected to the gated ONE input terminal. A resistor coupled output suitable for driving a transistor indicator amplifier is available. The output signals have built-in delays, so that they can be sensed reliably at the same time that the input is being pulsed.

INPUT: Direct Clear (pins M and X) requires DEC Standard 70 nanosecond Positive Pulse (1 unit of Pulse Load). Direct Negative Complement requires DEC Standard 70 nanosecond Negative Pulses (2½ units Pulse Load). The Gated Clear must come from one or more collectors of pulse gates. Gated Set is internally connected to the collector of the built-in pulse gate. Other pulse gate collectors can also be connected to this point. The two pulse gates are inverters like those included in the DEC Inverter Type 1105.

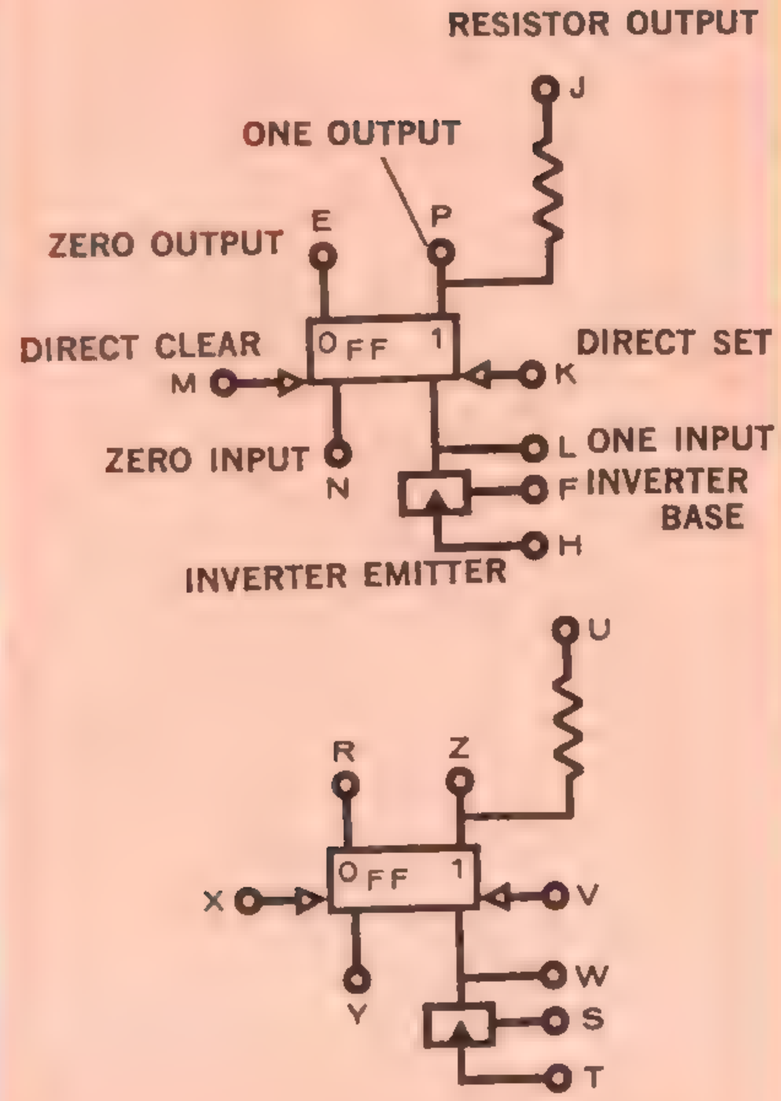
OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving: (a) 10 units of Base Load at 5 megacycles, 14 units where speed is not a problem; (b) 1 unit of DC Emitter Load; (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

POWER: −15 volts/108 ma; +10 volts (A)/2.4 ma; +10 volts (B)/2.4 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1209
FLIP-FLOP



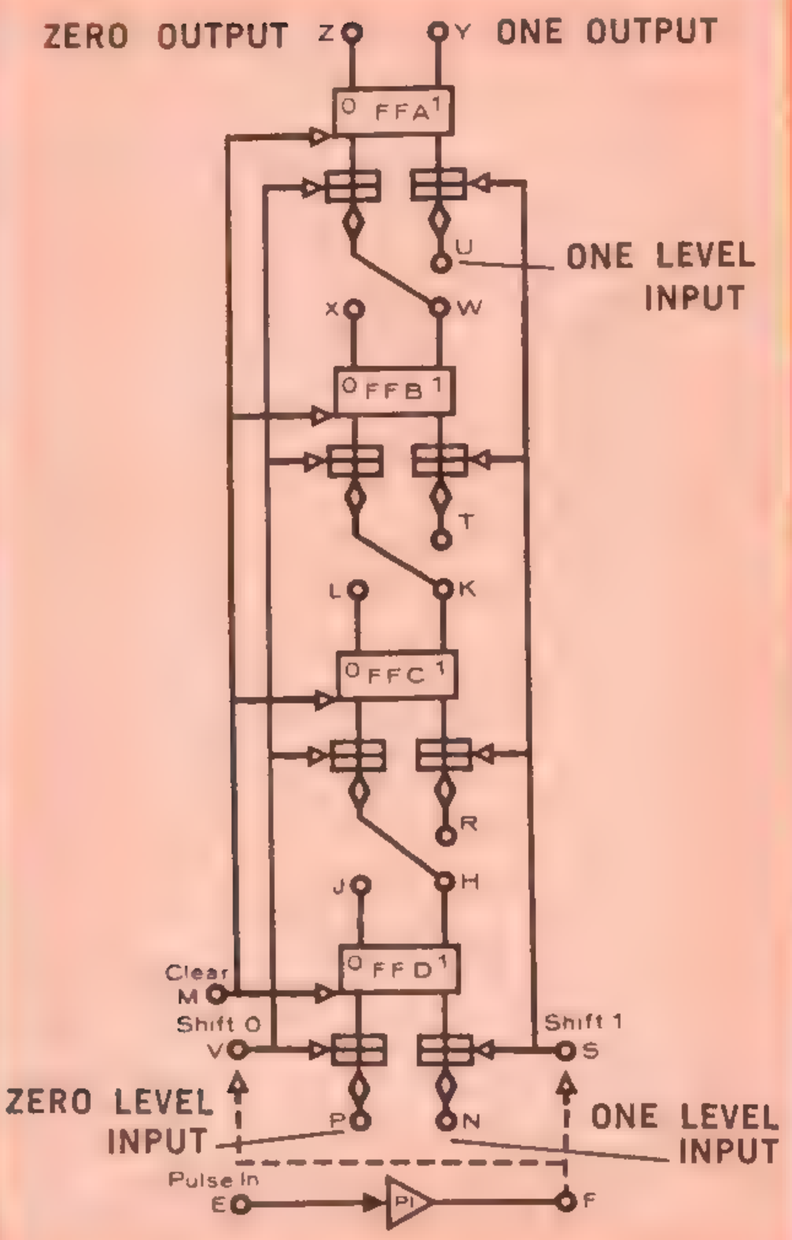
The Type 1209 contains two identical flip-flops with built-in output amplifiers. Each flip-flop has a direct and a gated input to the ZERO and ONE side. Each flip-flop has one pulse gate internally connected to the gated ONE input terminal. A resistor coupled output suitable for driving a transistor indicator amplifier is available. The output signals have built-in delays, so that they can be sensed at the same instant they are pulsed. This is particularly useful in shift register applications.

INPUT: Direct Clear and Direct Set require DEC Standard 70 nanosecond Positive Pulses (1 unit of Pulse Load). Gated Clear must come from one or more collectors of pulse gates. Gated Set is internally connected to the collector of the built-in pulse gate. Other pulse gate collectors can also be connected to this point. The two pulse gates are inverters like those included in the DEC Inverter Type 1105.

OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving: (a) 10 units of Base Load at 5 megacycles or 14 units where speed is not a problem; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

POWER: −15 volts/108 ma; +10 volts (A)/2.4 ma; +10 volts (B)/2.4 ma.

1213
QUADRUPLE FLIP-FLOP



The Type 1213 contains four flip-flops with associated gates for connection as a shift or buffer register. A pulse inverter is included for driving the capacitor-diode gates during either a read-in or a shift operation. The flip-flops can be individually set or cleared by connecting pulse gates (such as DEC Type 1105 inverters) to the proper output terminals. The maximum operating frequency is 3 megacycles.

INPUT: Pulse Inverter Input — A DEC Standard 70 nanosecond Negative Pulse (1 unit of Pulse Load). **Clear Input** — A DEC Standard 70 nanosecond Positive Pulse (1 unit of Pulse Load per flip-flop). Clear pulses may precede read-ins by as little as 0.2 microsecond. **Shift One** and **Shift Zero Inputs** — May be driven only by the output of the included pulse inverter. **Level Inputs** — Are DEC Standard Levels or equivalent (ground for assertion). There is no DC Load at these points. The transient load approximates 1 unit of Base Load. The level must be present at least 0.3 microsecond before a shift operation and 0.5 microsecond before a read-in operation. The flip-flops may be set or cleared by connecting an inverter to the appropriate output terminal. The emitter of the inverter must be permanently grounded. When the inverter is pulsed the flip-flop output to which it is connected is grounded.

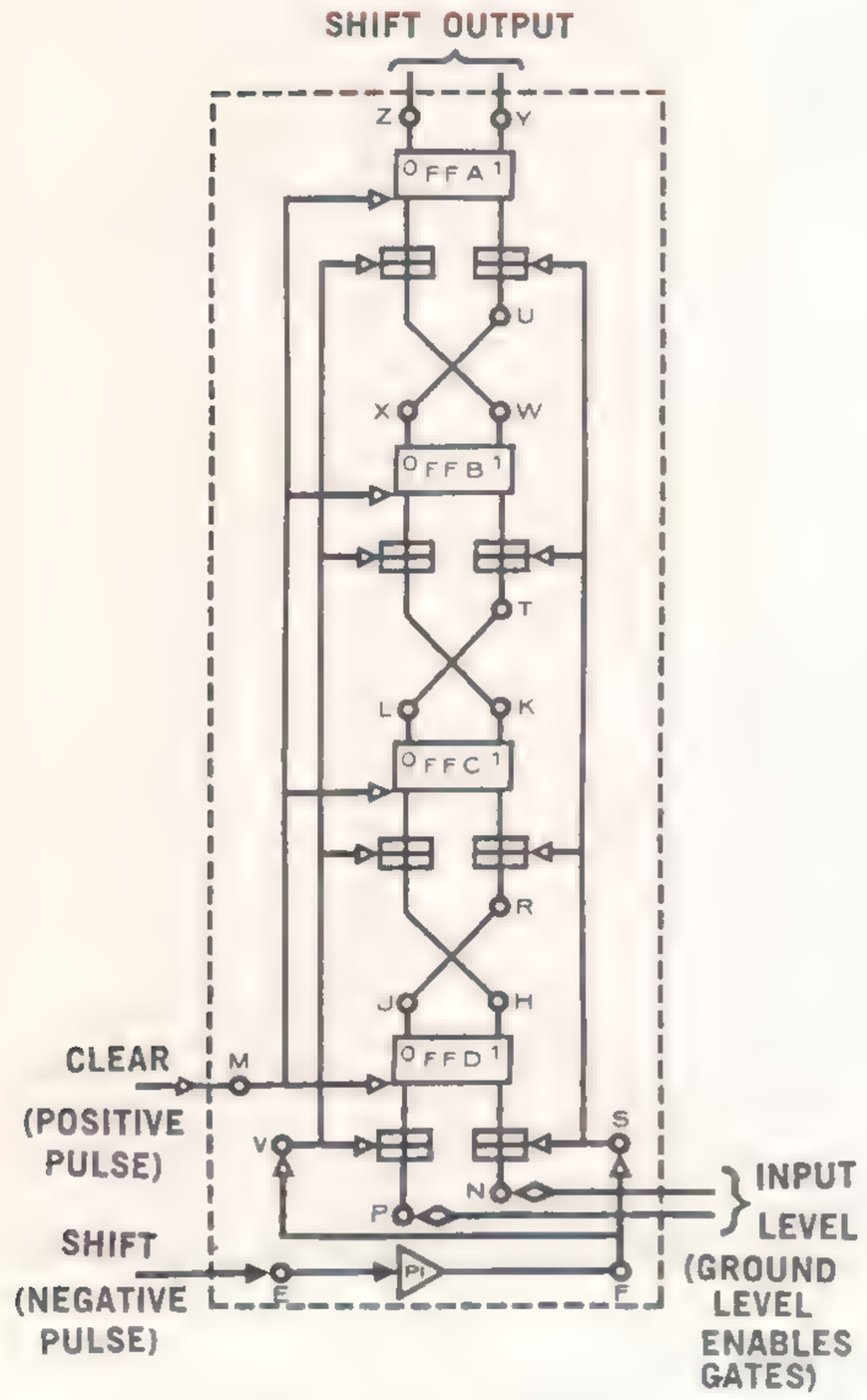
OUTPUT: One Output and **Zero Output** from each flip-flop provide DEC Standard Levels each capable of simultaneously driving: a) 2 units of Base Load and b) 1 capacitor-diode gate level input. The outputs are unbuffered and the delay is; therefore, short compared to the 70 nanosecond pulse width. When the flip-flop output is to be sampled and changed at the same time, provision must be made for a logical delay. This delay may be provided by the use of a capacitor-diode gate or three cascaded inverters.

Pulse Inverter Output — A positive 3 volt pulse from a DC level of −3 volts. This can only drive the Shift 1 and/or the Shift 0 gates included in the plug-in unit.

POWER: −15 volts/98 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

TYPICAL APPLICATIONS

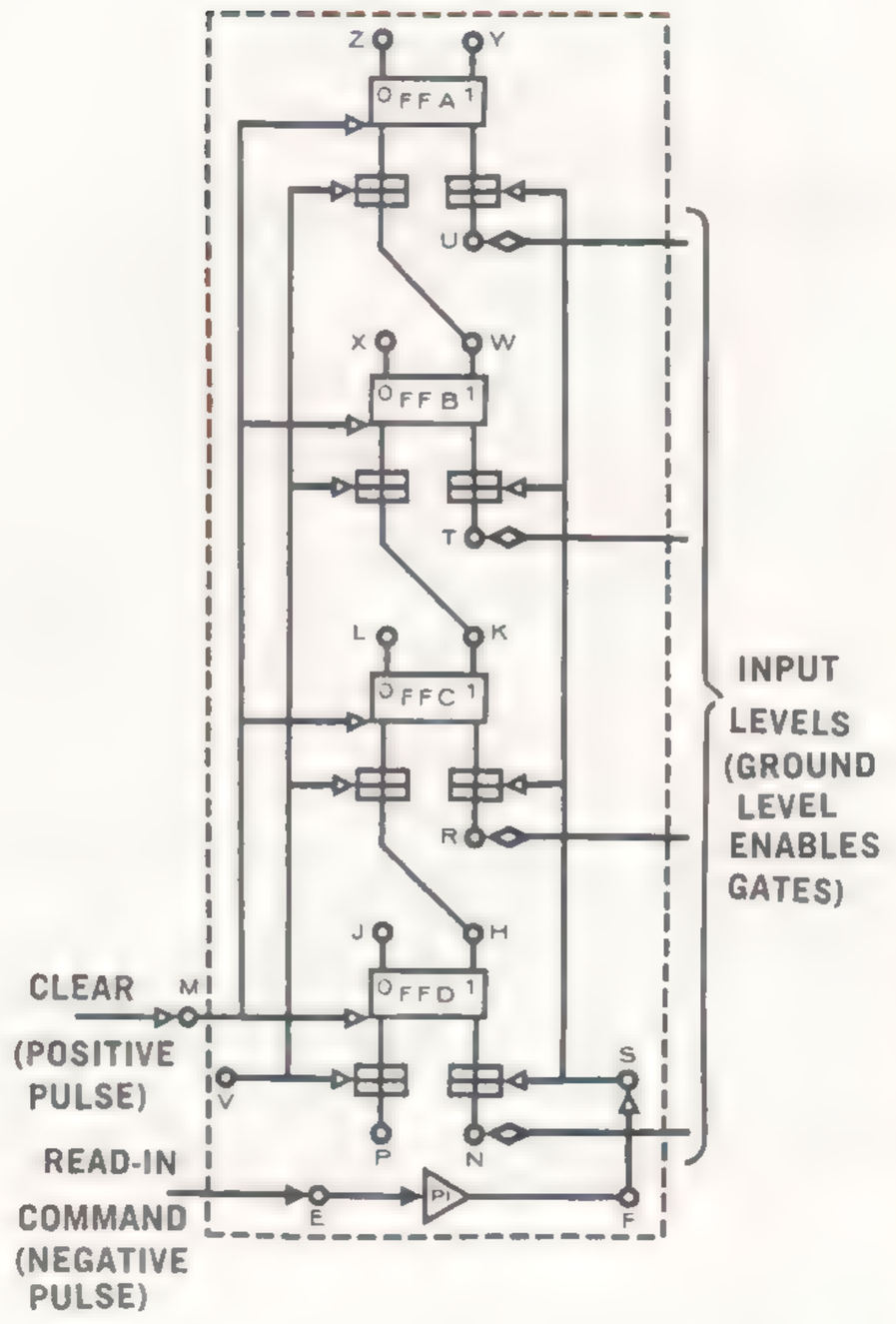
SHIFT REGISTER



SHIFT REGISTER APPLICATION

When connections are made as shown each Flip-Flop controls the level inputs to the capacitor-diode gates in the next Flip-Flop in the shift register. For this application the Pulse Inverter output is connected to both the Shift 1 and Shift 0 terminals. The contents of the Flip-Flops will advance one Flip-Flop upward for every input pulse. Maximum shift PRF is 3 MC.

BUFFER REGISTER

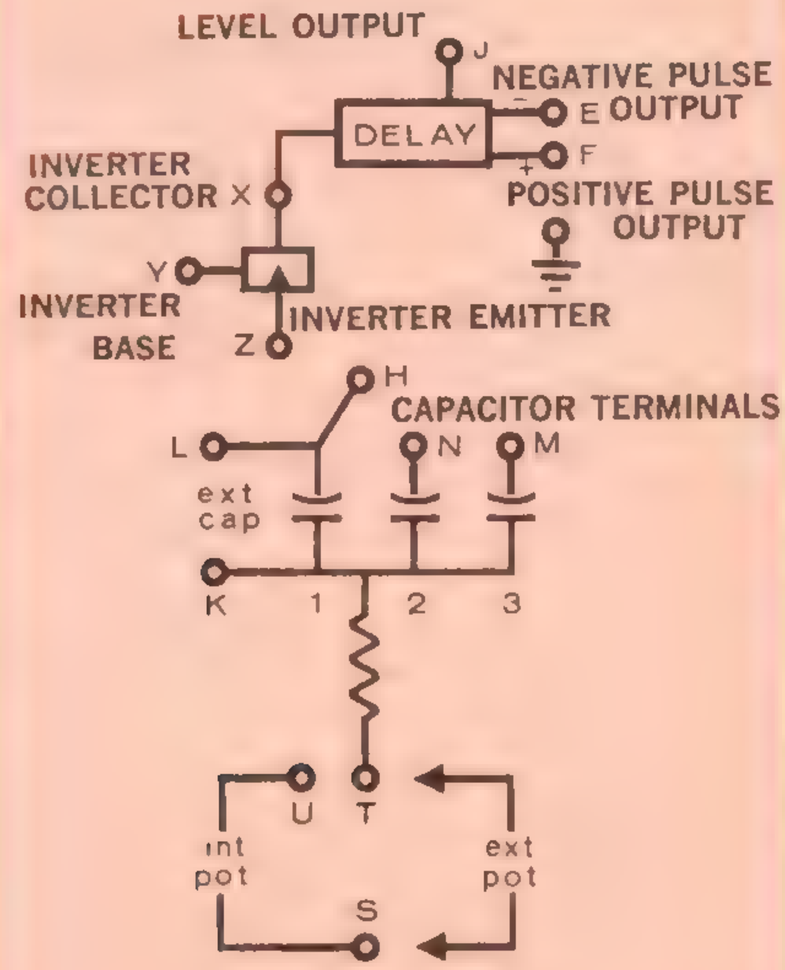


BUFFER REGISTER APPLICATION

When used as a buffer register, the Pulse Inverter output is connected to the Shift 1 terminal only. The input levels are connected to the ONE input gates as shown. A ground level enables the gates. The gating level must be present at least 0.5 microsecond before the Read In pulse. The common Clear input is pulsed with a positive pulse to clear the entire register before reading in a new word. The Clear may precede the Read In by as little as 0.2 microsecond.

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1304
DELAY (ONE SHOT)



The Type 1304 delay unit is a mono-stable multivibrator. When the input terminal is grounded, either through the inverter or externally, the level output terminal will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time and then back to ground. A pulse transformer generates a DEC Standard 70 nanosecond Pulse at the pulse output during the final transition. The pulse transformer has both positive and negative terminals so that either polarity pulse may be obtained. Typical output and input wave forms are shown in Figure 1.

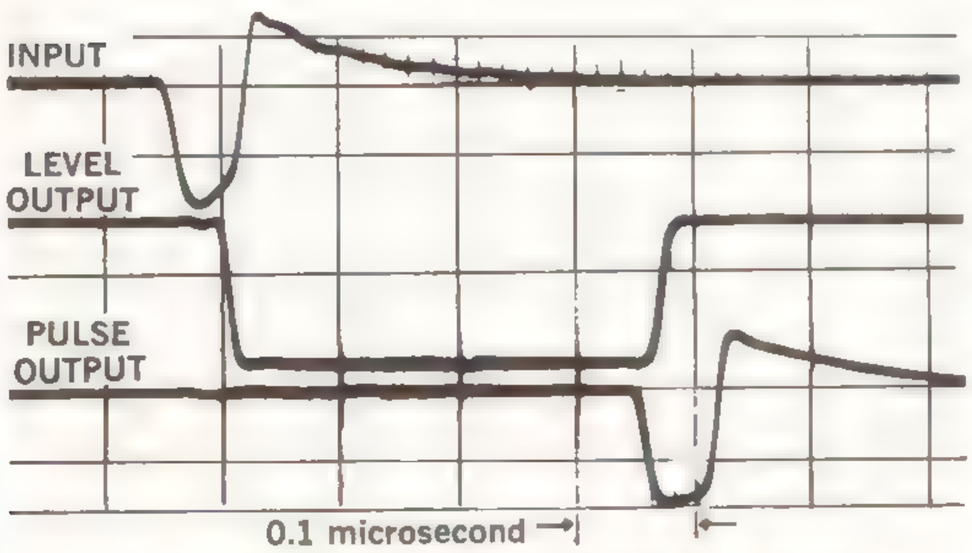


Figure 1 — INPUT AND OUTPUT VS TIME

The delay interval is determined primarily by the capacitor connection (3 capacitors are available). An internal 15,500 ohm potentiometer provides for the fine adjustment. The capacitor 1 will permit adjustment from approximately 0.25 microsecond to 2.5 microseconds; 2, from approximately 2.5 microseconds to 35 microseconds; and 3, from approximately 35 microseconds to 500 microseconds. A longer delay may be accomplished by installing an additional capacitor between the external capacitor terminals. Terminals U and T must be jumpered to use the internal potentiometer for fine control. Circuit recovery time is equal to 20% of the maximum delay available on that particular circuit's capacitor connection.

A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.3%.

INPUT: The input to the delay is a DEC Standard 70 nanosecond Negative Pulse on the base of a pulse gate, such as the one included in the delay module. The base of the built-in pulse gate represents 1 unit of Pulse Load. If more logical inputs are desired, they can be provided by connecting pulse gate collectors to the collector of the built-in pulse gate. Mixing of

several pulses can also be accomplished by using half of a DEC Diode Type 1110 with DEC Standard 70 nanosecond Negative Pulses applied to the diodes and the collector tied to the collector of the built-in pulse gate.

OUTPUT: Level — When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval. This level is capable of simultaneously driving: (a) 8 units of Base Load if speed is important, otherwise 12 bases; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. Pulse — At the end of the delay interval, a DEC Standard 70 nanosecond Pulse occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/80 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0 ma.

TYPICAL APPLICATIONS

WAVE FORM GENERATOR

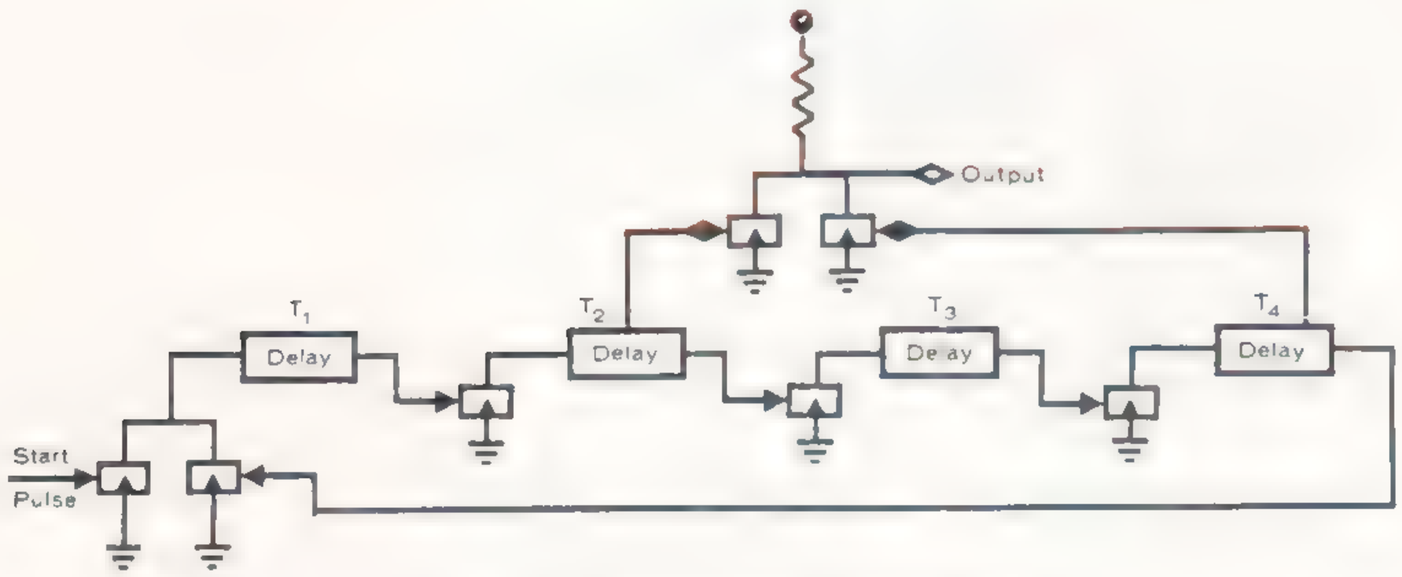


Figure 2 — WAVE FORM GENERATOR

Delay units are particularly useful in generating signals of arbitrary width. The network of delays in Figure 2 will produce the wave form in Figure 3.

The 1st and 3rd delays, not being connected to the output inverters, will produce no signal during their delay period. The 2nd and 4th, however, will produce a ground output for the duration of their respective delays. The wave form is periodic, since the pulse output from T_4 goes back to T_1. Due to delay recovery time, more than one delay unit is necessary to recycle the pulse.

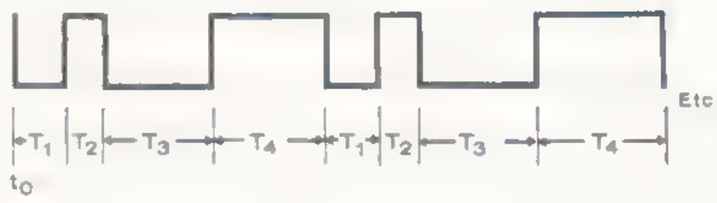


Figure 3 — OUTPUT WAVE FORM

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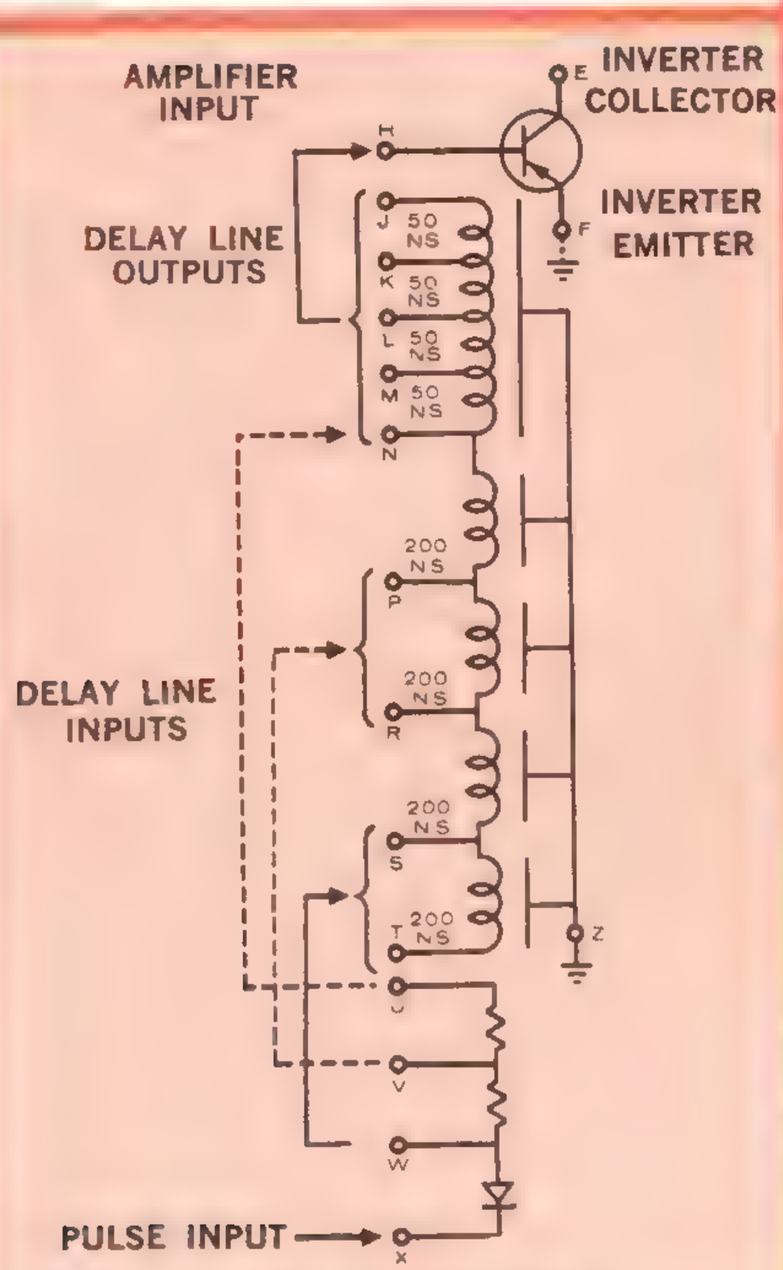
1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1310-1311
DELAY LINE



1310 DELAY LINE

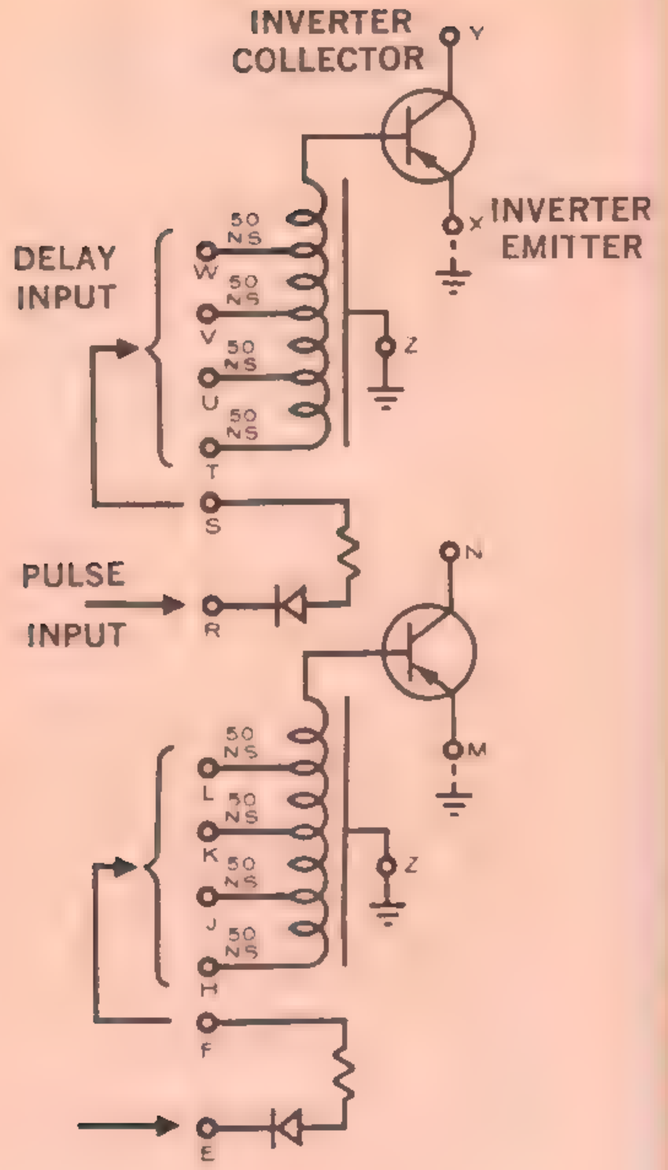
Delays in steps of 50 nanoseconds are produced on the Types 1310 and 1311. The maximum delay for the Type 1310 is 1 microsecond. The Type 1311 contains two delay lines with a maximum of 200 nanoseconds delay for each line. A transistor amplifier is built into the Type 1310 package, and its input, not being a standard inverter, must be driven by the delay line. The 20 nanosecond delay of the inverter must be added to the total delay time.

The delay output of each of the two delay lines contained in the Type 1311 is connected to a transistor inverter whose emitter and collector terminals are available for logical gating. The 20 nanosecond delay through the inverter must be added to the delay of the line; therefore, the available delay increments are 70, 120, 170, and 220 nanoseconds. Controls: The input pulse to the Type 1310 is connected to pin X, and the input of the delay line (pins N through T) is connected to one of the pins U, V, or W. The output of the delay line (pins J through N) is connected to the base of the output inverter, pin H. The input to the Type 1311 is applied at pin R (or E) and the desired delay is obtained by connecting S (or F) to one of the delay line taps.

INPUT: The input should be a DEC Standard 70 nanosecond Negative Pulse or its equivalent. The Type 1310 represents 5 units of Pulse Load; and the Type 1311, 3 units of Pulse Load.

OUTPUT: The emitter of the output inverter must be grounded; the transistor's collector should be connected to the input of a DEC Pulse Amplifier Type 1607 or other unit being pulsed. However, if additional logic gating is required, it may be done with up to three transistor inverters placed in series between the collector and the pulse amplifier.

POWER: Type 1310: −15 volts/0 ma; +10 volts (A)/2.1 ma; +10 volts (B)/0 ma. Type 1311: −15 volts/0 ma; +10 volts (A)/1.0 ma; +10 volts (B)/1.0 ma.



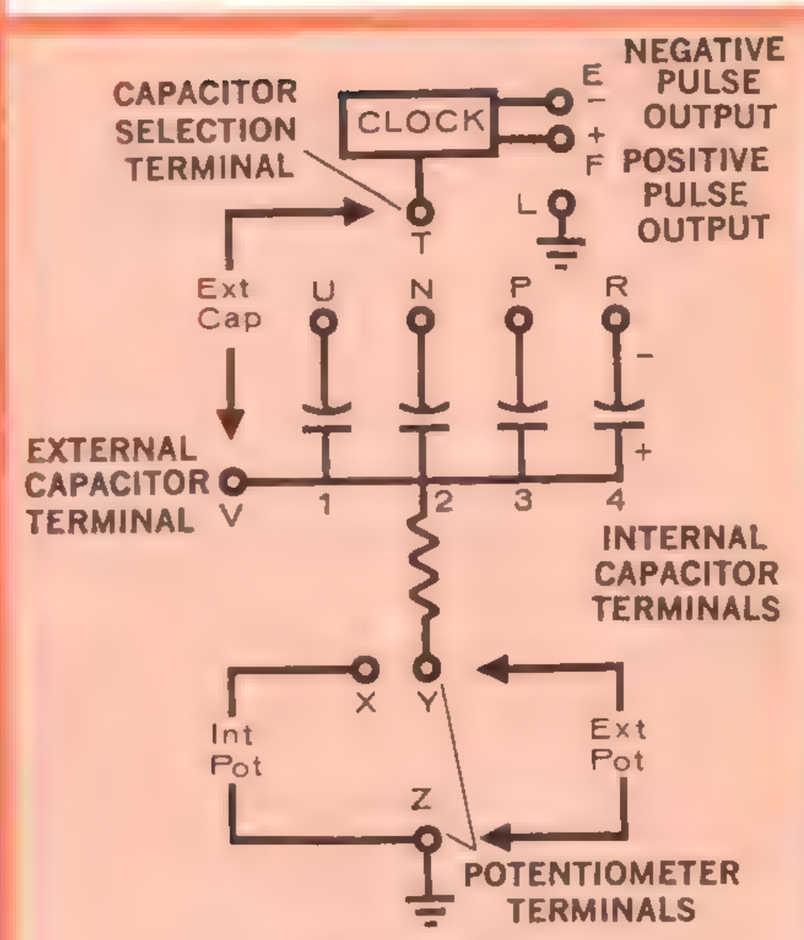
1311 DELAY LINE

INVERTER
EMITTER

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1404 -1406
CLOCKS



1404 VARIABLE CLOCK

1406 CRYSTAL CLOCK

The DEC Variable Clock Type 1404 produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies available. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the Type 1406 Crystal Clock, which contains a single-frequency crystal oscillator, may be used.

The Type 1404 variable frequency oscillator is variable from 500 cycles/second to 5 megacycles/second. Four scales provide magnitude control, and a built-in 20,000-ohm potentiometer permits fine adjustment. Terminals for an external potentiometer are available. Lower frequencies may be obtained by adding an external capacitor between pins V and T.

The Type 1406 employs a series resonant crystal oscillator circuit and pulse shaping buffer amplifiers to provide very precise timing. The amplifiers produce DEC Standard 70 nanosecond Pulses in the 500 kilocycle to 5 megacycle range. The clock frequency, specified by the customer, is stamped on the crystal. The 1404 and 1406 have the same output connection.

OUTPUT: The output is a DEC Standard 70 nanosecond Pulse which occurs at the preselected frequency. The pulse may be made either positive or negative by grounding the appropriate output terminal. The signal can drive 8 units of Pulse Load. **Crystal Clock:** The stability of the crystal clock's output frequency is 0.01% over a temperature range of −20 to +55°C. **Variable Clock:** A 20% change in the power supply voltage on the Type 1404 Clock will change the prf less than 1% and its pulse-to-pulse jitter is less than 0.2%.

POWER: Type 1404: −15 volts/66 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. **Type 1406:** −15 volts/171 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

SYNCHRONIZATION

It is possible to synchronize the output of Type 1404 Variable Clock to the outputs of other clocks, generators or external signals. The frequency of the synchronizing signal may be the same, a harmonic or a subharmonic. (Synchronization to a subharmonic results in an average period standardization only. The time from one pulse to the next may vary since only one clock pulse in several is actually triggered by the incoming signals.) The phase drift of clocks operating on the same frequency is eliminated by synchronizing the clocks.

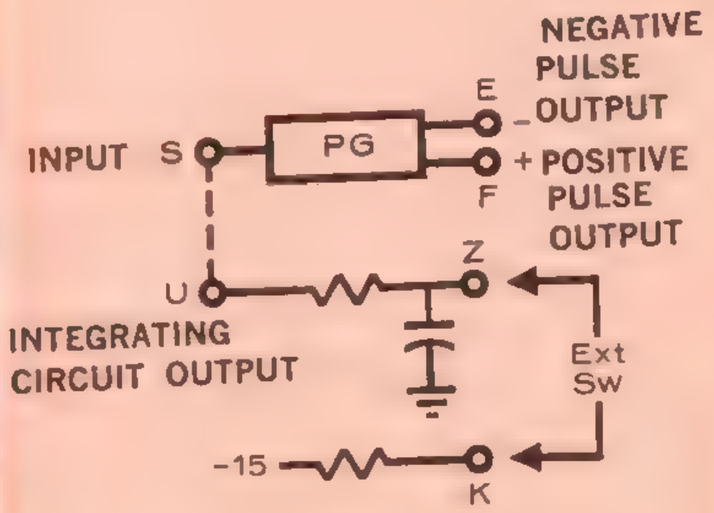
A typical application is the synchronization of DEC Variable Clocks to a DEC Crystal Clock to obtain the desirable features of both the crystal and variable clocks. Provide the DEC Crystal Clock Type 1406 with a simple resistive attenuator whose output (capacity coupled) can be used as the standardization signal for the variable clocks used in the system. Synchronization signal amplitudes of from one-tenth to several tenths of a volt peak to peak are most satisfactory. The signal of the crystal clock is applied to the capacitor of the variable clock at pin V. (This signal must be applied through a blocking capacitor with an impedance on the order of 1000 ohms at the operating frequency.)

As in all synchronizing schemes, the smaller the synchronization signal, the less reliable is the lock and the more tendency there is over a long period of time for small variations in the natural free running frequency of the multivibrator to cause the locking action to become intermittent or fail. There may be cases, however, in which it is desirable to be able to synchronize the variable clock in a special ratio to the synchronizing frequency for a short period of time (e.g. 2/3, 4/3, 5/7) to perform a single experiment, and in these cases the locking reliability for the weak inputs required will be found to be satisfactory.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1410
PULSE GENERATOR



The Type 1410 converts external signals to DEC Standard Pulses. A Schmitt circuit produces a DEC Standard 70 nanosecond Pulse at the output every time the input voltage goes more negative than −2.5 volts after having been more positive than −1.0 volts. This unit also contains an integrating circuit to filter contact bounce when a switch or relay is used to generate the pulse.

INPUT: Pulse Generator — The input is a DC connection, thereby eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. The input signal should stay between +10 volts and −10 volts. The input can come from an external source or from the output of the integrating circuit. Integrating Circuit — The two inputs to this circuit come from switch or relay outputs.

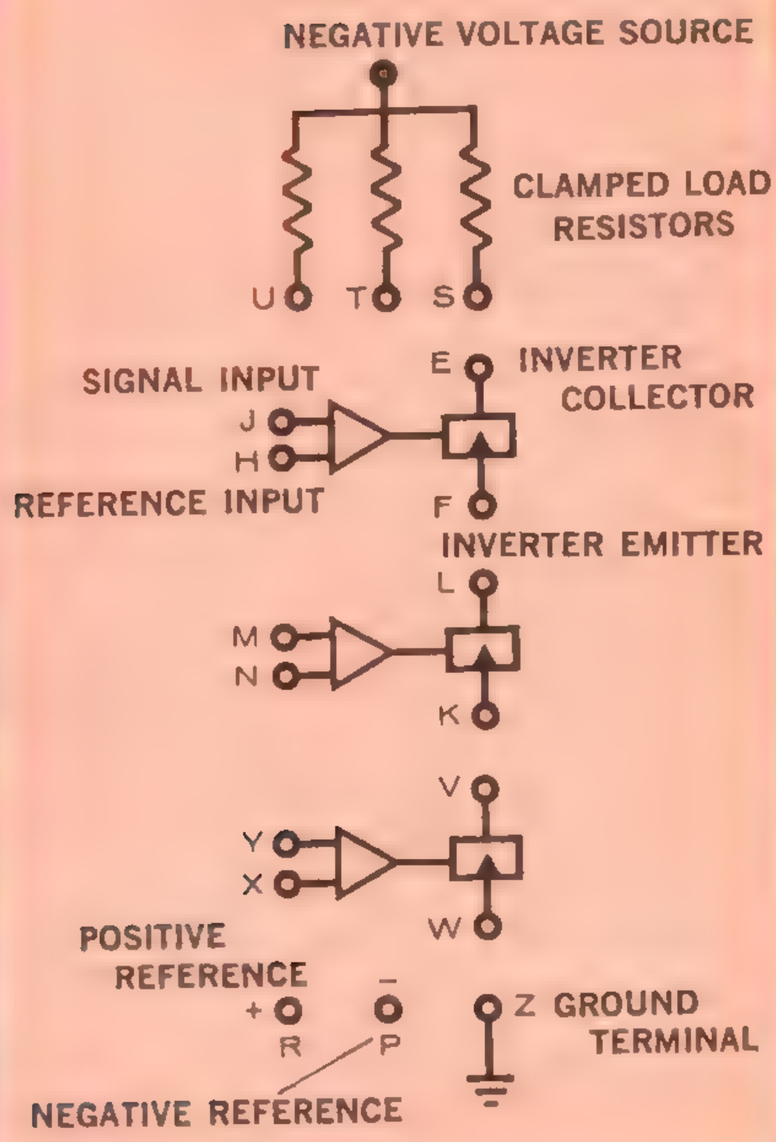
OUTPUT: Pulse Generator — The output is a DEC Standard 70 nanosecond Pulse. The pulse will be negative if the positive terminal is grounded; it will be positive, if the negative terminal is grounded. The maximum prf is 2 megacycles. This signal can drive 8 units of Pulse Load. Integrating Circuit: The time constant of the integrating circuit is 12 milliseconds.

POWER: −15 volts/34 ma; −3 volts/0 ma; +10 volts (A)/5 ma; +10 volts (B)/5 ma.

d g t l

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1501
LEVEL STANDARDIZER



Three difference amplifiers convert signals in the range of ±10 volts to DEC Standard Levels. Reference levels may be between +10 and −1.5 volts. The maximum ZERO offset is 0.1 volt and the minimum dynamic range is 0.1 volt. Three reference voltages are provided in the package. These are: + 1.2 ±0.1 volts, −1.5 ±0.1 volts, and ground. The output is from a transistor inverter similar to the DEC Inverter Type 1105. If the transistor collector is connected to the load resistor (available in the package) and its emitter is grounded, the output will be at −3 volts when the input is positive with respect to the reference voltage and at ground when the input is negative with respect to its reference.

INPUT: Reference — An external reference voltage in the range of +10 to −1.5 volts may be used. The current required is +0.1 ma if the reference is more positive than the input, and −0.2 ma if the reference is more negative than the input. When the reference is more negative than +3.0 volts and also more negative than the input, the load is 1800 ohms to +3.3 volts. Signal Input — Voltages may be in the range of ±10 volts. If the input is more positive than the reference, the load is +0.1 ma. If the input is more negative than the reference, the load is −0.2 ma. If the input is more negative than −2.7 volts, the load is 800 ohms to −2.5 volts.

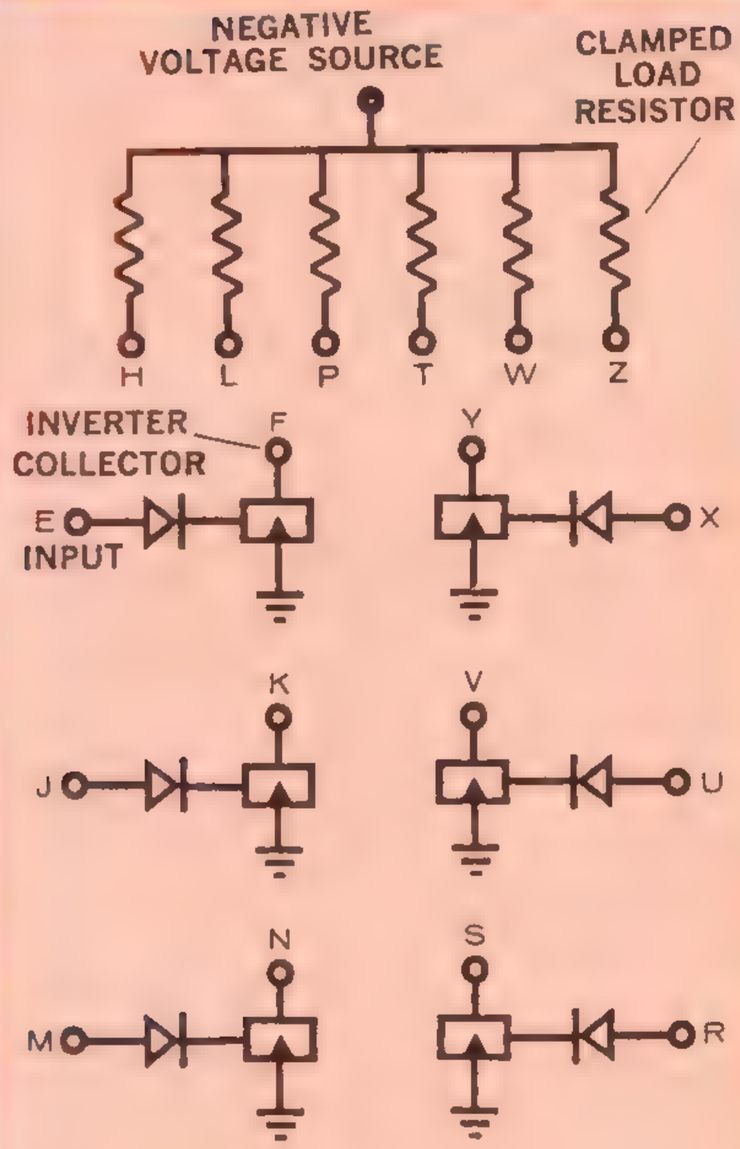
OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of a flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 4 units of Base Load at 5 megacycles (7 where speed is not a problem); and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters, provided there is not more than one simultaneous emitter-collector path to a DC Emitter Load. No more than 3 level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, 4 gates may be connected in series.

POWER: −15 volts/72 ma; +10 volts (A)/0.5 ma; +10 volts (B)/18 ma;

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1502
LEVEL STANDARDIZER



Six circuits convert levels in the range of −50 volts to +10 volts into DEC Standard Levels. The upper input level must be more positive than ground and the lower level more negative than −2.5 volts. The total transition time for the Type 1502 is 0.6 microsecond or less. A typical application of the Type 1502 is for conversion of Univac 1102 levels into DEC Standard Levels.

INPUT: Voltage levels must be within the range of −50 volts to +10 volts. Maximum input current is 2.5 ma at +10 volts. Less than 0.15 ma is required when the input is more negative than −2.5 volts. When the input is more negative than −2.5 volts, the output will be at ground. When the input is more positive than ground, the output will be at −3 volts.

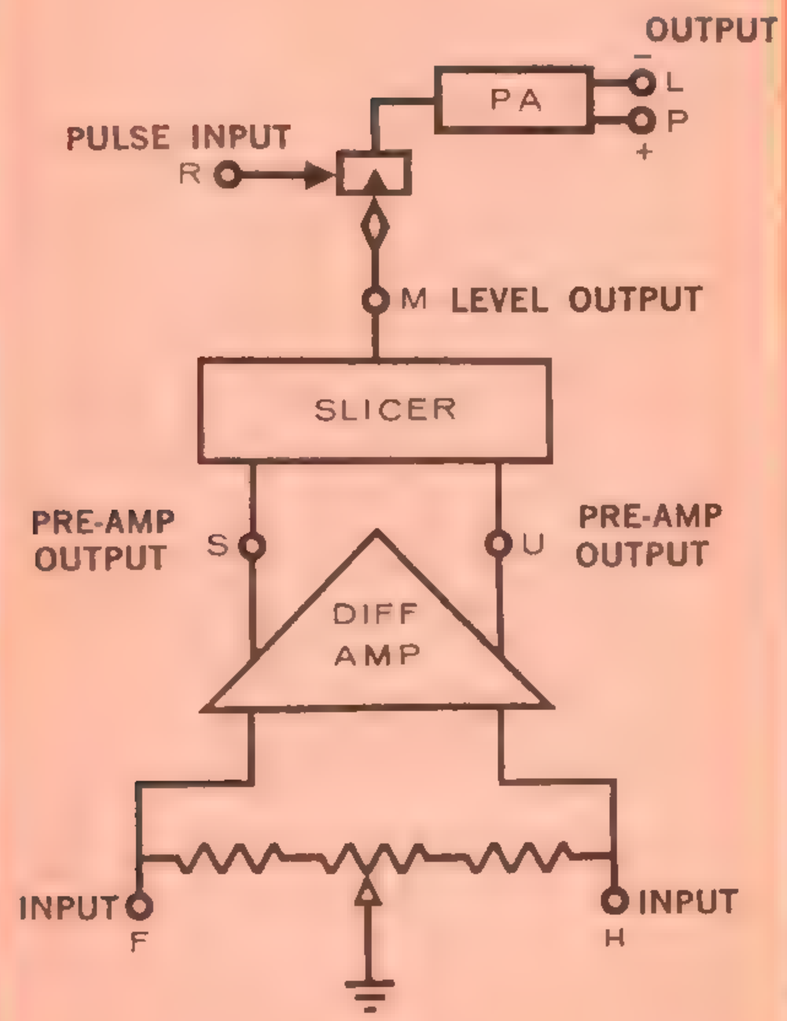
OUTPUT: When connected to a clamped load resistor, each output can simultaneously drive 7 units of Base Load and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor may be connected to several emitters providing there is not more than one simultaneous emitter-collector path to a DC Emitter Load or to the pulse input of a flip-flop or other unit being pulsed. No more than two level gates and one pulse gate may be connected in series with a level standardizer.

POWER: −15 volts/94 ma; +10 volts (A)/9 ma; +10 volts (B)/0 ma.

d g t l

1000 SERIES
SYSTEM MODULES

1540
SENSE AMPLIFIER FOR CORE MEMORIES



The Type 1540 detects ONE and ZERO outputs from coincident-current core memories. An AC coupled differential preamplifier with a difference gain of approximately 20 and a common mode gain of one-half precedes a rectifying slicer with a variable slicing voltage. The output of the slicer is amplified and used as an enabling level for the pulse amplifier contained in the package. When the core signal is of sufficient amplitude to produce a ONE output from the slicer, a pulse at the input of the pulse amplifier produces a pulse at the output.

Varying the +10A voltage varies the slice level which permits memory marginal checking. The low frequency response of the preamplifier is such that the output returns to ground 0.5 milliseconds after a 50 mv step is applied to the input. There is an 80 nanosecond maximum delay from the input to pin M.

Two potentiometers are provided. The upper potentiometer controls the balance of the input. The lower controls the slice level, which may be from 0 to 50 mv referred to the input of the preamplifier.

Three terminals are provided to monitor the operation of the circuit. Two are connected to the junction of the preamplifier and the slicer; the third monitors the enabling level to the pulse amplifier. No permanent connection should be made to these terminals, especially to the preamplifier outputs; the preamplifier has sufficient gain and band pass to oscillate, if enough capacitive coupling is present between these terminals and the input. If the input signal is relatively negative at pin F, the preamplifier output is relatively negative at pin S.

— the load presented to a difference signal is the 500-ohm balance potentiometer, the center tap of which is grounded. — a DEC Standard 70 nanosecond Negative Pulse (1 unit of Base Load) drives the pulse amplifier.

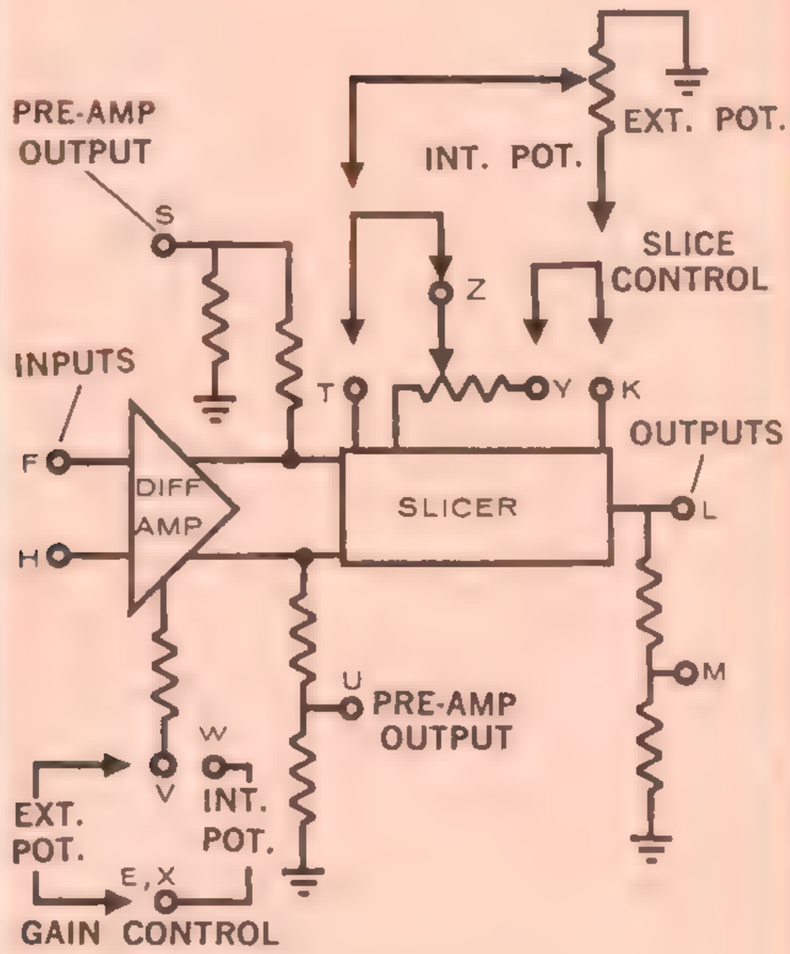
Each time the input conditions are met, a DEC Standard 70 nanosecond Pulse of either polarity, capable of driving 16 units of Pulse Load, is produced at the output.

−15 volts/75 ma; +10 volts (A)/0.2 ma; +10 volts (B)/13 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1546
SENSE AMPLIFIER



The Type 1546, like the Type 1540, detects ONE and ZERO outputs from coincident-current core memories; however, several more test points are brought out, and the gain of the preamplifier may be varied from 5 to 65. The preamplifier is an AC-coupled difference amplifier. It is followed by a rectifying slicer and inverter output.

The low frequency response of the preamplifier is such that the output of the preamplifier returns to the DC operating point in 120 to 500 microseconds, depending on gain control setting. The unit delay is 25 nanoseconds. Controls: Internal connections are provided to determine the gain of the preamplifier and the DC comparison level that is applied to the slicer; however, terminals are brought out so that the internal connections may be replaced by external controls. Internal gain control occurs if pin W is tied to pin V. External control may be accomplished by connecting a 1000-ohm potentiometer between X and V. The slicing level will be controlled internally by connecting pin Y to pin K and pin Z to pin T. External control is provided by connecting T to the arm of a 1000-ohm potentiometer that is installed between pin K and ground.

Two attenuated signals are brought out to permit monitoring of the preamplifier output and the slicer output without seriously loading the circuit. The outputs of the preamplifier, attenuated 10:1, are brought to pins S and U; that of the slicer, attenuated 11:1, is brought to pin M.

INPUTS: About 300 ohms should be tied from each input to ground since no DC load is provided at the input. Common-mode input impedance is near 50,000 ohms. Differential input impedance, dependent upon gain control setting, may be as low as 500 ohms. Preamplifier common-mode gain is one-half.

OUTPUTS: The unit is capable of driving one DC Emitter Load or several Pulsed Emitter Loads, providing not more than one is pulsed at a time. Output is ground when the slice control voltage is maximum; it is −4.5 to −5.5 volts when the slice control voltage is ground. Slice control has a sufficient range to slice through ZERO input.

POWER: −15 volts/48 ma; +10 volts (A)/0.2 ma; +10 volts (B)/15 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1547
DIFFERENCE AMPLIFIER

The Type 1547 is a high gain difference amplifier, the outputs of which are logic levels of 0 and −3 volts. Although it is a linear amplifier for relatively small input voltages (less than 10 millivolts), its high gain and good common mode rejection make it especially useful for detecting the sign of the voltage difference applied to its input.

This unit is particularly useful in analog-to-digital conversion. It may also be used for converting small signals into DEC Standard Levels. The circuit contains two stages of difference amplifiers coupled to output amplifiers. Two potentiometers are included for adjustment of ZERO SET and COMMON LEVEL.

INPUT: The input voltage range is from 0 to −10 volts. The more positive of the pair of inputs draws approximately 1 microampere. The more negative input draws approximately −0.1 microampere.

OUTPUT: The difference amplifier outputs are logic levels that will be between ground and −3 volts. When the input voltage difference is less than approximately 10 millivolts, the output will be a function of the input. When the input voltage difference exceeds 10 millivolts, one output will be at −3 volts and the other will be at ground. Each output is capable of driving 7 units Base Load, if speed is no problem. For maximum speed, it is recommended that the output loading be limited to 1 unit Base Load.

POWER: −15 volts/55 ma; +10 volts (A)/0 +10 volts (B)/21 ma.

TYPICAL APPLICATIONS

ZERO SET AND COMMON BALANCE: Figure 1a shows the output voltage at each terminal as a function of the difference between the input voltage signals when the amplifier is balanced. Figures 1b and 1c show examples of an unbalanced amplifier. If the intersection of the curves is shifted to the left or to the right, the resulting error is zero offset and may be corrected by the ZERO SET control. The intersection of the curves may be shifted up or down from the nominal —1.5 volt point by the COMMON LEVEL adjustment.

The adjustment of the difference amplifier may be changed to suit the application. Generally, adjustment is made by measuring the voltage at the two output terminals when the inputs are tied together at the center of the input voltage range. The upper potentiometer is used to bring the output signals to the same voltage (ZERO SET) while the lower one adjusts the output level of both terminals simultaneously (COMMON LEVEL). The adjustment is correct when both terminals are —1.5 volts.

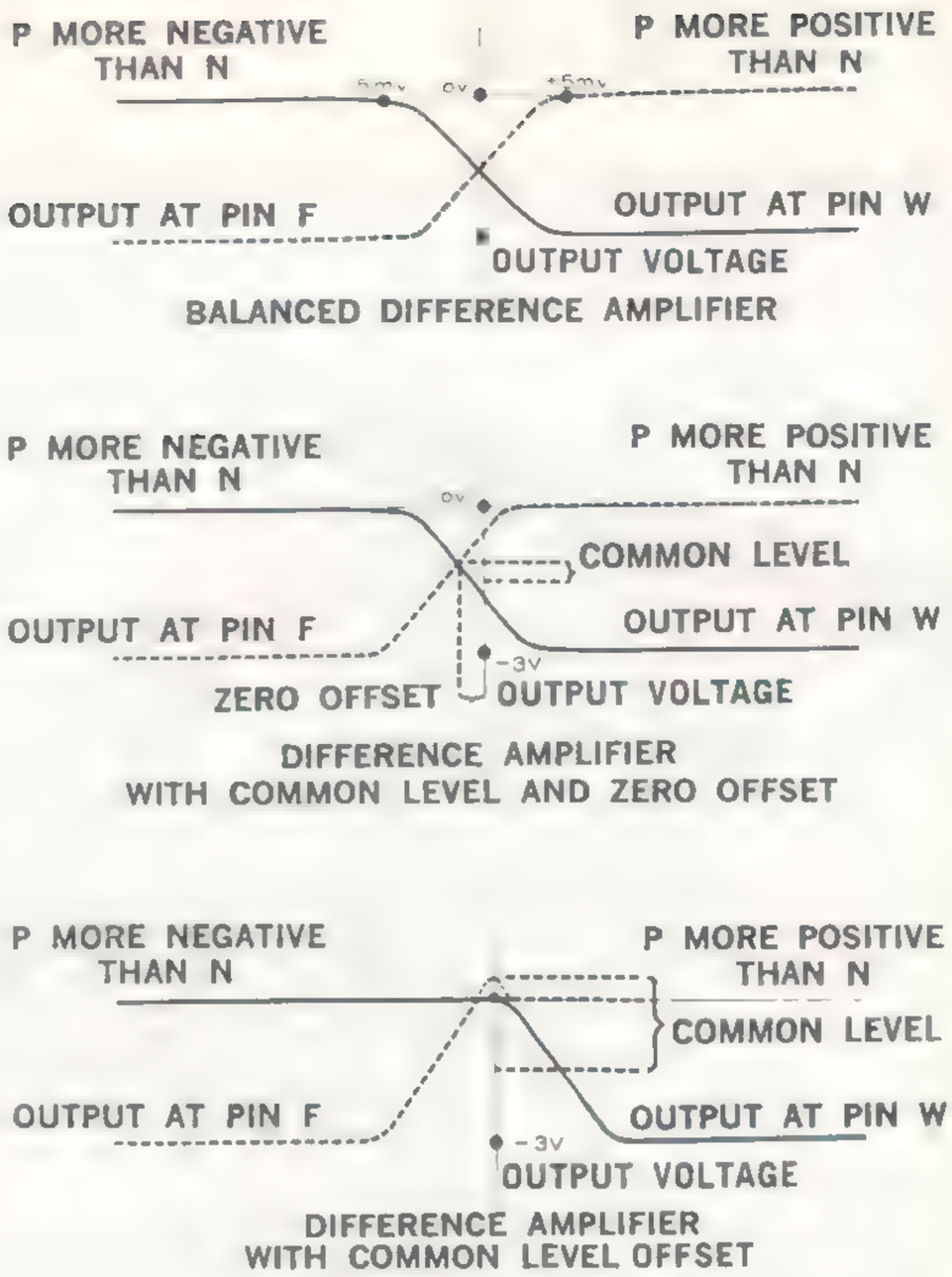


Figure 1 — DIFFERENCE AMPLIFIER OUTPUTS

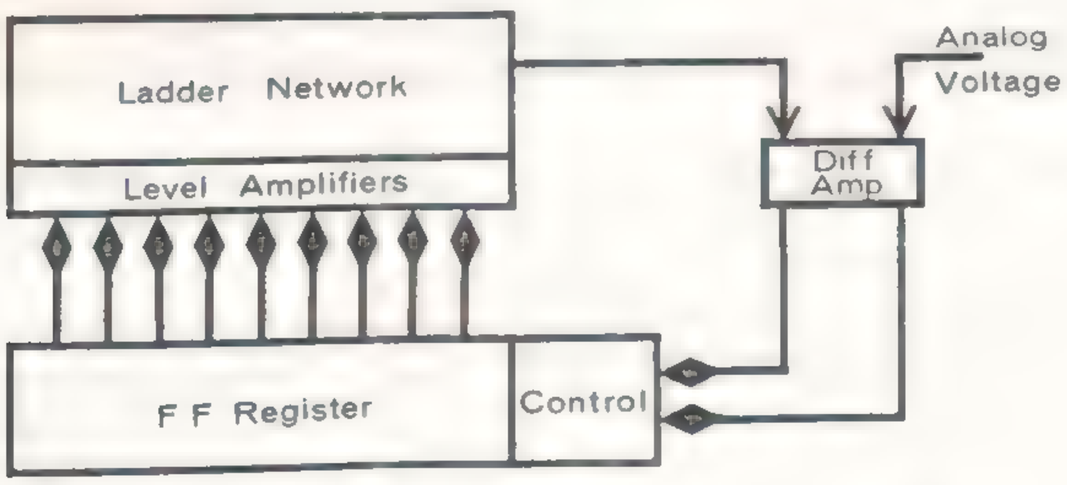


Figure 2 — ANALOG TO DIGITAL CONVERTER

FACTORS AFFECTING ACCURACY: Typical common mode rejection ratio is 3 millivolts equivalent input offset for 10V common voltage change at the input. Typical temperature coefficient is 1 millivolt equivalent input offset per degree centigrade. When a DEC Power Supply Type 728 or 722 is used, a change of line voltage of from 105 to 125 volts at the power supply input will cause less than 0.6 millivolts equivalent input offset in the 1547 difference amplifier.

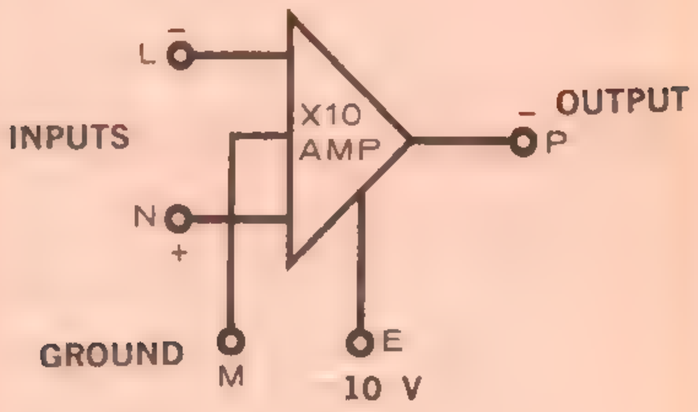
Figure 2 shows a general block diagram of an analog-to-digital converter. Conversion is implemented by assuming a digital value, converting this value to an analog signal, comparing the analog equivalent of the assumed value with the actual analog input, and using the results of the comparison to adjust the assumed value. The comparison device used is the Type 1547 difference amplifier.

Detailed bulletins are available on the adjustment of the Type 1547 and on the use of the 1547 in analog-to-digital conversion devices. These may be obtained from your nearest Digital sales office or representative.

d g t a l

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1550
X10 AMPLIFIER



This wide-band AC difference amplifier is used in core and memory testers to amplify core output prior to slicing. The gain is 10:1 for difference signals and varies slightly with the −10 supply voltage; therefore, the −10 volt supply must be stable and well regulated. The attenuation is 10:1 for common mode signals. The band pass is flat from 10 kilocycles to 10 megacycles and is down 3 decibels at 20 megacycles. The maximum output noise is 2 mv when 300-ohm resistors are attached to ground from each input. Non-linearity is less than 1%.

Controls: There is a potentiometer available through the module handle that varies the gain from 4 to 12 if there is no load at the output. Power: Pin E is used for bringing −10 volt power into the module. Since the gain of the amplifier is dependent on the stability of this voltage, the Type 1562 is recommended as the source of power.

INPUT: The maximum input is 100 mv when the gain is set at 10. The input impedance is approximately 5000 ohms. If the input at pin L is negative relative to that at pin N, the output is negative.

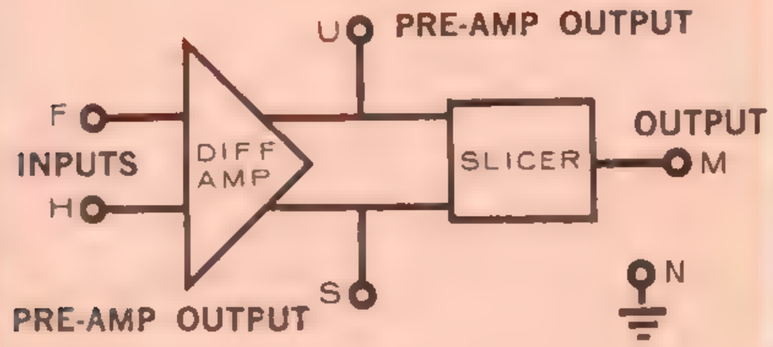
OUTPUT: The output circuit is an emitter-follower, AC coupled to an inductor insuring that the DC output level remains ground. The maximum output voltage is 1 volt. The output impedance is approximately 35 ohms. Each output can drive three slicer inputs (DEC Types 1556 or 1570).

POWER: −15 volts/45 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma; −10 volts (E)/±5 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1552
SENSE AMPLIFIER FOR CORE MEMORIES



The Type 1552 is an economical circuit for detecting ONE and ZERO outputs from coincident-current core memories. It is suitable for use in small, relatively slow memories where some of the features of the Type 1540, particularly the pulse amplifier, are not necessary. A high gain, AC coupled differential amplifier and a rectifying slicer make up this unit. Marginal check on memory may be made by varying the +10(A) voltage which varies the slice level. The +10 volt(B) terminal should not be varied significantly.

Maximum delay time for the sense amplifier is 45 nanoseconds. Low frequency response is such that the output of the preamplifier returns to ground approximately 500 microseconds after a 50 mv step is applied to the input. Control: A slice control varies the slicing point from 5 to 20 mv referred to the input of the preamplifier. Two terminals are brought out to permit monitoring of the preamplifier. No permanent connections should be made to these points, since the preamplifier may oscillate if sufficient capacitive coupling is present between input and output. If the negative side of the input is at pin F, the negative side of the preamplifier output is at pin S.

INPUT: The operating range is 0 to 50 mv. A load of about 300 ohms to ground is suggested for each input terminal, since no input termination is provided. Preamplifier common-mode input impedance is 50,000 ohms, and differential signals less than 50 mv have an input impedance of about 3,000 ohms.

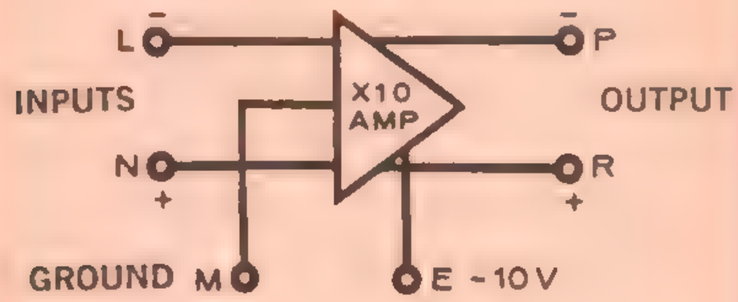
OUTPUTS: The output is through an unclamped inverter. The output is −3 volts except when a differential signal is applied at the input; then the output level becomes ground. The output is capable of driving one DC Emitter Load or any number of Pulsed Emitter Loads, provided only one is pulsed at a time. The output impedance is 1500 ohms when the output transistor is off. When the unit is driving a capacitor-diode gate input, the normal time required to inhibit the gate is doubled.

POWER: −15 volts/35 ma; +10 volts (A)/0.4 ma; +10 volts (B)/14 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1554
X10 AMPLIFIER



The Type 1554, like the Type 1550, is used to amplify core outputs prior to slicing; however, outputs are provided for both core output polarities. The gain is 10:1 from a difference input signal to each single-ended output and is stable if the −10 volt supply is well regulated. Common-mode gain is 1/10. The band pass is flat (±1 decibel) from 10 kilocycles to 10 megacycles and is down 3 decibels at 20 megacycles. Two mv is the maximum output noise introduced by the amplifier with 300-ohm resistors attached to the input terminals. Non-linearity is less than 1%. Controls: The gain can be varied from 4 to 12, provided the output is not loaded. A balance control adjusts the gain at pin R to be equal to that at pin P. The range is about 6%.

INPUTS: 100 mv is the maximum input for a gain of 10. The input impedance is approximately 5000 ohms. If the input is relatively negative at pin L, the output at P is relatively negative.

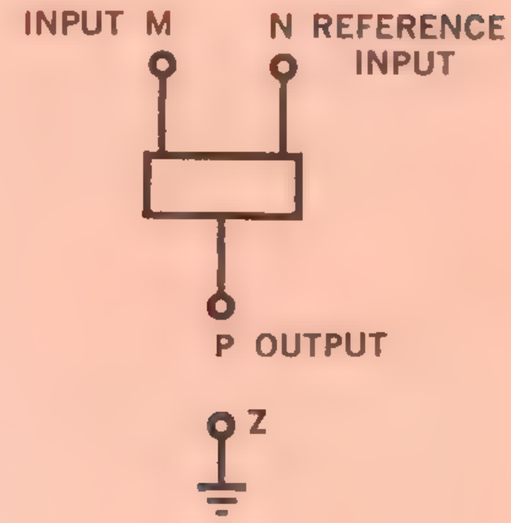
OUTPUTS: The output circuits are emitter followers, AC coupled to inductors to insure that the DC output voltage is zero during standby. The output impedance is 35 ohms. The unit normally drives three slicer inputs (DEC Types 1556 or 1570).

POWER: −15 volts/70 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma; ±10 volts/−10 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1556
SLICE AMPLIFIER



The Type 1556 Slice Amplifier is a high speed detector of the relative polarity of two input signals. It contains one slicing circuit — essentially a difference amplifier — whose output saturates at 0 and −3 volts. The typical delay for output rise is 40 nanoseconds and the total transition time is 62 nanoseconds. The typical delay for output fall is 24 nanoseconds, and the total transition time is 38 nanoseconds.

Stability is ±1 mv at constant temperature, and its accuracy is ±5 mv from −20°C to +55°C. Control: An internal potentiometer controls the slicing point. It is generally set so that the output is either oscillating or at −1.5 volts when the two input voltages are equal. The potentiometer could be set so that the output oscillates when the difference is up to 30 mv.

INPUT: The input magnitude should be less than 1 volt. A DC reference level in the range of 0 to −1 volt should be applied to pin N. If two AC signals are to be compared, the capacitor attached to pin N is to be removed. When pin M is more negative than pin N, the input current is 0.4 ma, otherwise no current is required. The circuit should be driven by an impedance of 100 ohms or less.

OUTPUT: The output is an inverter with a 680-ohm clamped load. For maximum speed, the load should be limited to one unit Base Load. Up to 10 units Base Load can be driven at 5 megacycles. The output is negative when pin M is more negative than N; otherwise it is ground.

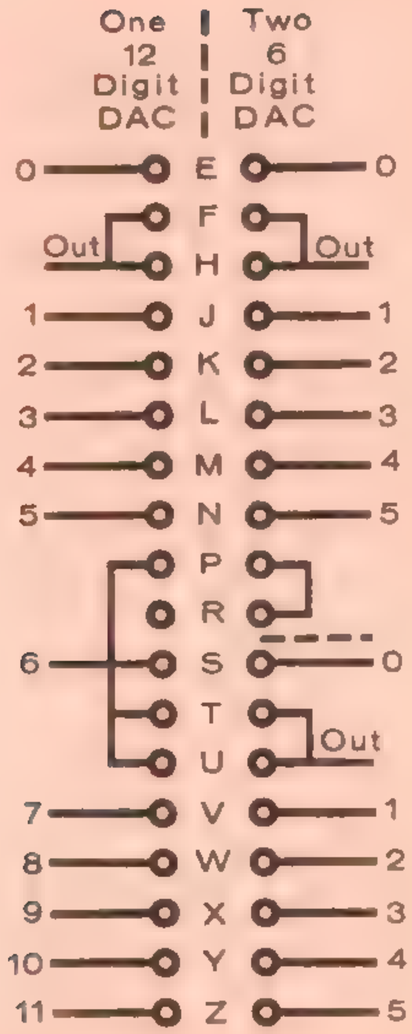
POWER: −15 volts/45 ma; +10 volts (A)/0 ma; +10 volts (B)/9.5 ma.

FEATURE: The short delay and the total transition time of the 1556 make it especially suitable for testing core memory outputs. (The 1550 Amplifier is used to amplify the core output by a factor of 10, before it is fed into pin M of the 1556.) During the time the maximum magnitude of the core signal equals or exceeds that of the DC reference level, the slicer output responds; otherwise no change occurs. The 1550 Amplifier is used to increase the core signal by a factor of 10. For example: when negative core signals ≥ -1 volt go into pin M with N set at −1 volt, the output will switch from ground to −3 volts. When the core pulse decays, the output switches back to 0 volts.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1561
DIGITAL-TO-ANALOG CONVERTER



The Type 1561 is a digital-to-analog converter employing a binary weighted resistor ladder network. This module can serve as the single converter for up to twelve binary bits or it may be used as two converters with up to six bits each. In addition, the most significant bit may be removed, thus effectively providing a one bit shift. This is useful when the ladder (or ladders) is driving a high impedance circuit. The settling time of the Type 1561 is 0.1 to 0.15 microsecond.

The Type 1561 uses 1% deposited carbon resistors with a temperature coefficient of ±250 ppm/°C. Potentiometers (of 500 ohms each) are available for adusting the eleven most significant bits. (When a circuit is used to make two converters, one of the converters has six adjustable bits, while the other converter has only the five most significant bits adjustable.) The Type 1554 Module Extender should be used to permit potentiometer adjustment.

Of the five converter networks manufactured by Digital Equipment Corporation, the Type 1561 is the fastest but has the least accuracy and the highest temperature variation. A summary table of the characteristics of the five networks is shown on the reverse side of this page.

INPUT: The input impedance is 3000 ohms. The inputs are normally driven from DEC Single-Ended Bridges with 0 and −10 volt levels. When accuracy requirements permit, level amplifiers such as the Types 4667 or 1667 may be used, with the more negative voltage level in the range of −3 to −10 volts. When an accuracy of three bits or less is required, the input may be driven by DEC Standard Levels of 0 and −3 volts. The input current will vary from 0 to ±1ma (±1 unit Base Load) depending on the state of the ladder. Inputs not in use should be grounded.

OUTPUT: The output impedance is 1000 ohms. When the shift feature is used, the output impedance will be 2000 ohms. The maximum open circuit output voltage will be equal to the more negative input voltage level less the value of the least significant bit.

POWER: −15 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

DIGITAL-ANALOG CONVERSION

DIGITAL-TO-ANALOG

To convert from a digital number to an analog voltage, a resistive ladder network is connected to the flip-flop register which holds the digital number. The ladder network is weighted so that each digit of the register will contribute to the output voltage in proportion to its value.

The digital input signal determines the analog output voltage, since the resistive ladder network is a passive component. Since digital voltage levels are not as precise as is usually required in an analog system, level amplifiers are often placed between the flip-flops and the ladder network. These may be the single-ended bridges Types 1677, 4677 or 4677A. Where less accuracy is required, the Types 1667 or 4667 may be used. A reference voltage is supplied to the level amplifiers from a precision reference power supply such as Type 1562.

ANALOG-TO-DIGITAL

Analog-to-digital conversion is implemented by assuming a digital number, converting this number to an analog signal with a D to A converter, comparing this voltage with the analog input and using the results of this comparison to adjust the assumed number. The comparison device used is the Type 1547 Difference Amplifier.

The speed of an analog-to-digital conversion system depends on the method chosen for adjusting the assumed number and on the accuracy required. (The accuracy has a two-fold effect, since it determines the number of steps in the adjustment process and also since the more accurate components, ladders, level amplifiers, and the difference amplifier operate more slowly.)

Ladder Network Table

Type No.	No. of Ladders	No. of Bits	Settling Time (in μsec)	Input Impedance (in ohms)	Output Impedance (in ohms)	Remarks
1561	1 or 2	Up to 12; or 2 converters of 6 bits each (11 bits adjustable)	0.15	3000	1000*	Deposited carbon resistors and carbon composition potentiometers for trimming. Of the five models, the 1561 has the smallest setting time but has the greatest temperature variation.
1563	2	Up to 8 for each ladder; (potentiometers on the 4 most significant bits of each ladder)	1.0	3000	1000	Wire wound resistors and potentiometers. (Wire wound resistors provide maximum accuracy but have the longest setting time.)
1564	1	Up to 14; (potentiometers on the 8 most significant bits)	1.0	3000	1000	Wire wound resistors and potentiometers. Identical to Model 1563 except for number of bits.
1566	1	Up to 3 decimal digits plus one optional bit: that is, 0 to 999 or 0 to 1999. (potentiometers on 8 most significant bits, including optional bit)	2.5	3000	900	For BCD (8421 code) conversion. Wire wound resistors and potentiometers similar to Model 1563.
1568	1	Up to 12; (8 bits adustable)	0.3	3000	1000	Metal film resistors and potentiometers.

*May be 2000 ohms for single 11 bit converter of two 5 bit converters.

ADDITIONAL INFORMATION

Detailed bulletins are available on Digital-to-Analog and Analog-to-Digital Conversion processes (speeds and accuracies). These may be obtained from any Digital sales office or representative.

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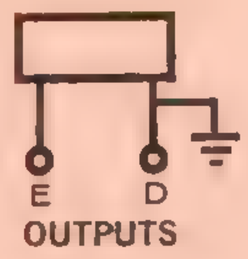
digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1562
−10 VOLT REFERENCE SUPPLY



The Type 1562 is a −10 volt shunt regulated, reference voltage supply. This supply is primarily used in digital-to-analog and analog-to-digital conversion systems, where a precision reference voltage is required. In this application, the Type 1562 supplies the reference voltage to the single-ended bridges or level amplifiers, which in turn drive the ladder networks. In this application, a 500 microfarad capacitor should be placed across the output terminals.

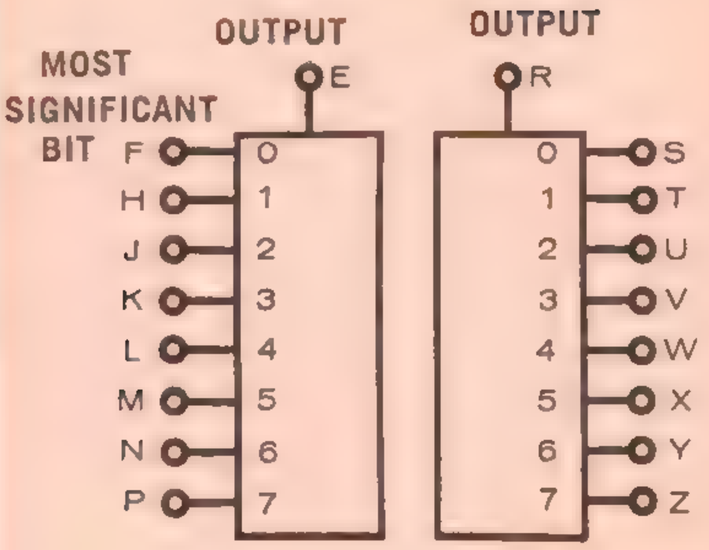
OUTPUT: The output may be in the range of −8 to −12 volts. At −10 volts, the maximum output current is ±60 ma, and the peak-to-peak ripple is less than 10 millivolts. In digital-analog conversion applications, this current is sufficient for driving up to two 14-bit digital-to-analog converter ladder networks, with an accuracy of 0.1% at constant temperature. The temperature coefficient of the Type 1562 is 2 millivolts /°C or 0.02% /°C.

POWER: −15 volts/100 ma; +10 volts (A)/0 ma; +10 volts (B)/10 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1563-1564
DIGITAL-TO-ANALOG CONVERTERS



1563 DIGITAL-TO-ANALOG CONVERTER

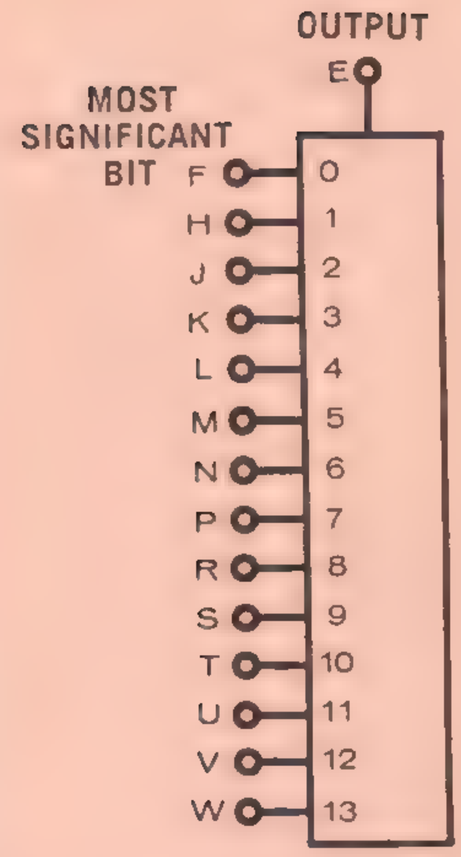
The Types 1563 and 1564 are digital-to-analog converters employing binary weighted resistor ladder networks. The Type 1563 contains two converters for up to 8 bits each. The Type 1564 contains one converter of up to 14 bits. The settling time of the networks is approximately 1 microsecond. The Types 1563 and 1564 are constructed from 0.1% wire wound resistors with a temperature coefficient of 20 ppm/°C. The potentiometers (of 20 ohms each) are used for adjusting the 8 most significant bits from the Type 1564 and the 4 most significant bits of each ladder in the Type 1563. The Type 1954 Module Extender should be used during potentiometer adjustment.

The wire wound ladders are the most accurate converters of the five types manufactured by DEC; however, they also have the longest settling time. A table showing the characteristics of the different ladder networks is included with the Type 1561 product bulletin. Additional information on digital-to-analog and analog-to-digital conversion techniques is available in the form of special applications bulletins. This information may be obtained from any DEC sales office or sales representative.

INPUT: The input impedance is 3000 ohms. The inputs are normally driven from DEC Single-Ended Bridges with 0 and −10 volt levels. When accuracy requirements permit, level amplifiers such as the Types 4667 or 1667 may be used, with the more negative voltage level in the range of −3 to −10 volts. When an accuracy of three bits or less is required, the input may be driven by DEC Standard Levels of 0 and −3 volts. The input current will vary from 0 to ±1ma (±1 unit Base Load) depending on the state of the ladder. Inputs not in use should be grounded.

OUTPUT: The output impedance is 1000 ohms. The maximum open circuit output voltage is equal to the more negative input level less the value of of the least significant bit.

POWER: −15 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

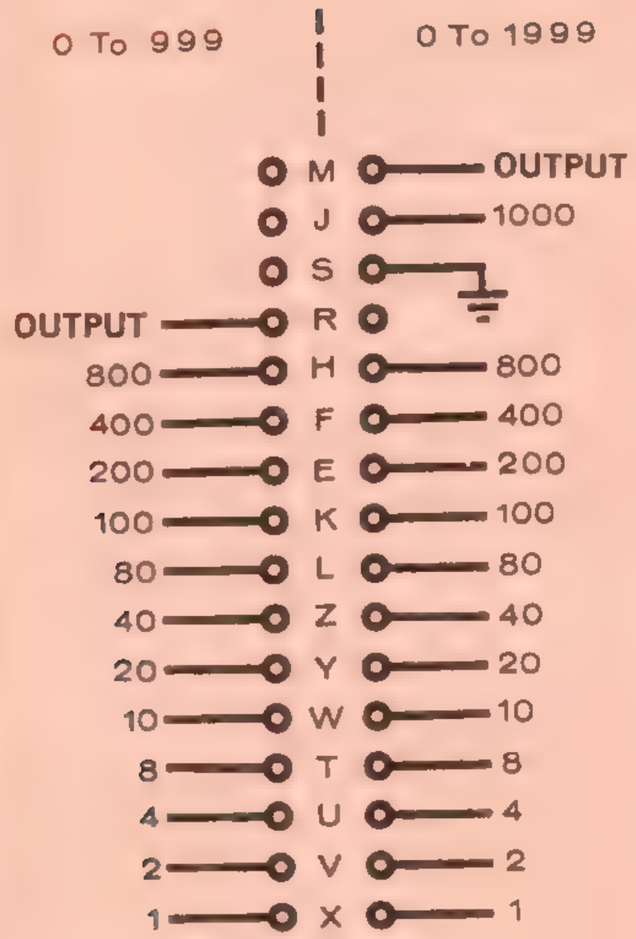


1564 DIGITAL-TO-ANALOG CONVERTER

d i g i t a l

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1566
BCD DIGITAL-TO-ANALOG CONVERTER



The Type 1566 contains a special weighted resistor ladder network for converting binary coded decimal information (8 4 2 1 code) into an analog voltage. The converter has a capacity of up to 3 decimal digits plus 1 optional bit; that is, 0 to 999, 0 to 1999, or +999 to −999. The settling time for the ladder network is approximately 2.5 microseconds. The Type 1566 is constructed from 0.1% wire wound resistors with temperature coefficients of 20 ppm/°C. The potentiometers (of 20 ohms each) are used for adjusting the eight most significant bits (including the optional bit). The Type 1554 Module Extender should be used to permit potentimeter adjustment.

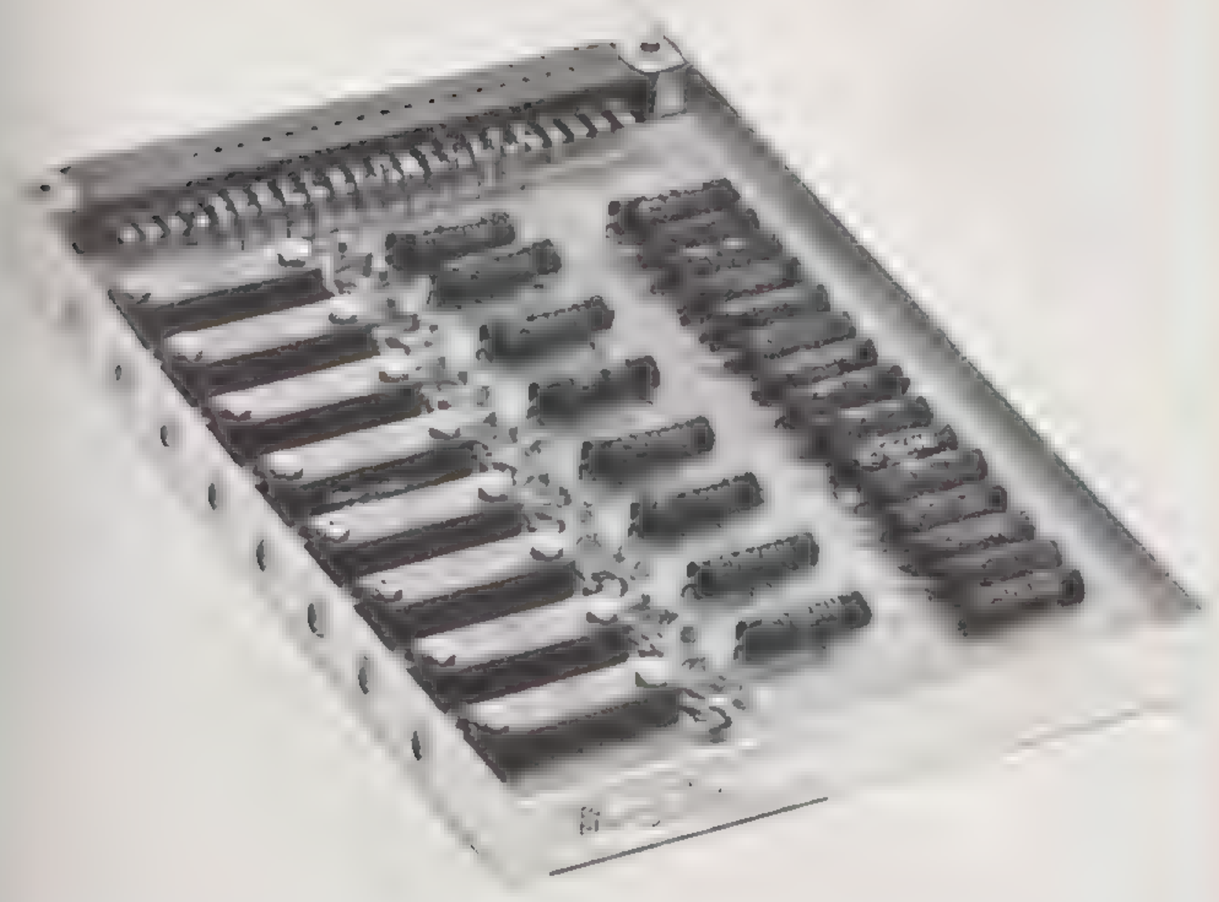
A table showing the characteristics of different ladder networks is included with the Type 1561 product bulletin. Additional information on digital-to-analog and analog-to-digital conversion techniques is available in the form of special application's bulletins. This information may be obtained from any Digital sales office or sales representative.

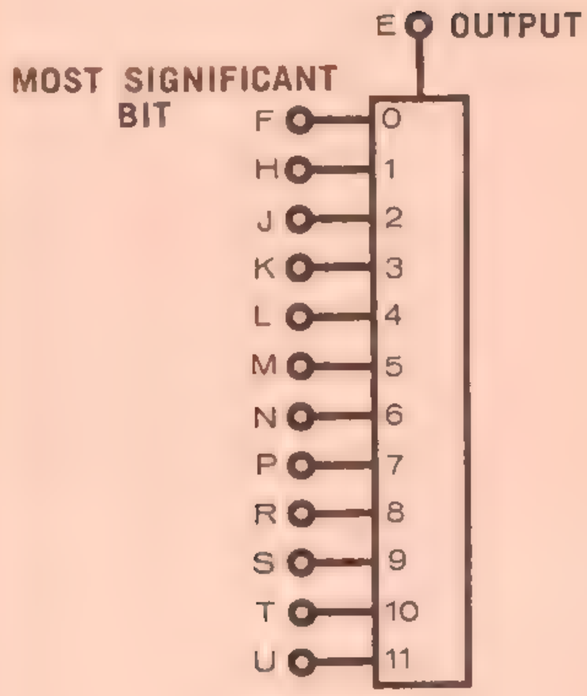
INPUT: The inputs are identical to the Type 1561, except in that the information should be in binary-coded-decimal form instead of binary. The diagram above shows the different connections used for 0 to 999 and 0 to 1999. Unused digits should be grounded; that is, T, U, V, and X should be grounded for 0 to 99 and 0 to 199.

OUTPUT: The output impedance is 900 ohms with the 0 to 999 connection, and 950 ohms with the 0 to 1999 connection. The maximum open circuit output voltage is 62% of the more negative input voltage level.

POWER: −15 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

1568
DIGITAL-TO-ANALOG CONVERTER





The Type 1568 contains a binary weighted resistor ladder network which will convert up to twelve bits of binary information into an analog voltage. The settling time of the network is approximately 0.3 microsecond. The Type 1568 is constructed of 0.5% metal film resistors with a temperature coefficient of ±50 ppm/°C. Potentiometers (of 50 ohm each) are available for adjusting the eight most significant bits of the ladder.

The Type 1568 is intended to bridge the gap between the fast, but less accurate, carbon ladder, Type 1561, and the slow, but accurate, wire wound ladders. A table showing the characteristics of all ladder networks is included with the Type 1561 product bulletin. Additional information on methods of analog-to-digital and digital-to-analog conversion is available in special bulletins which may be obtained from any DEC sales office or sales representative.

INPUT: The input impedance is 3000 ohms. The inputs are normally driven from DEC Single-Ended Bridges with 0 and −10 volt levels. When accuracy requirements permit, level amplifiers such as the Types 4667 or 1667 may be used, with the more negative voltage level in the range of −3 to −10 volts. When an accuracy of three bits or less is required, the input may be driven by DEC Standard Levels of 0 and −3 volts. The input current will vary from 0 to ±1ma (±1 unit Base Load) depending on the state of the ladder. Inputs not in use should be grounded.

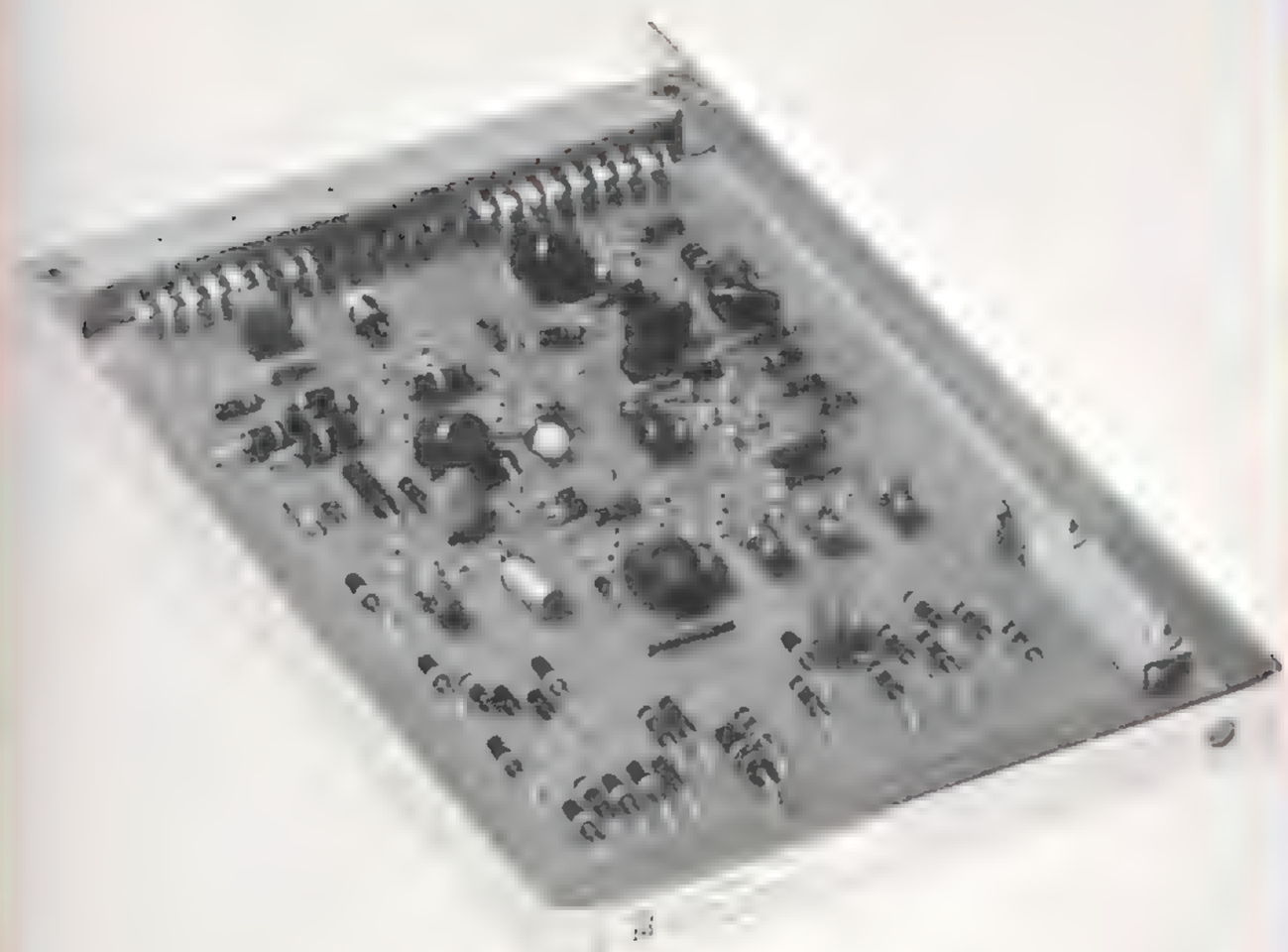
OUTPUT: The output impedance is 1000 ohms. The maximum open circuit output voltage is equal to the more negative input voltage level, minus the value of the least significant bit.

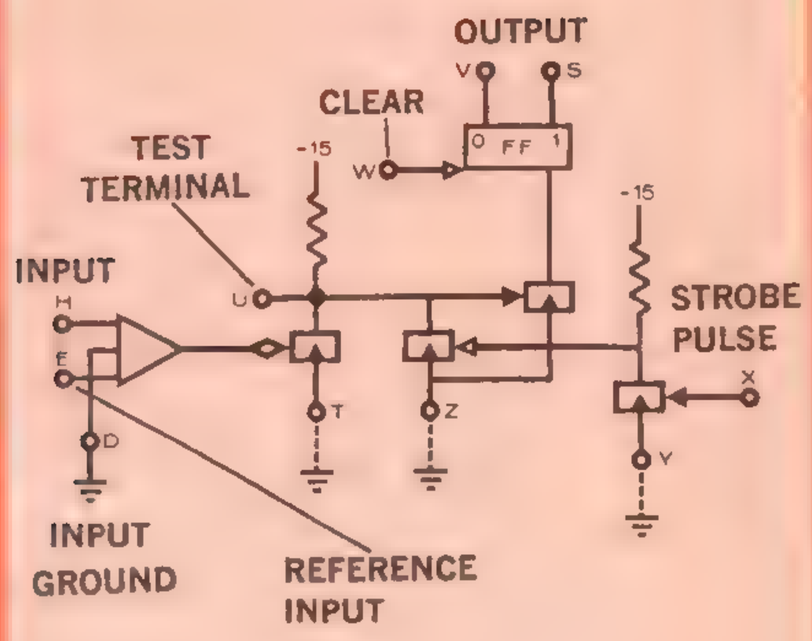
Power: −15 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

d g t l

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1570
SLICER FLIP-FLOP





The Type 1570 is used to compare the output pulses from memory elements such as ferrite cores (amplified by X10 amplifier 1550 or 1554) with a calibrated DC reference level. The slicer output is determined by the voltage difference between the input terminals E and H. An external strobe is ANDed with the slicer output and, if input terminal H is more negative than terminal E at the time of the strobe, the flip-flop in the circuit is set to the ONE state. An external clear signal is required to clear the flip-flop.

The slicing section and internal flip-flop will respond to a 15 nanosecond 50 millivolt negative signal where the pulse width is measured at the 50% point and the reference level is at −25 millivolts. In order to prevent loading of the high speed section of the circuit, the flip-flop buffers are not provided with overdrive and hence respond slowly. The total transition time is less than 1.7 microseconds.

INPUT: A 5 millivolt difference saturates the output transistor of the slicing section. The input current required at pin H is 0.4 ma when pin H is more negative than pin E, otherwise the current is 5 microamperes. A DEC Standard 70 nanosecond or wider Positive Pulse applied to pin W, is required to clear the flip-flop.

To prevent the strobe pulse and the flip-flop switching transients from getting into the amplifier input, separate grounds have been provided for the various sections of the module. The input ground is pin D, the amplifier output inverter ground is pin T, the strobe inverter is grounded on pin Y, and the rest of the circuit is grounded through pin Z. Pins T, Y, and Z may be grounded together, but pin D must be grounded separately.

OUTPUT: The flip-flop outputs are DEC Standard Levels capable of driving up to 1½ units of DC Emitter Load and 3 units of Base Load.

CONTROLS: The slice section is balanced by grounding pins E and H, applying −2.5 volts DC to pin X and adjusting the slice balance potentiometer. When the slicer is unbalanced the test terminal will be

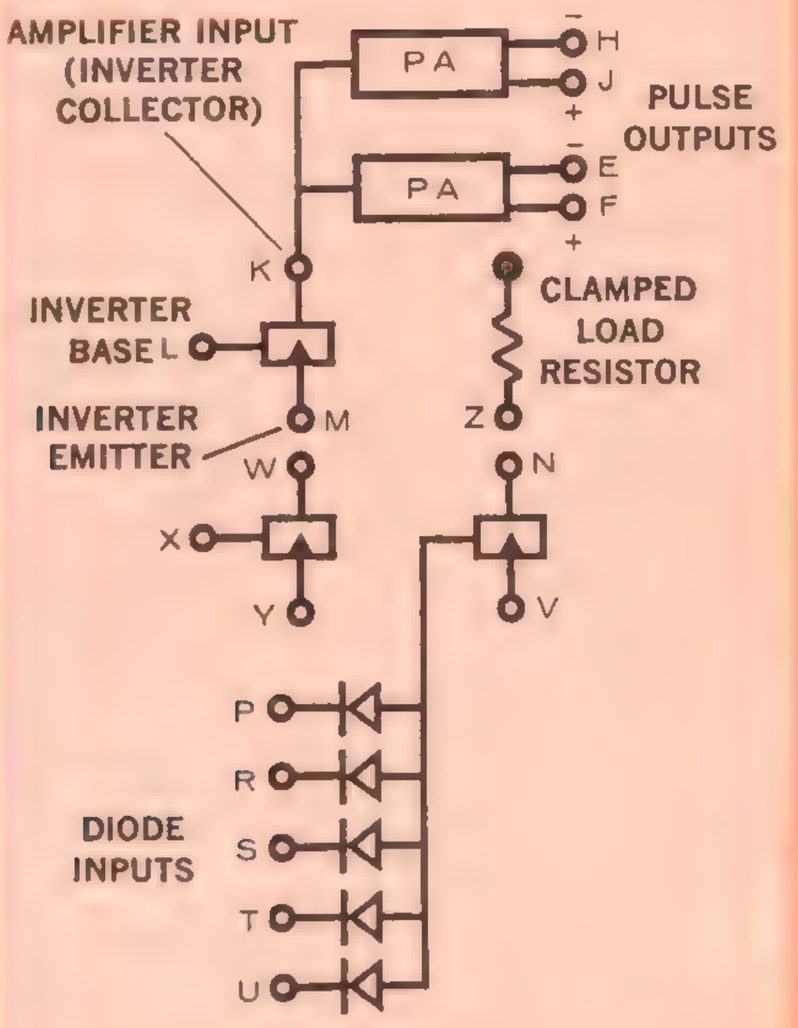
either ground or −1 volt. When it is balanced, the test terminal output will be in the region of −½ volt. Any load applied to the test terminal slows down the circuit; therefore, nothing should be connected to the test terminal while the circuit is operating.

POWER: −15 volts/80 ma; +10 volts (A)/0.5 ma; +10 volts (B)/18.5 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1606
DUAL PULSE AMPLIFIER



The Type 1606 contains a dual output pulse amplifier for standardizing DEC Standard Pulses in amplitude and width. Each of the two output circuits have the same driving ability as a standard pulse amplifier. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 5 megacycles. Two inverters and a five-input negative diode NOR are available for conveniently mixing pulse inputs from several sources. They may also be used for input level gating or in other portions of the system.

INPUT: The input to the pulse gate, whose collector drives the pulse amplifier (it may pass through some level gates on the way), is normally a DEC Standard 70 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 50 nanoseconds and width (at 2 volts) greater than 50 nanoseconds can be used. Input pulses of less than −0.5 volts will not generate an output pulse. Many pulse gate collectors can be connected together to mix pulse sources. If the emitter of any pulse gate is conditioned by the output of a level gate, a load resistor must be connected to the emitter of the pulse gate (ex.: connect M to Z). The two pulse gates are inverters like those included in the DEC Inverter Type 1105. The diode unit is similar to that in the DEC Type 1110.

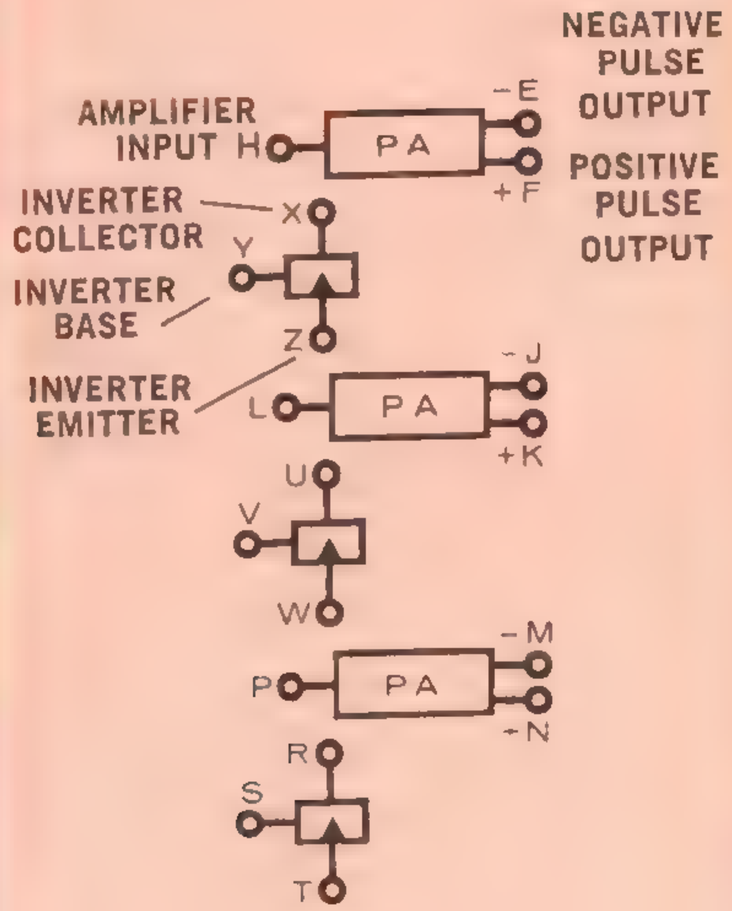
OUTPUT: The output is a DEC 2.5 volt, 70 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. Each pulse amplifier output is an independent transformer winding, which may be used to produce positive or negative pulses by grounding the appropriate terminal. Transformers may be connected in parallel to increase the driving power or in series to increase the pulse amplitude for driving external devices. Each output is capable of driving 16 units of Pulse Load.

POWER: −15 volts/90 ma; +10 volts (A)/0.88 ma; +10 volts (B)/.70 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1607
PULSE AMPLIFIER



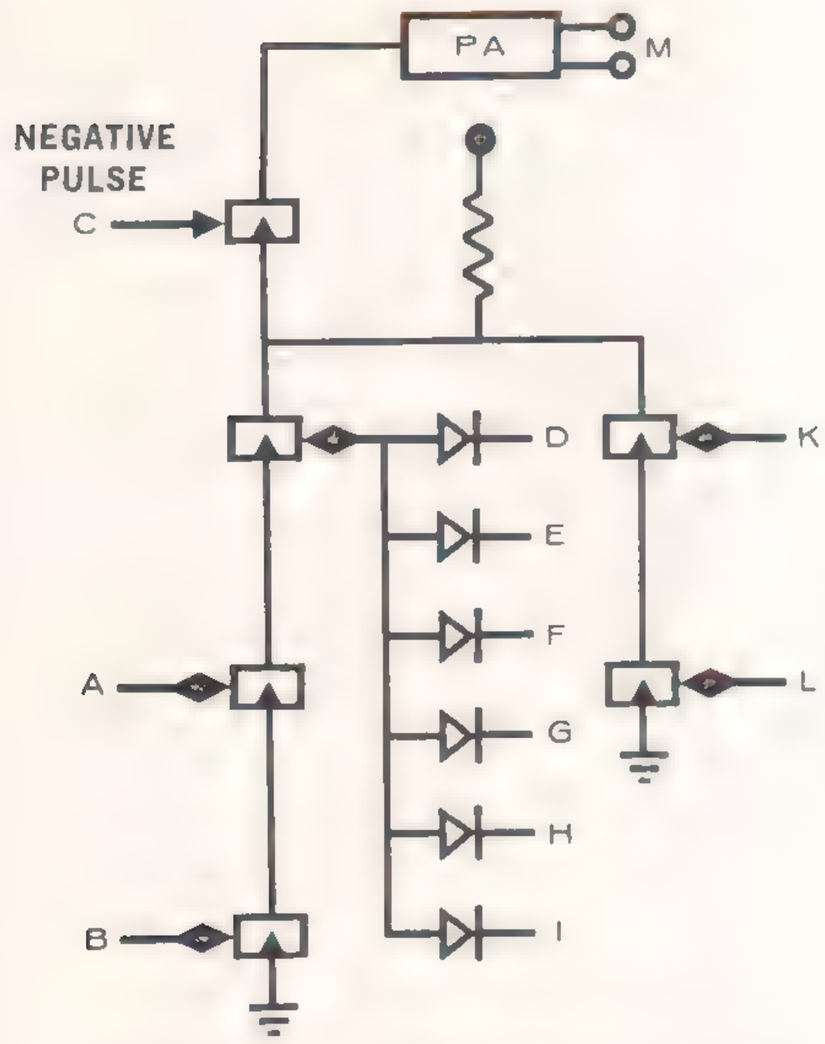
The Type 1607 contains three pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Three standard inverters are included for gating the input. The inverters are similar to those in the DEC Inverter Type 1105. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 5 megacycles. The DEC Diode Type 1110 may be used in conjunction with the pulse amplifier for conveniently mixing pulses from several sources.

INPUT: The input must come from the collector of one or more pulse gates. The signal on the base of the pulse gate is normally a DEC Standard 70 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 50 nanoseconds and width (at 2 volts) greater than 40 nanoseconds can be used. Input pulses of less than —0.5 volts will not generate an output pulse. Many pulse gate collectors can be connected together to mix pulse sources. The two pulse gates are inverters like those included in the DEC Inverter Type 1105.

OUTPUT: The output is a DEC Standard 2.5 volt, 70 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. The pulse will be negative if the positive output is grounded; it will be positive if the negative output is grounded. Each output is capable of driving 16 units of Pulse Load.

POWER: —15 volts/136 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.15 ma.

LOGICAL GATING



$$M = C[A \cdot B(D + E + F + G + H + I) + K \cdot L]$$

Figure 1 — PULSE AMPLIFIER GATING

When a large amount of gating must be performed in several places, it is often economical to perform this gating before a pulse amplifier. The output pulse may then go directly to flip-flops and other pulsed units with the same results as if the gating had been performed at each unit being pulsed. Figure 1 illustrates a typical gated pulse amplifier.

For more information on mixed systems, see "Integrating Different Series of DEC Modules."

PULSE STANDARDIZING

DEC Pulse Amplifiers are also useful in providing compatibility between the different series of DEC Modules. Since the modules are designed with compatibility in mind, the only differences between frequency lines are in the timing characteristics. In particular, pulses in the 10 megacycle line have a duration of 40 nanoseconds in the 5 megacycle line, 70 nanoseconds; and in the 500 kilocycle line, 400 nanoseconds (0.4 microseconds).

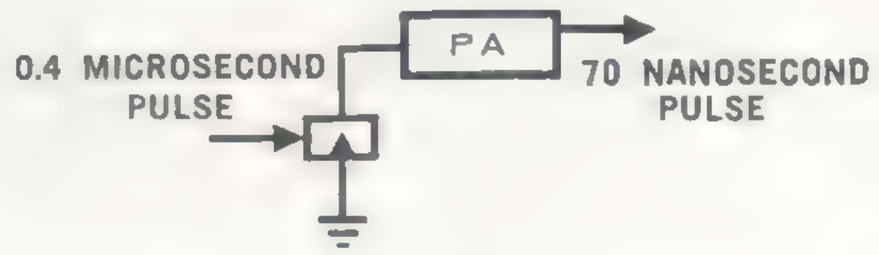


Figure 2 — REDUCING PULSE DURATION

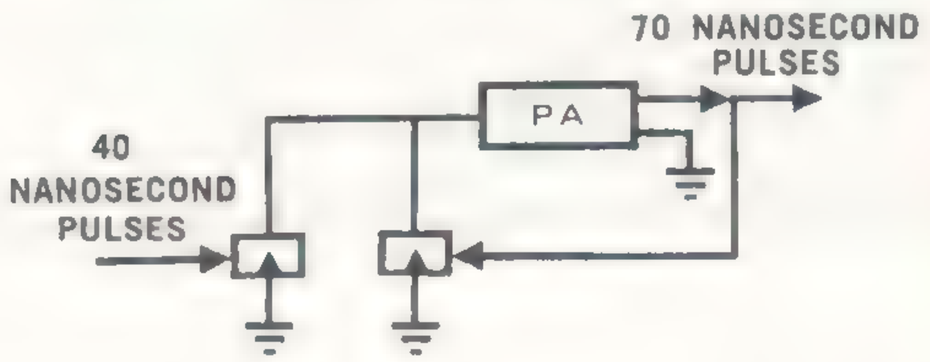


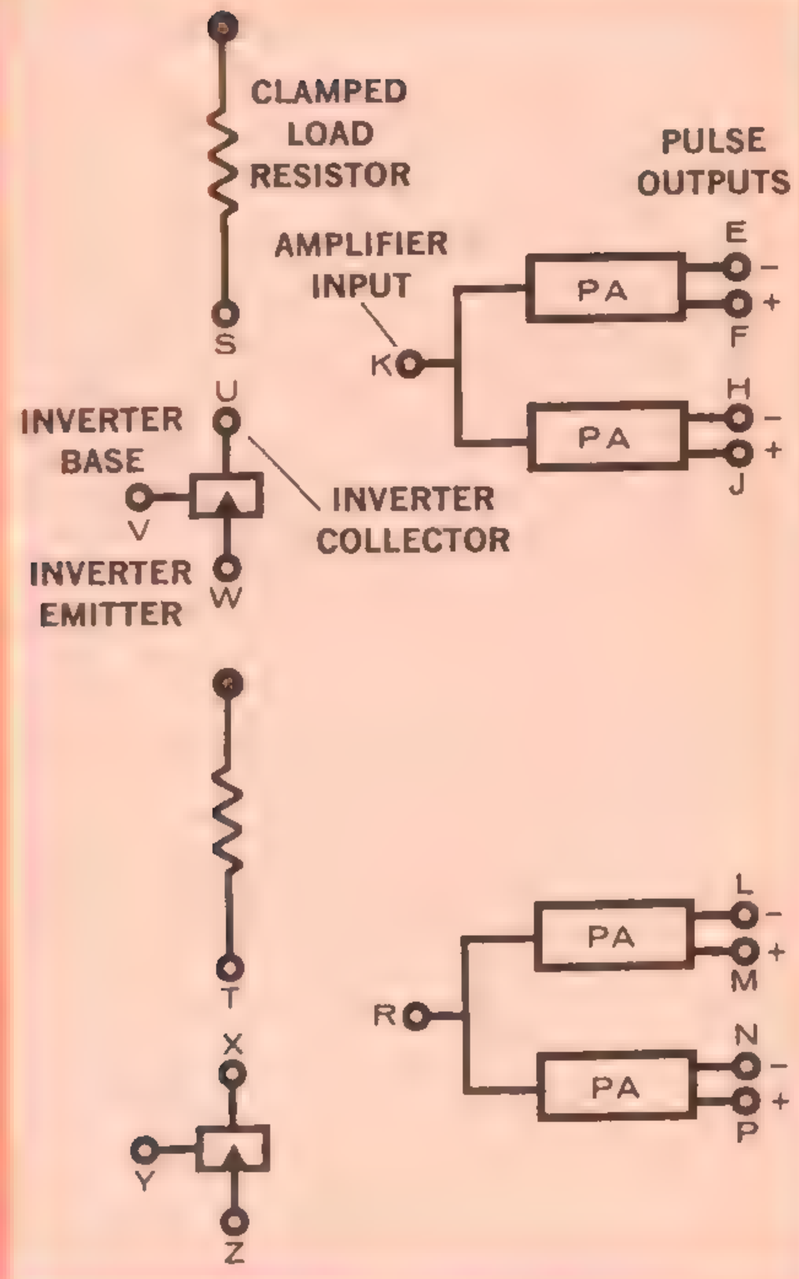
Figure 3 — INCREASING PULSE DURATION

To produce a 70 nanosecond pulse from an 0.4 microsecond pulse, the Type 1607 Pulse Amplifier is used, as shown in Figure 2. To produce a 70 nanosecond pulse from a 40 nanosecond pulse, the Type 1607 is used with a feedback loop. This method, as shown in Figure 3, produces a full duration pulse, but reduces the output driving ability slightly.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1608
DUAL PULSE AMPLIFIER



The Type 1608 contains two dual output pulse amplifiers for standardizing DEC Standard Pulses in amplitude and width. Flexible gated inputs are available through use of two inverters for multiple input level gating of input pulses or for mixing pulses. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may ocur at any frequency up to 5 megacycles. The DEC Diode Type 1110 may be used in conjunction with the pulse amplifier for conveniently mixing pulses from several sources.

INPUT: The input to the pulse gate, whose collector drives the pulse amplifier (it may pass through some level gates on the way), is normally a DEC Standard 70 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 50 nanoseconds and width (at 2 volts) greater than 50 nanoseconds can be used. Input pulses of less than −0.5 volts will not generate an output pulse. Many pulse gate collectors can be connected together to mix pulse sources. The two pulse gates are inverters like those included in the DEC Inverter Type 1105.

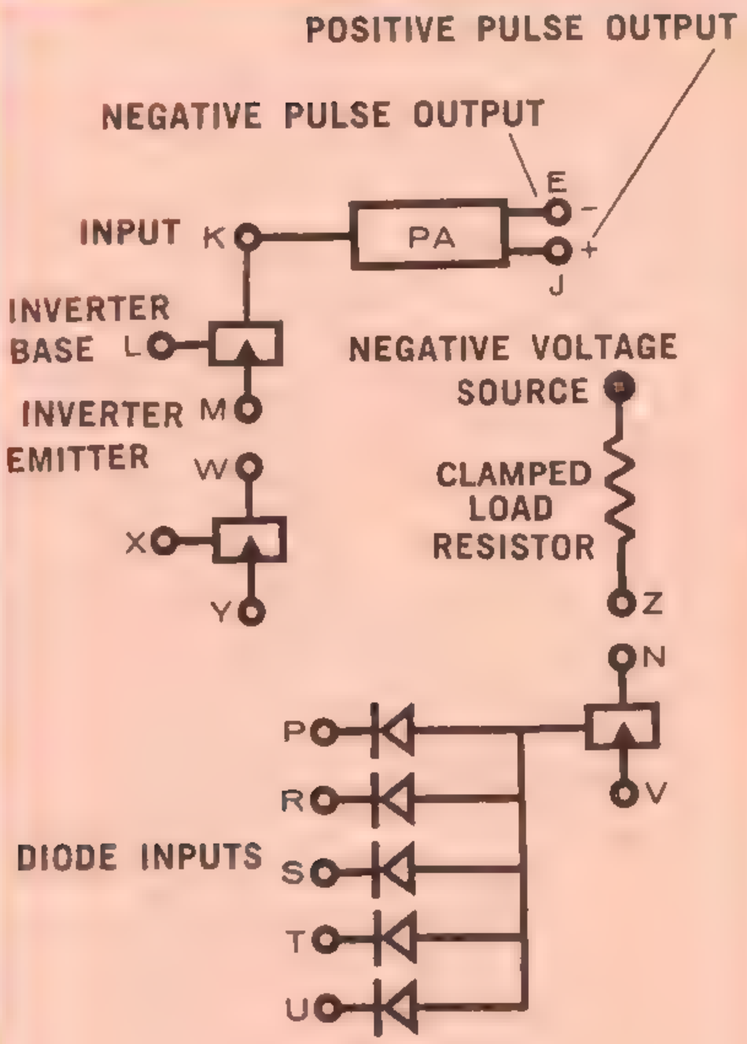
OUTPUT: The output is a DEC 2.5 volt, 70 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. Each pulse amplifier output is an independent transformer winding, which may be used to produce positive or negative pulses by grounding the appropriate terminal. Transformers may be connected in parallel to increase the driving power or in series to increase the pulse amplitude for driving external devices. Each output is capable of driving 16 units of Pulse Load.

POWER: −15 volts/160 ma; +10 volts (A)/0.15 ma; +10 volts (B)/0.15 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1616
OUTPUT PULSE AMPLIFIER



The Type 1616 contains one pulse amplifier which produces 5 volt, 0.5 microsecond pulses for driving external devices. Flexible input gating is available through the use of the two inverters or the five input diode gate contained in the package. The two inverters are similar to those in the DEC Inverter Type 1105. The diode gate is similar to that in the DEC Diode Gate Type 1110 and may be used for mixing negative pulse inputs. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 500 kilocycles.

INPUT: The input to the pulse amplifier must be negative and have a minimum amplitude of —2.0 volts and a maximum of —5.0 volts and should approach the general rise and fall time characteristics of DEC Standard Negative Pulses. Input pulses of less than —0.5 volts will not generate an output pulse. The input pulse must be applied to the base of an inverter. Inverter collectors can be connected together to mix many pulse sources. If the emitter of any pulse gate is conditioned by the output of a level gate, a load resistor must be connected. Another application of the diode circuit is for making a five input positive AND circuit. By use of the remaining inverter contained in the unit, this diode circuit can control the pulsing of the pulse amplifier.

OUTPUT: Each time the input requirement is met, the pulse amplifier will produce a 5 volt, 0.5 microsecond pulse into a 100-ohm load. Pulse outputs may be made either positive or negative by grounding the appropriate output terminal.

POWER: —15 volts/60 ma; +10 volts (A)/1.2 ma; +10 volts (B)/0.9 ma.

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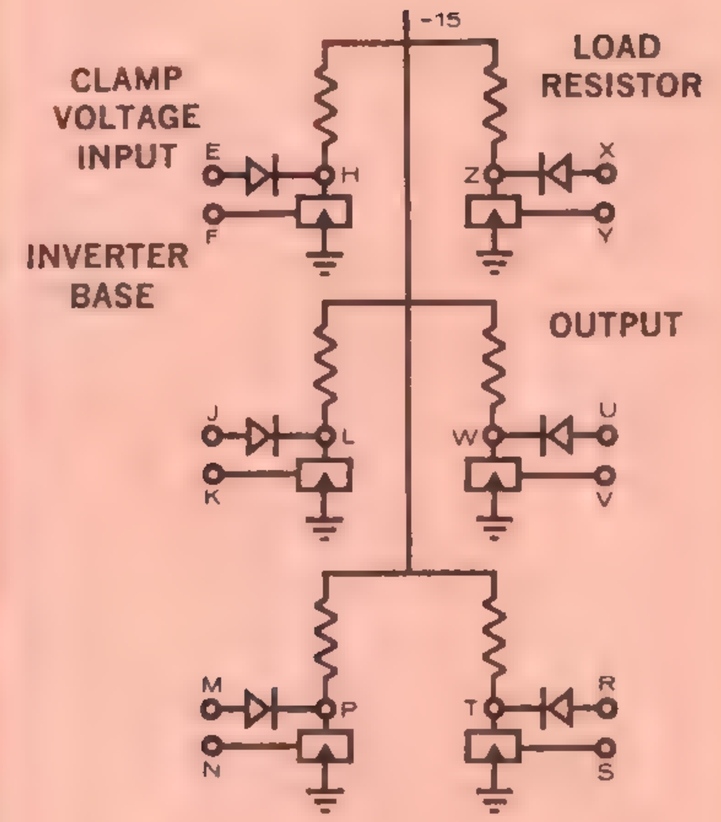
digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1667
LEVEL AMPLIFIER



The Type 1667 contains six grounded emitter inverters which amplify DEC Standard Levels into 15 volt Negative Levels. Clamping diodes connected to each inverter collector are brought out to the plug and may be returned to any voltage between ground and −15 to obtain any desired output level within this range. Delay through an amplifier is approximately 0.05 microsecond.

INPUT: The base input is DEC Standard Levels or equivalent (1 unit of Base Load). When the base is at ground level, the output is at −15 volts. When the base is at −3 volts, the output is at ground level.

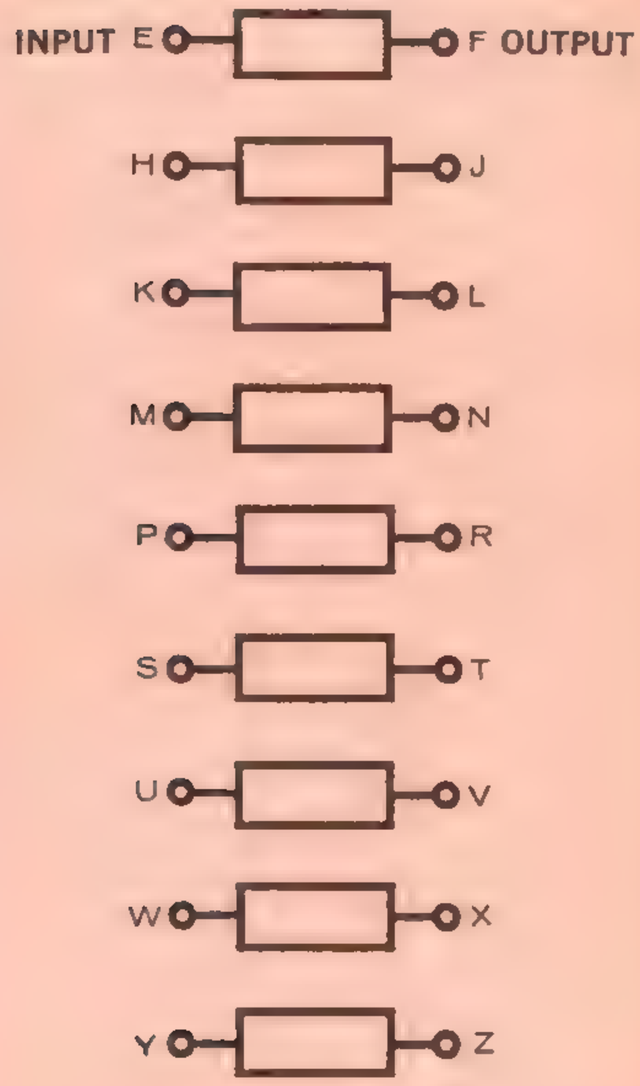
OUTPUT: The upper output level is ground. The lower output level is determined by the external supply attached to the clamp diodes, and must be in the range of ground to −15 volts. When the output signal is at ground, each inverter will supply up to 5 ma to external circuitry. When the output level is negative, the maximum current which can be accepted is determined by a 1500-ohm resistor to −15 volts.

POWER: −15 volts/60 ma; +10 volts (A)/0.44 ma. +10 volts (B)/0.44 ma.

digital

1000 SERIES
SYSTEM MODULES

1669
INDICATOR DRIVER



The Type 1669 contains nine transistor amplifiers capable of driving an indicator panel of miniature incandescent bulbs. It is ideal for providing remote indicators from DEC System Module Flip-flops. The indicator lights are on whenever the inputs to their respective amplifiers are −3 volts; if the input is from a flip-flop, it indicates a ONE state.

INPUT The input requires DEC Standard Levels or equivalent and represents 1 unit of Base Load (no capacitance).

OUTPUT Each output is suitable for driving a Type 327 28-volt indicator lamp that is returned to −15 volts. Other loads may be driven, providing the required current is no greater than 30 ma and the voltage no greater than −20 volts.

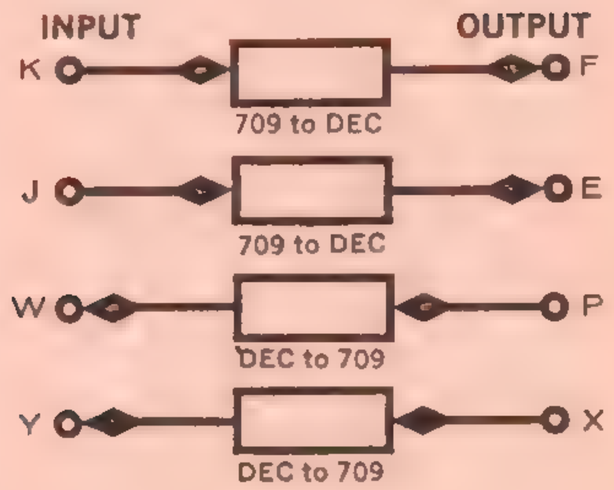
POWER +10 volts (A)/1.3 ma; +10 volts (B)/0 ma; −15 volts/270 ma*.

*This voltage is not supplied to this unit; this is the current drawn by the remote lamps from −15 volts when they are all turned on.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1672
709 CONVERTER



DEC Module Tvpe 1672 provides signal compatibility between the IBM 709 Electronic Data Processor and DEC Modules. Input-output buffers, data handling, and control equipment constructed with DEC equipment can be easily connected to the input-output bus of an IBM 709 Electronic Data Processor. Each Type 1672 plug-in-unit contains four independent circuits (two 709-to-DEC circuits and two DEC-to-709 circuits). These are normally used in pair to provide two-way communication with the IBM 709 input-output bus.

INPUT: 709-TO-DEC CIRCUITS — The upper level needs to be more positive than +5 volts, and the lower level more negative than −20 volts. There is no limit on rise and fall times. Input impedance may be approximated by 270,000 ohms and 15 pf to ground.

DEC-TO-709 CIRCUITS — DEC Standard Levels of 0 and −3 volts drive this part of the circuit. The input load is 1 ma at ground input and no load at −3 volts input. There is a shunt capacitance of about 250 pf.

OUTPUT: 709-TO-DEC CIRCUITS — The output is 0 volts for +10 volts input, and is −3 volts for −30 volts input. The output can drive four units of Base Load and/or any number of Pulse Emitter Loads provided only one is pulsed at a time. With an input rise or fall time of ½ microsecond the output delay will be less than ½ microsecond and the output rise or fall time less than ¼ microsecond.

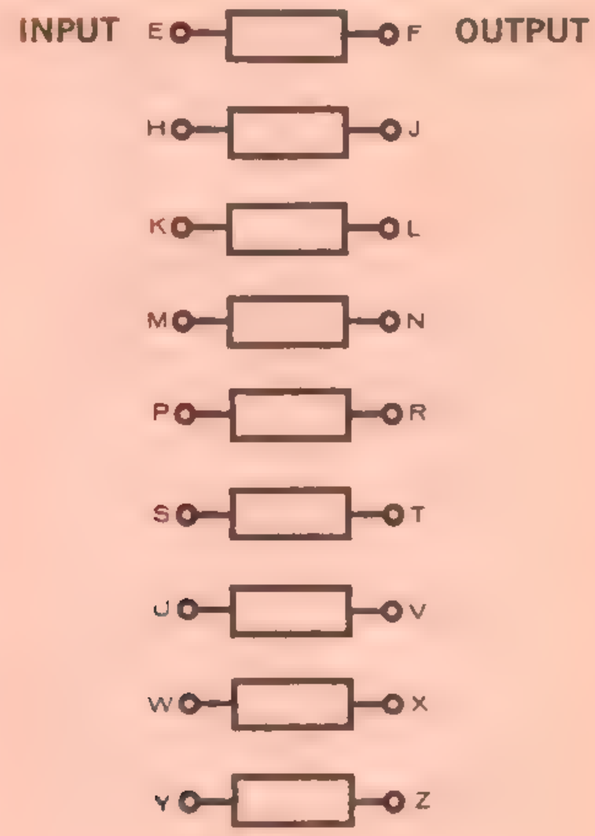
DEC-TO-709 CIRCUITS — The upper level will be more positive than +6 volts for a ground level input, and the lower level more negative than −26 volts for a −3 volt level input. The intended load is the 709 bus system. The DEC-to-709 circuit drives this load through a diode, and has no built-in load resistor of its own. The rise delay is less than ¼ microsecond and the rise time less than ½ microsecond. The fall delay is less than ½ microsecond and the fall time is limited by the shunt capacitance of the bus system. The DEC-to-709 circuit cannot drive the bus negatively since it drives the bus through a diode.

POWER: −15 volts/44 ma; +10 volts (A)/0.3 ma; +10 volts (B)/20 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1675
INDICATOR DRIVER



The Type 1675 contains nine transistor amplifiers each capable of driving a miniature incandescent bulb. It is ideal for providing remote indicators from DEC Flip-flops Types 4201, 1201, 1209, or 6202. The indicator lights are on whenever the flip-flop is in the ONE state.

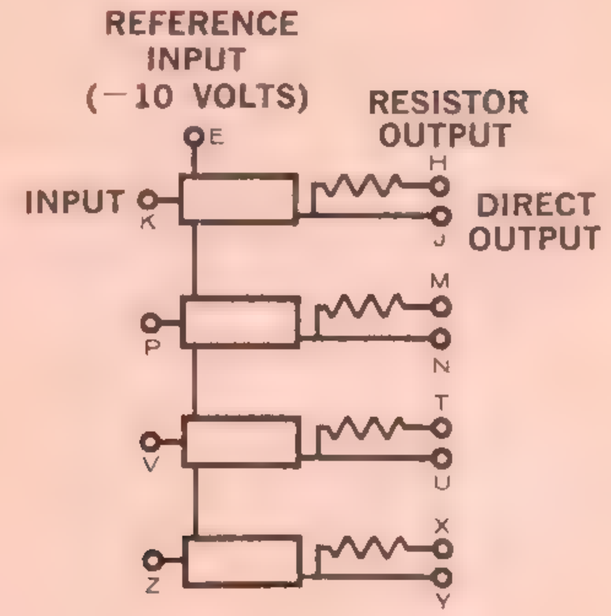
INPUT: The input is the base of a transistor inverter with no input resistor. It may be driven only by the resistor outputs of the DEC Flip-flops Types 4201, 1201, 1209, or 6202, or from any flip-flop that has a 3000-ohm resistor wired between it and the Type 1675. When an indicator driver is used, the driving ability of the flip-flop ONE output must be decreased by 1 unit Base Load.

OUTPUT: Each output is suitable for driving a Type 327 28-volt indicator lamp that is returned to −15 volts. Other loads may be driven, providing the required current is no greater than 30 ma and the voltage no greater than −20 volts.

POWER: +10 volts (A)/1.3 ma; +10 volts (B)/0 ma; −15 volts/270 ma.*

*This voltage is not supplied to this unit; this is the current drawn by the remote lamps from −15 volts when they are all turned on.

1677
SINGLE ENDED BRIDGE



The Type 1677 contains four single ended bridge amplifiers which are designed principally for driving DEC Digital-to-Analog Converter Networks. The amplifier may also be used as bus drivers. The output voltages for the amplifiers are ground and a negative voltage (of up to −10 volts). Similar amplifiers also useful for these purposes are the Types 4677 and 4677A.

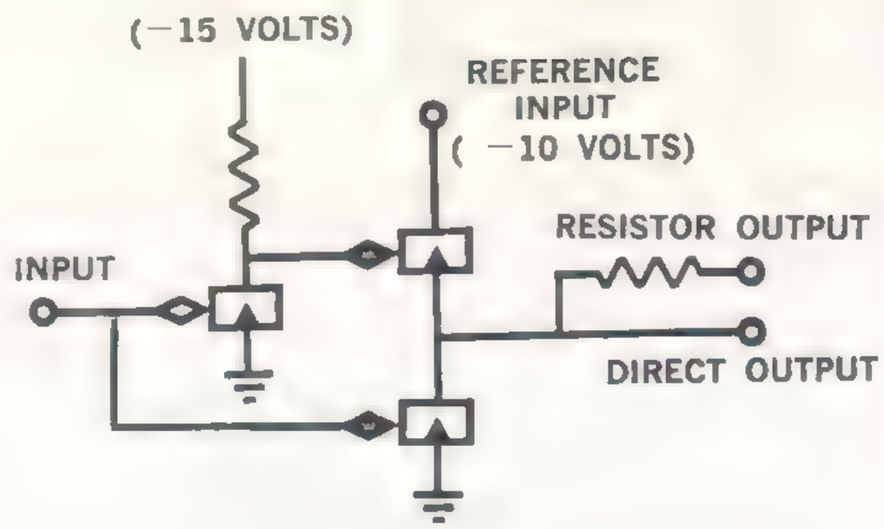
INPUT: The input signals are DEC Standard Levels or equivalent. Each input represents two units of Base Load.

POWER: The reference voltage supplies all output current plus a nominal amount for internal use. This voltage may be as great as −10 volts. When the amplifier is used in digital-to-analog conversion, −10 volts is recommended for the greatest accuracy. In this case, a maximum of ±13.2 ma will be required. For other applications the maximum current required should not exceed 120 ma total.

OUTPUT: A ground input gives a negative output. A −3 volt input gives ground output. Each output is available either directly or through a 100-ohm resistor. The direct output should always be used to drive digital-to-analog converters. (Either output may be used in driving the Type 1561 Digital-to-Analog Converter.) If the amplifier is to be used for any other purpose, the 100-ohm resistor outputs should be used in order to protect the transistor from accidental shorting to ground. Up to 15 ma can be supplied at the ground level and up to 30 ma at the reference level. The direct output terminal should never be shorted directly to any external voltage or ground.

Table 1 shows a summary of the different characteristics of the amplifier. Column I shows the variation in output impedance with the output connected through a resistor (greater than 3000 ohms) to −10 volts. Column II shows the variation in output impedance with the output at −10 volts and connected

through a resistor (greater than 3000 ohms) to ground. Column III shows the total transition time, measured from 10% of input to 90% of output.



SINGLE ENDED BRIDGE TABLE

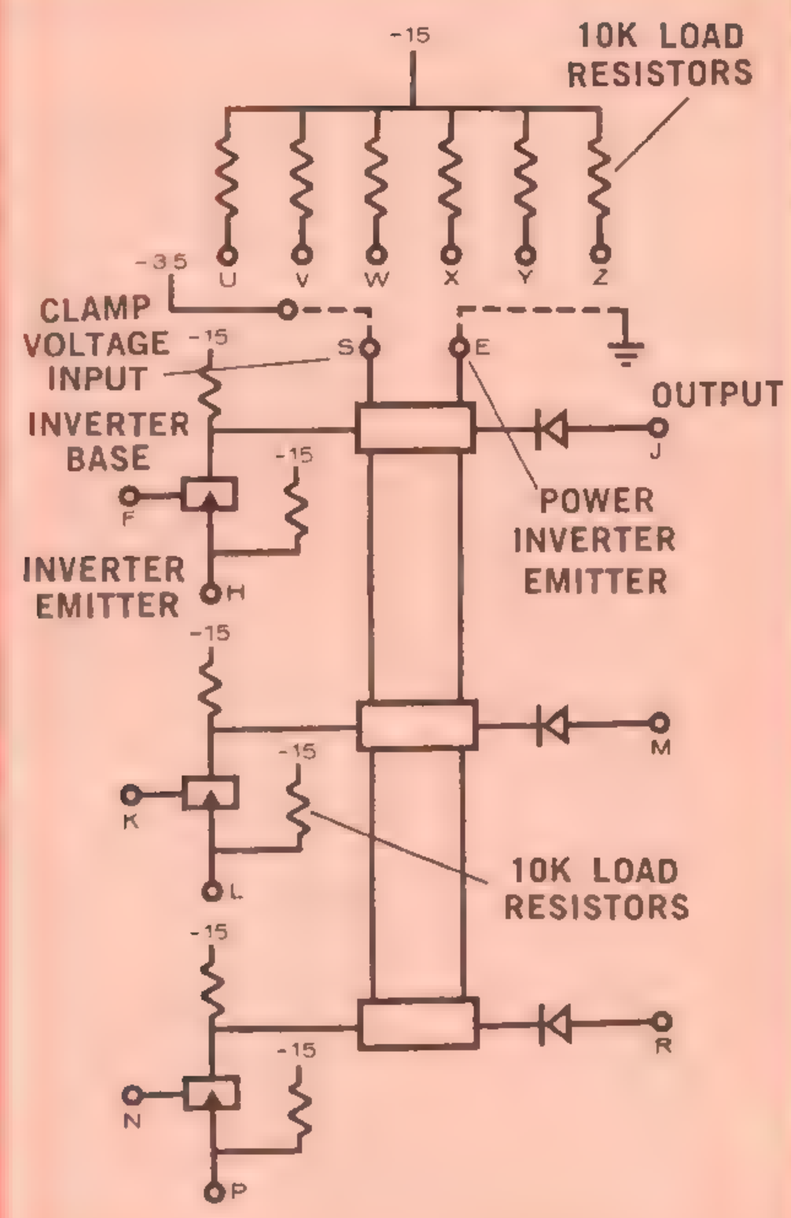
Type	To Reference Voltage (ohms)	To Ground (ohms)	Total Transition Time (microsecond)
1677	0 - 7	5 - 15	0.045
4677	1 - 5	4 - 9	0.2
4677A	0 - 3	1 - 3	1.5

POWER: −15 volts/40 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1678
BUS DRIVER



The Type 1678 contains three non-inverting bus drivers which provide high negative drive currents to heavy loads. This unit may also be used to amplify DEC Standard Levels, up to —12 volts, for driving external devices. Each circuit consists of a DEC Standard Inverter followed by a special power inverter. Both base and emitter inputs of the standard inverter are brought out to permit gating. The emitter has an attached 10K load, useful when it is part of an exclusive OR network.

The power inverter emitters are connected to a common external voltage which determines the more positive output level. The more negative output level is determined by an external clamp voltage. A fixed supply of —3.5 volts is provided within the module for connection to this point if desired. When the bus driver is operating with ground and —3.5 volt output levels, the total transition time is less than 100 nanoseconds.

Diodes in series with the output terminals prevent the Type 1678 from supplying positive drive; therefore, several circuits may be used in parallel to operate as a logical OR for negative signals. The module contains six 10,000 ohm resistors returned to —15 volts. These resistors are useful in constructing exclusive OR circuits from DEC Standard Inverters.

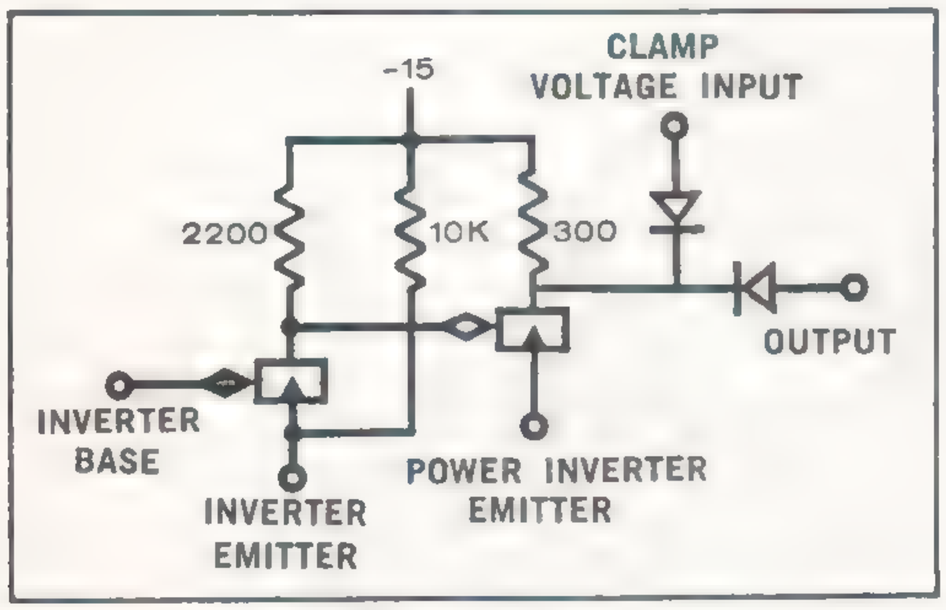
INPUT: The inputs to the standard inverter are DEC Standard Levels or equivalent. The base represents 1 unit Base Load, and the emitter represents 1 unit DC Emitter Load.

The power inverter emitters are brought out to a separate pin so that the upper output level may be varied, as a marginal check on the equipment that the bus driver is driving. The allowable voltage range of this input is +0.1 to —0.3 volts. It may be connected to ground if this feature is not desired. The clamp voltage input may be connected to the —3.5 volt terminal provided or to an external clamp voltage between —12 volts and ground. A 6.8 microfarad capacitor is internally connected from the clamp input to ground.

OUTPUT: Since each bus driver has a diode in series with the output, no current will be supplied to a positive return. Thus, several bus drivers may be ORed together to drive the same load.

Using the internal clamped load, each driver can generate −3.5 volts into a 100 ohm load. At other clamp voltages, and loads, the lower level is determined by the internal 300 ohm resistor returned to −15 volts, the output load, and the clamp voltage. The clamp voltage should be made no more negative than −12 volts.

POWER: −15 volts/200 ma; +10 volts (A)/0.35 ma; +10 volts (B)/0.5 ma.

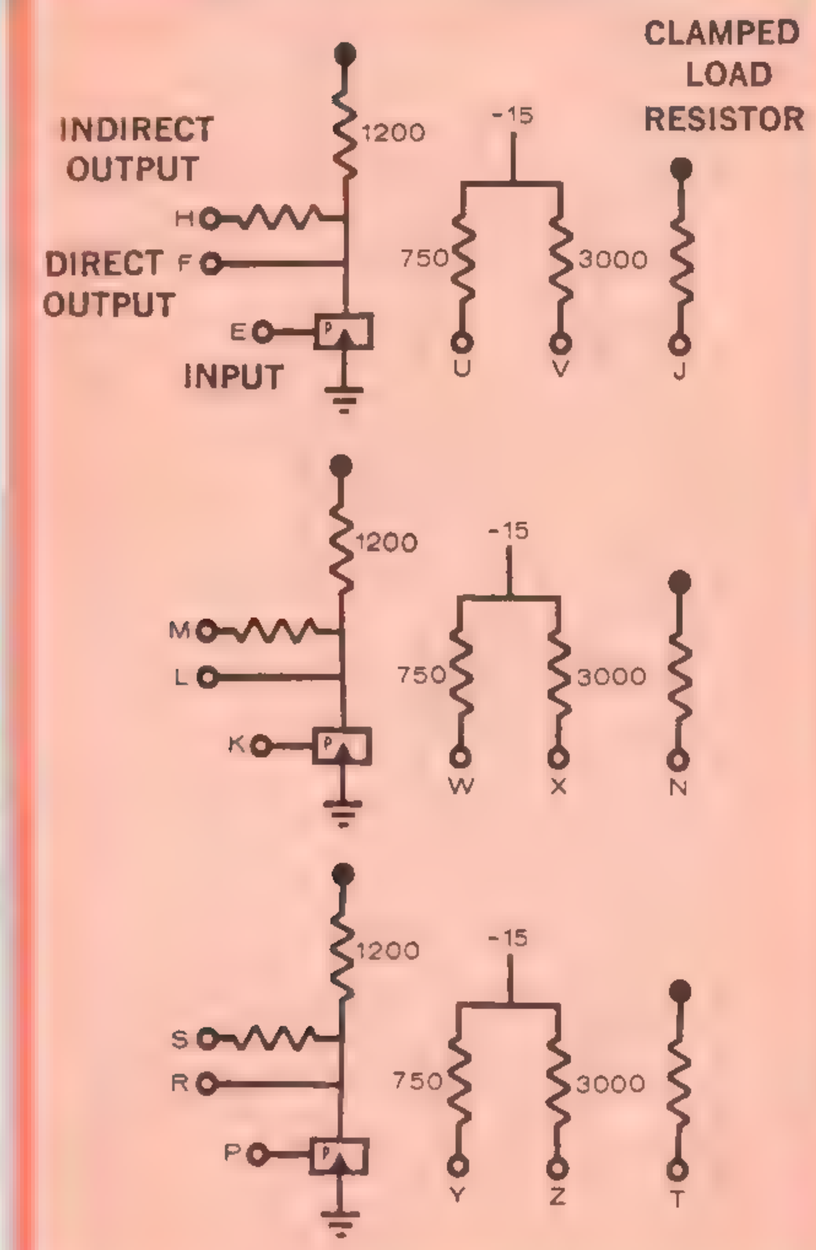


SCHEMATIC

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1681
POWER INVERTER



The Type 1681 contains three circuits, each similar to an ordinary inverter, except that the current level is higher. This module is used where a heavy load must be driven by Standard Logic Levels. The total transition time for output rise is less than 35 nanoseconds. For output fall, it is less than 45 nanoseconds.

INPUT: The inputs are DEC Standard Levels. Each input represents 3 units of Base Load.

OUTPUT: Both direct and indirect outputs are available from each power inverter. The indirect outputs (through 100-ohm resistors) may be used to drive coaxial cable so that the source end of the line may be terminated. The direct outputs are used for all other purposes.

The output driving ability of the Type 1681 is determined by the load resistors that are connected to the direct output. A 1200-ohm clamped load resistor is internally connected and the following additional loads are available: A 1500-ohm clamped load resistor, a 3000-ohm unclamped load resistor, and a 750-ohm unclamped load resistor. The following configurations may be used:

No external load resistors: The output driving ability is 3 units DC Emitter Load and 9 units Base Load.

3000-ohm load resistor: The output driving ability is 2½ units DC Emitter Load and 12 units Base Load.

1500-ohm clamped load resistor: The output driving ability is 2 units DC Emitter Load and 16 units Base Load.

3000-ohm load resistor and 1500-ohm clamped load resistor: Output driving ability is 1½ units DC Emitter Load and 19 units Base Load.

1500-ohm clamped load resistor and 750-ohm load resistor: The output driving ability is 30 units Base Load.

A power inverter may drive many units of Pulsed Emitter Load, providing only one is pulsed at a time. The DC Emitter loading should be decreased by one unit.

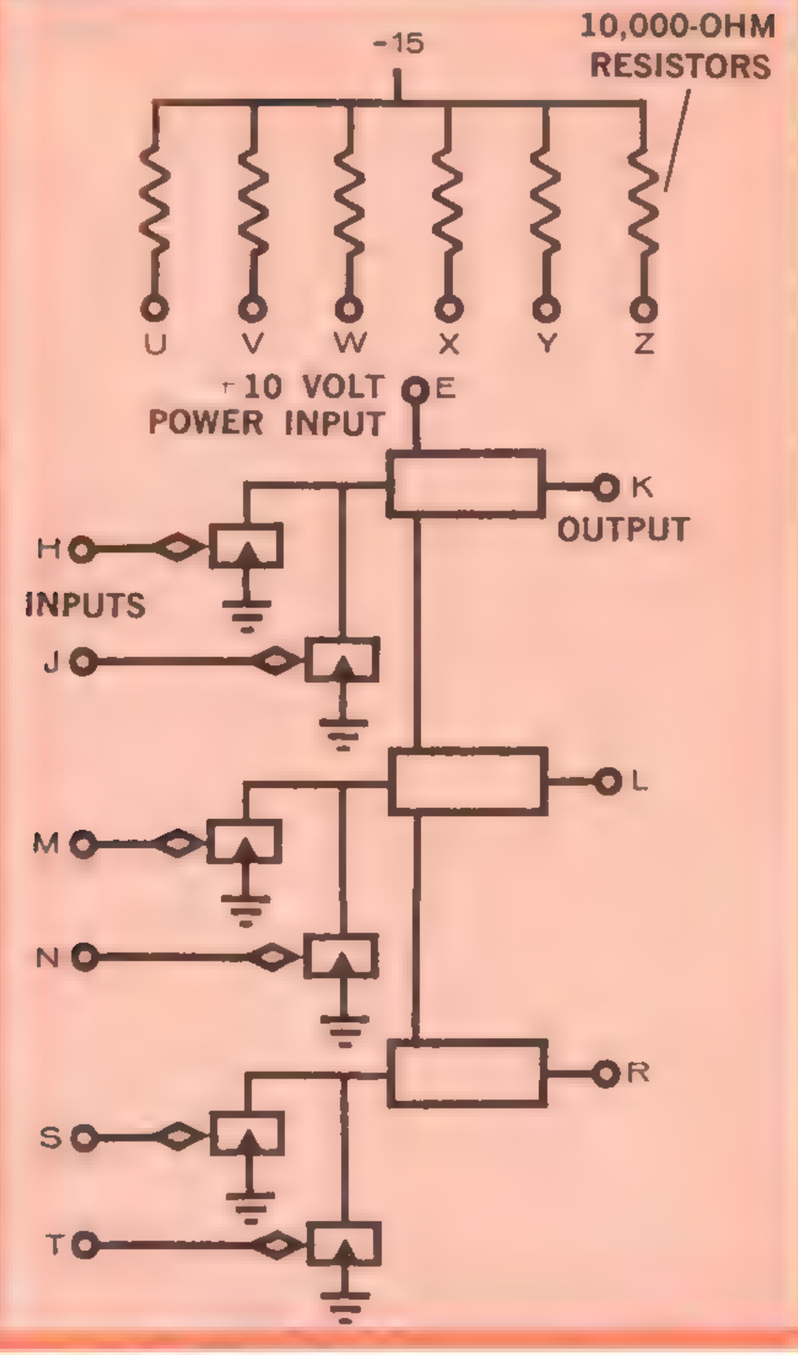
POWER: −15 volts/175 ma; +10 volts (A)/0.11 ma; +10 volts (B)/0.23 ma.

11 ma;

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1682
BUS DRIVER



Three identical circuits, each with two input inverters, are used as line or bus drivers. The two input inverters form an AND gate for ground inputs and an OR gate for negative inputs. Two ground inputs produce a +6 volt output capable of driving 75 ohms to ground; one or two negative inputs result in a grounded output. Six 10,000-ohm resistors, not part of the bus driver circuitry, are included in the package. These resistors are useful in forming exclusive OR circuits with inverters.

When driving a 75-ohm load, the total transition time for output fall is ≦400 nanoseconds; for output rise, the total transition time is ≦70 nanoseconds. The +6 volt level output may vary from 5.4 to 6.0 volts when the +10 volt supply is at exactly +10 volts. The lower level may vary from −0.2 to −0.3 volts under the same conditions.

INPUT: The inputs are DEC Standard Levels. Each input represents 1 unit Base Load. Power: a +10 volt source should be connected to pin E. This input requires 225 ma.

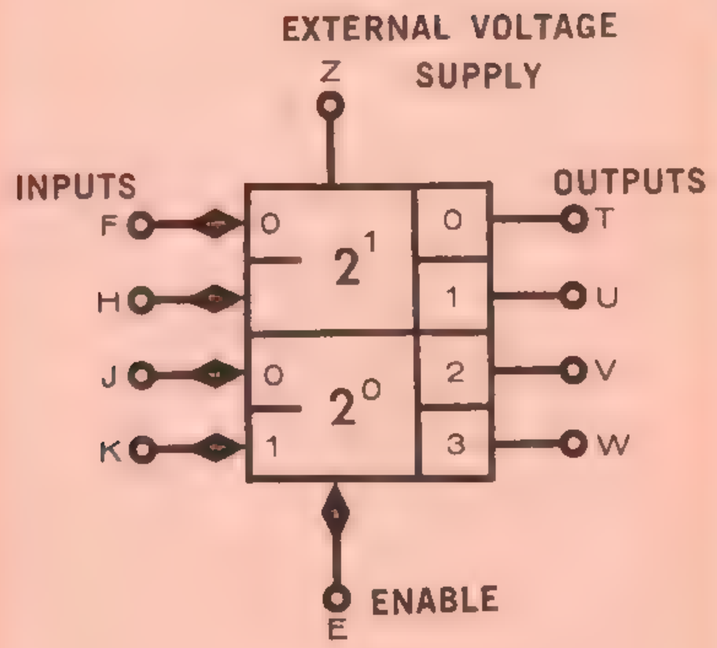
OUTPUT: Output levels are ground and +6 volts. The +6 volt level output can drive a 75-ohm load to ground.

POWER: −15 volts/76.5 ma; +10 volts (A)/0.9 ma; +10 volts (B)/0 ma; +10 volts (E)/225 ma.

digital

1000 SERIES
SYSTEM MODULES

1683
HALF-BINARY-TO-OCTAL DECODER



The Type 1683 decodes two flip-flops into four lines with the selected line at a positive voltage up to +60 volts. The lines not selected are at ground. A common enabling level is provided at pin E so that this unit may be used as one-half of a binary-to-octal decoder, if desired. The total transition time is 1.5 microseconds for output fall and 2.5 microseconds for output rise.

INPUT: DEC Standard Levels or equivalent drive the Type 1683. Each input terminal represents ¼ unit of DC Emitter Load. Pins F and H should be complementary levels, as should pins J and K. Pin E should be −3 volts or open circuited to enable the gates. The load presented at this point is ¼ unit of DC Emitter Load. A positive voltage (+60 volts maximum) must be connected to pin Z to determine the positive output level. The load is equivalent to 3000 ohms to ground.

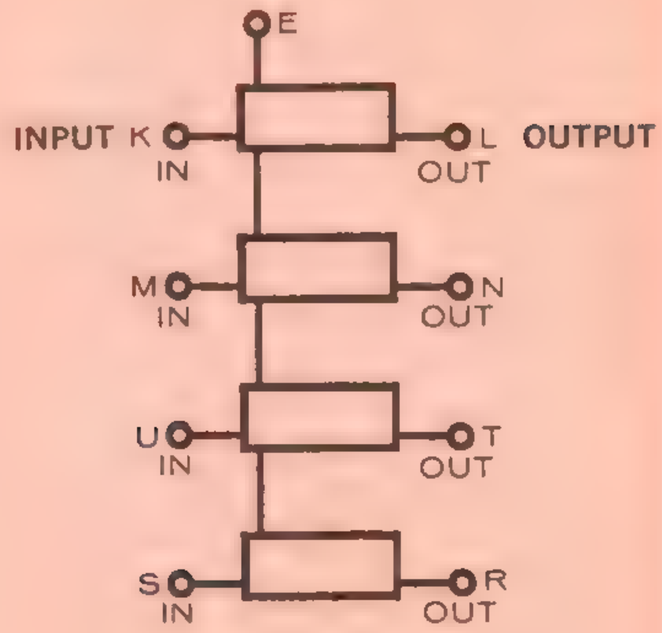
OUTPUT: The selected output is a positive voltage and the unselected outputs are ground. If the enabling signal is ground, all outputs will be ground. When an output is ground, the output transistor is capable of supplying 10 ma to its own load (12,000 ohms to pin Z) plus external circuitry. When the output is a positive voltage, the driving ability is determined by the voltage at pin Z. External load resistors may be included to increase driving capabilities provided that no more than 10 ma are required to go through any output transistor.

POWER: −15 volts/60 ma; +10 volts (A)/0 ma; +10 volts (B)/3 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1684
BUS DRIVER



The Type 1684 is a non-inverting bus driver used to provide levels for heavily loaded logic lines at speeds up to 5 megacycles. There are four identical circuits in the module. The input to each circuit is through a grounded inverter. The unloaded total transition time is ≤75 nanoseconds. Increasing the driving capabilities of each output from 5 to 20 units of Base Load is accomplished by connecting pin E through a 120-ohm, 2 watt resistor to −15 volts.

INPUT: Each input represents 1 unit of 5 megacycle Base Load.

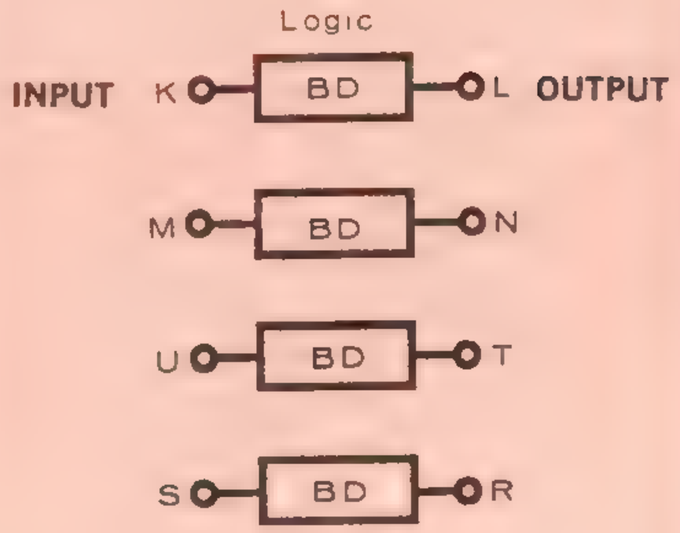
OUTPUT: Each unit is capable of driving 5 units of DC Base Load and an infinite amount of capacitance. Its output impedance is 22 ohms. With additional resistors each output is capable of driving 20 units of 5 megacycle Base Load at 5 megacycles, or 15 units of 500 kilocycle Base Load at 500 kilocycles, or 20 units of 500 kilocycle Base Load where speed is no problem.

POWER: −15 volts/84 ma; +10 volts (A)/1.6 ma; +10 volts (B)/1.6 ma. Optional 120-ohm, 2 watt-resistor to −15 volts from pin E/115 ma.

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1685
BUS DRIVER

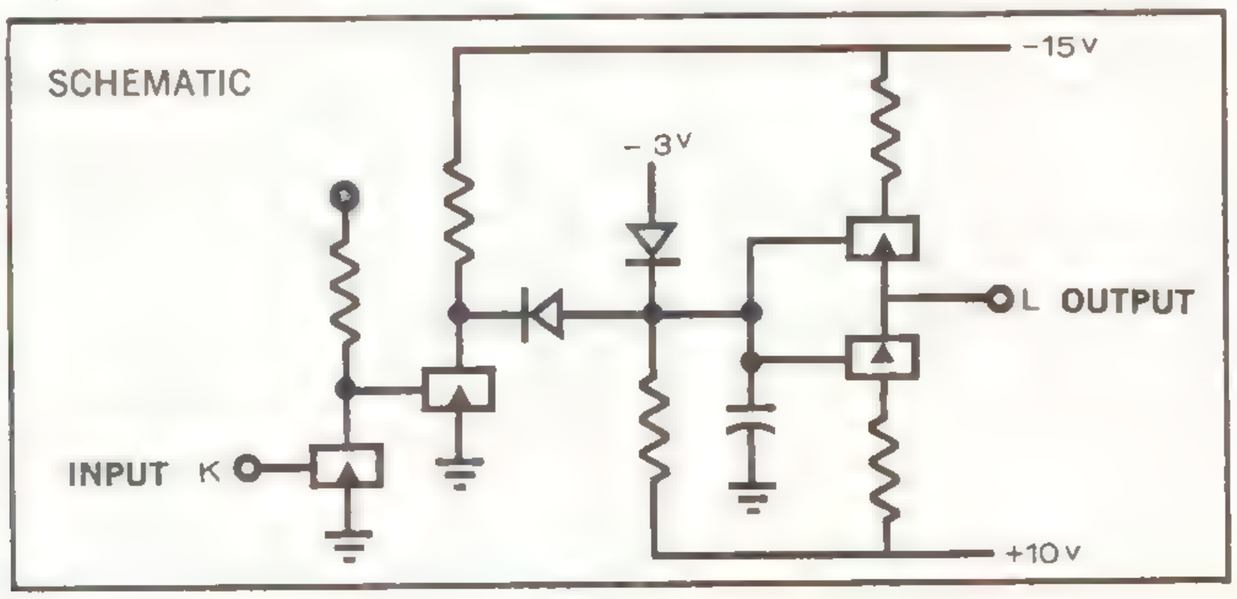


The Type 1685 contains four non-inverting bus drivers for use in driving heavily loaded output lines where fast rise and fall times would create severe ringing and large induced voltage transients. The rise and fall times of the output signal are approximately 1 microsecond. There are four identical circuits in the module with two cascaded inverters at each input. For more than 5000 pf output load, the maximum rise or fall time in microseconds is equal to the capacitance in pf divided by 5000.

INPUT: Each input represents ½ unit of 5 megacycle Base Load.

OUTPUT: Each output is capable of driving 15 units of 5 megacycle Base Load at 500 kilocycles, or 8 units of 500 kilocycle Base Load at 500 kilocycles, or 15 units of 500 kilocycles Base Load at lower frequencies. It can supply ±15 ma.

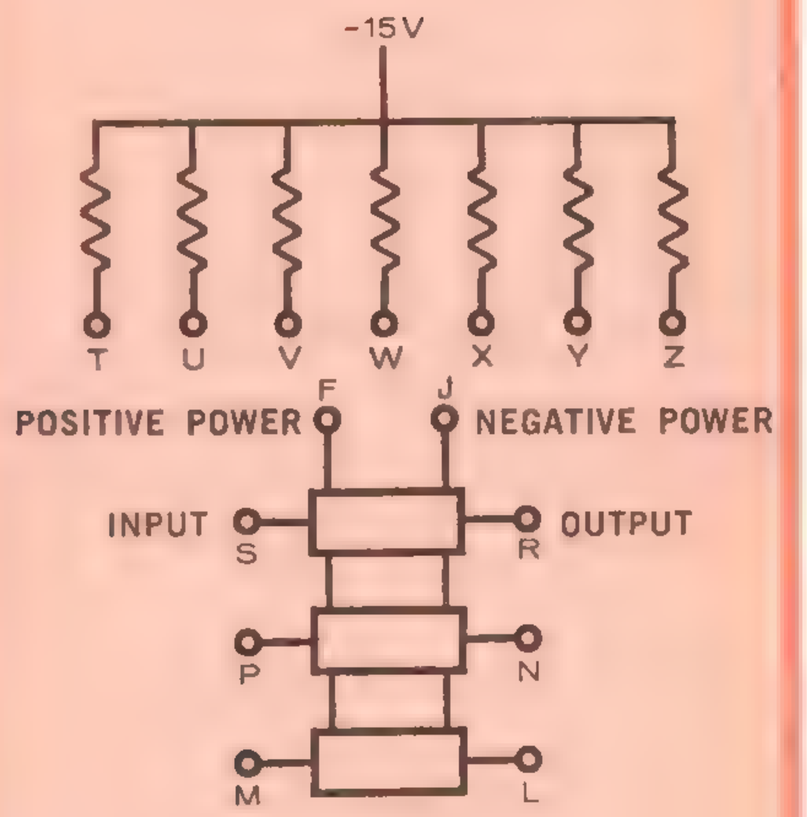
POWER: −15 volts/145 ma; +10 volts (A)/0.8 ma; +10 volts (B)/105 ma.



digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1687
LEVEL AMPLIFIER



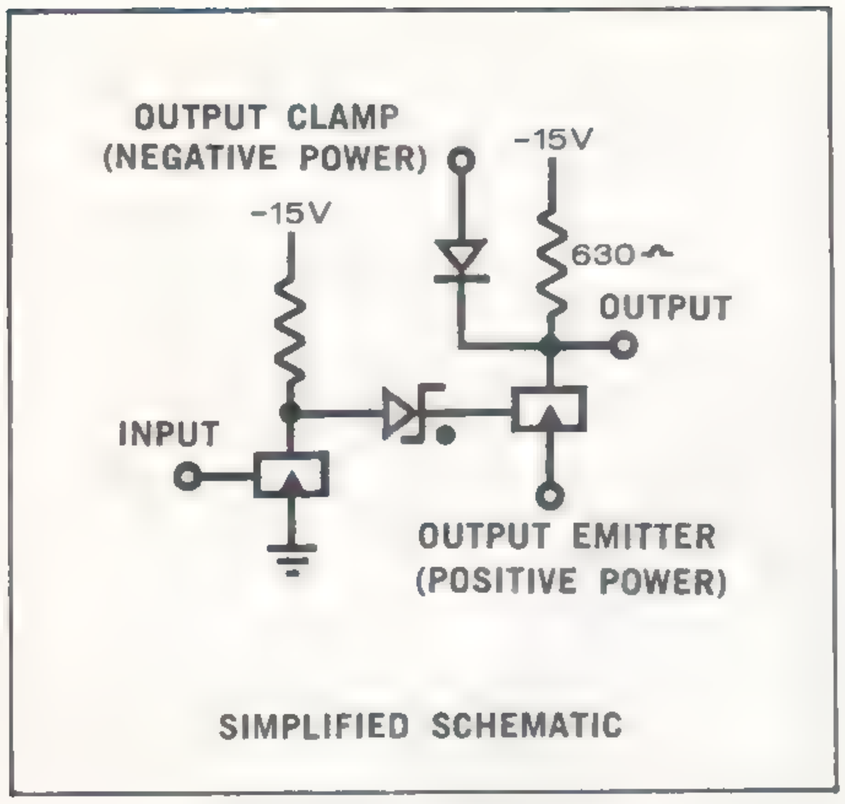
The Type 1687 contains three general-purpose level amplifiers whose upper level is determined by an external supply between 0 and +6.5 volts and whose lower level is determined by an external clamp voltage that may be as negative as −6.5 volts. Each input is through a 5 megacycle inverter which drives its output inverter through a zener diode. The output emitter power supply (pin F) may be in the range 0 to +6.5 volts. The clamped load power supply (pin J) must be more negative than the emitter power supply and may be as negative as −6.5 volts.

Seven 10,000-ohm resistors, returned to −15 volts, are included in the package, but are not part of the level circuitry. These may be used with DEC inverters to form exclusive OR circuits, if desired.

INPUT: The inputs should be DEC 5 megacycle Standard Levels of ground and −3 volts. Each input represents 1 unit of Base Load.

OUTPUT: The level amplifier can deliver up to 10 ma at its upper level of 0 to +6.5 volts. The current available at the lower level varies with the lower level used. At −6.5 volts, 10 ma is available. The current is determined by the load resistor which is returned to −15 volts. More current is available at a less negative lower level; for example, when the lower level is +2 volts, the current available is 20 ma. Total transition time is less than 70 nanoseconds.

POWER: −15 volts/150 ma; +10 volts (A)/0.4 ma; +10 volts (B)/5.4 ma; pin F at +6.5 volts/140 ma + external load current; pin J at −6.5 volts/40 ma charging current.

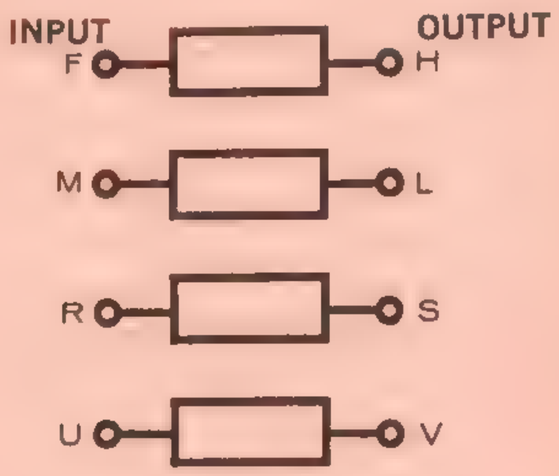


SIMPLIFIED SCHEMATIC

digital

1000 SERIES
SYSTEM MODULES
5 MEGACYCLES

1689
DEC TO 7090 CONVERTER



The Type 1689 contains 4 circuits that convert DEC signals to voltage mode IBM 7090 signals. A ground input signal will give an output of +8 volts and a −3 volt input will give an output of ground. Each circuit is able to drive a 93 ohm load with a total transition time of less than 0.20 microseconds. A simplified schematic of one of the circuits is shown in Figure 1. The input is a grounded-emitter inverter which drives, through a zener diode, an output inverter whose emitter is at +8.5 volts. The +8.5 volts is derived from the +10 volt supply by forward-biased silicon diodes.

INPUT: The input is a DEC level of ground or −3 volts. A ground input produces +8 volts out, and a −3 volt input produces ground out. Input load is one unit of base load.

OUTPUT: Each output is able to drive a 93 ohm load. The output total transition time is less than 0.20 microseconds. The upper level is +8 ±2 volts, and the lower level is determined by the internal 3000 ohm load in parallel with the external load.

POWER: +10 volts (A)/180 ma*; +10 volts (B)/180 ma*; −15 volts/60 ma.

*This is the +10 volt current for 100% duty factor driving 93 ohm loads. When the output voltages are ground these currents are reduced to 1 ma each.

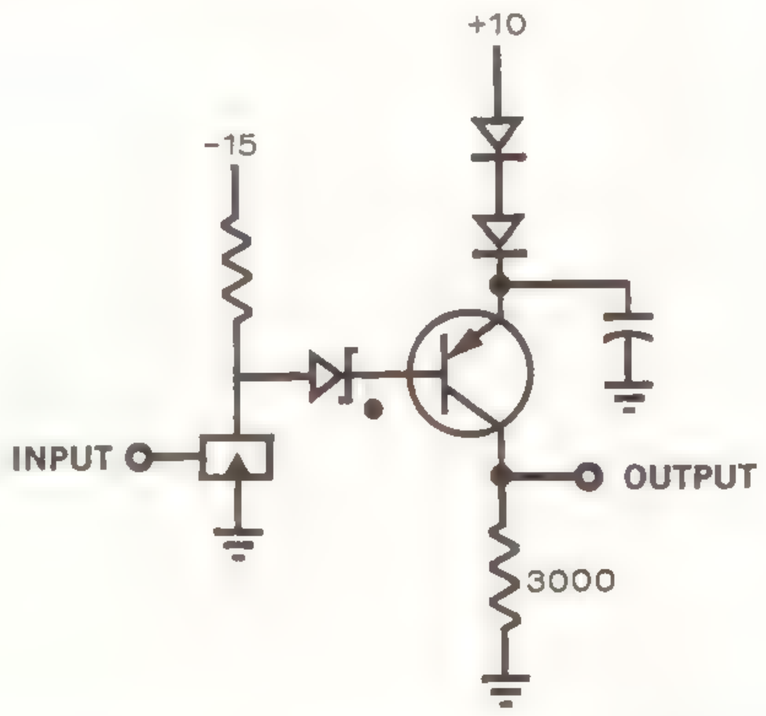
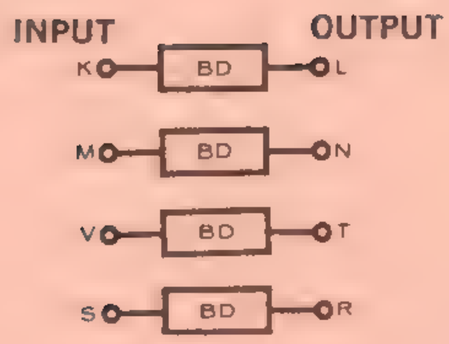


Figure 1

digital

1000 SERIES
SYSTEM MODULES

1690
BUS DRIVER



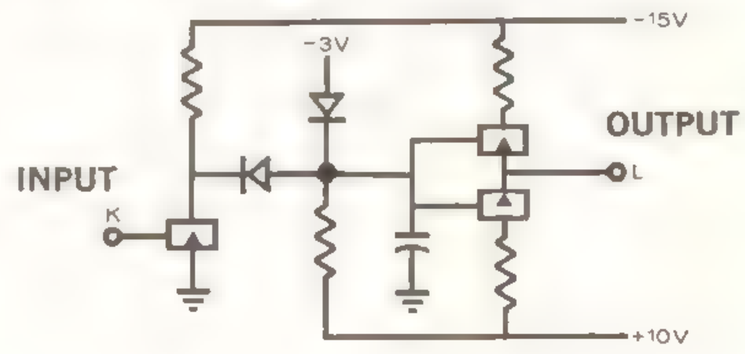
The Type 1690 contains four inverting bus drivers for use in driving heavily loaded output lines where fast rise and fall times would create severe ringing and large induced voltages. The delay is less than 120 nanoseconds and the rise and fall times of the output signal are approximately 1 microsecond. For more than 5000 pf output load, the maximum rise or fall time in microseconds, is equal to the capacitance in pf divided by 5000.

INPUT Each input represents ½ unit of 5 megacycle Base Load.

OUTPUT Each output is capable of driving 15 units of 5 megacycle Base Load at 500 kilocycles or 8 units of 500 kilocycle Base Load at 500 kilocycles or 15 units of 500 kilocycles Base Load at lower frequencies. It can supply a maximum current of ±15 ma.

POWER −15 volts/123 ma; +10 volts (A)/0.8 ma; +10 volts (B)/10.5 ma.

SCHEMATIC



Types 52 and 62 Current Drivers will withstand up to ±20 volts back voltage. By adding additional voltage in series with the power supply output, the back voltage tolerance can be increased to ±50 volts. This connection, shown in Figure 2, requires a +30 volt, 1 amp power supply and a −30 volt, 1 amp supply. Intermediate voltages will give correspondingly less back voltage tolerance. It is not necessary that the positive and negative back voltage tolerances be alike. The supplies only have to handle the average output current of the corresponding current drivers.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGES: Two 35 volt and two 10 volt supplies connected as shown in Figure 1.

MAXIMUM OUTPUT CURRENT: 4 amperes from each 35 volt supply; 0.35 amperes from each 10 volt supply

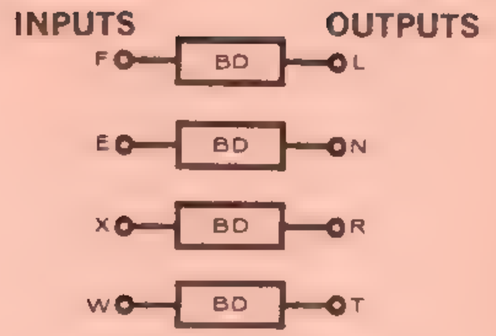
LINE AND LOAD REGULATION: For line voltage variation of 105 to 125 volts and load variations from 0 to maximum, the 35 volt supplies will be between 34 and 40 volts, and the 10 volt supplies will be between 9.5 and 10.6 volts.

P-P RIPPLE: 35 volt/1.5 volts maximum 10 volt/0.3 volts maximum

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝"
PANEL HEIGHT: 14"
DEPTH: 5"
FINISH: Chromicoat
POWER INPUT CONNECTION: Cinch Jones no. 141 Terminal Strip
POWER OUTPUT CONNECTION: DC: 8 Amphenol 26-4401-8P sockets.

1691
BUS DRIVER



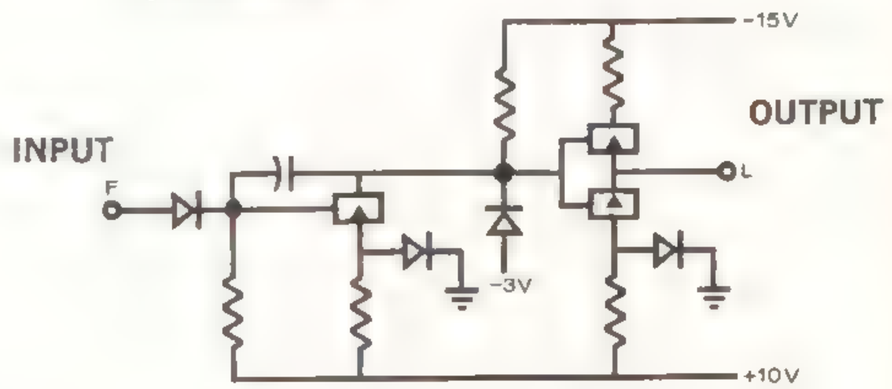
The four inverting drivers in the Type 1691 drive external equipment with logic levels of 0 and −10 volts. The delay is less than 600 nanoseconds and the rise and fall times are both approximately 1.5 microseconds. For more than 1500 pf output load, the maximum rise or fall time, in microseconds, is equal to the capacitance in pf divided by 1000.

INPUT DEC Standard Levels or their equivalent are required for input levels. Each input represents ⅛ unit of DC Emitter Load.

OUTPUT Ground input produces −10 volt output; −3 volt input produces 0 ±0.1 volts. Each output can supply ±10 ma.

POWER −15 volts/68 ma; +10 volts (A)/48 ma; +10 volts (B)/48 ma.

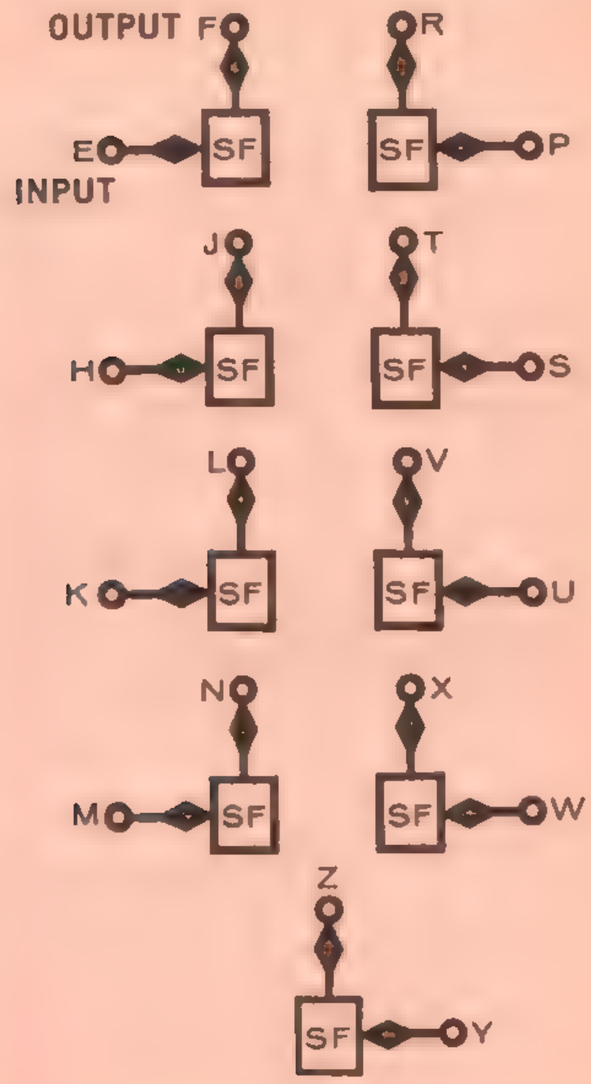
SCHEMATIC



digital

1000 SERIES
SYSTEM MODULES

1703
SWITCH FILTER



Nine switch filters eliminate contact bounce in converting contact closures to DEC Standard Logic Levels. An open input terminal produces a ground output, and a —15 volt input produces a —3 volt output. Output fall time varies from 2.5 to 5 milliseconds, and the output rise time is approximately twice the fall time.

INPUT: A 10 ma current flows through a contact when it connects an input to the —15 volt supply.

OUTPUT: Each output can drive 3 units of Base Load, ¼ unit of DC Emitter Load, any number of level inputs to capacitor-diode gates, and any number of Pulsed Emitter Loads providing no more than one is pulsed at a time.

POWER: —15 volts/90 ma; +10 volts (A)/27 ma.

digital

3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

SERIES CHARACTERISTICS

A basic selection of 3000 Series Modules for digital logic demonstrations

DEC 3000 Series Laboratory Modules are a coordinated set of solid state digital circuits operating at frequencies up to 500 kilocycles. They are packaged in sturdy aluminum cases, measuring 1¾ x 4½ x 7 inches with graphic front panels which illustrate the logical function of each module. All logical interconnections are made on the front panels with miniature stacking banana jack patch cords. Power connections are made automatically when the modules are inserted in the Type 901 Laboratory Module Mounting Panel.

This unique method of packaging and special built-in safety features make these high quality circuits ideal for test equipment and laboratory use. Logical signals are in the range of 0 to −3 volts, which permits logical experimentation without the risk of damage to the circuitry. By following simple, well-defined loading rules, the user can quickly and easily duplicate existing systems for test or instruction purposes or implement new and unusual systems designs. The modules may be assembled and reassembled in countless combinations to meet any type of test or design requirement.

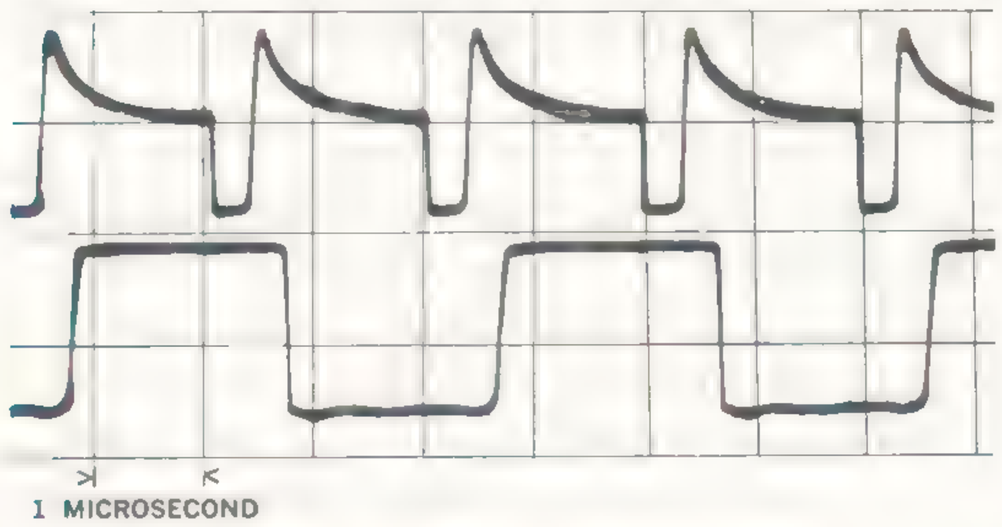
A particular advantage of all Digital Modules is their complete compatibility across speed lines. The 3000 Series units are mechanically and electrically compatible with the 100 and 5000 Series Laboratory Modules, and they are electrically compatible with the 1000, 4000 and 6000 Series System Modules. Thus systems capabilities may be readily extended to high frequencies, if desired, by incorporating suitable units from other lines.

The logic employed in all DEC Laboratory Modules, as described in the Introduction, uses static flip-flops with level logic and pulse sampling. The flip-flop outputs are buffered and include a built-in delay which permits the flip-flops to be pulse-sampled while being changed. Logic gating is peformed with DEC saturating transistor inverters and multiple input diode circuits internally connected to transistor inverters for signal amplification. This method of transistor gating and pulse sampling allows the construction of systems with a minimum of concern over wiring techniques and lead lengths.

The basic selection of logic modules in the 3000 Series includes a six-inverter package for logical gating, a negative diode NOR, a general purpose flip-flop with buffered level outputs and built-in carry pulse output, a delay one-shot with built-in pulse amplifier, both variable frequency and stable crystal clocks, a dual pulse amplifier package for logical gating and standardization of input pulses, and a pulse generator used to produce DEC Standard Pulses from external signals or by means of manual control.

DEC Standard Levels, used in all Digital Modules for performing logical gating functions, are 0 and −3 volts. DEC Standard Negative Pulses, used for sampling logic levels, are 2.5 volts in amplitude. The pulse width, which is commensurate with the speed line, is 0.4 microsecond in the 3000 Series. This pulse may be converted to the pulse widths of other frequency lines through the use of the pulse amplifier.

DEC STANDARD 0.4 MICROSECOND NEGATIVE PULSES



DEC TYPE 3201 FLIP-FLOP OUTPUT

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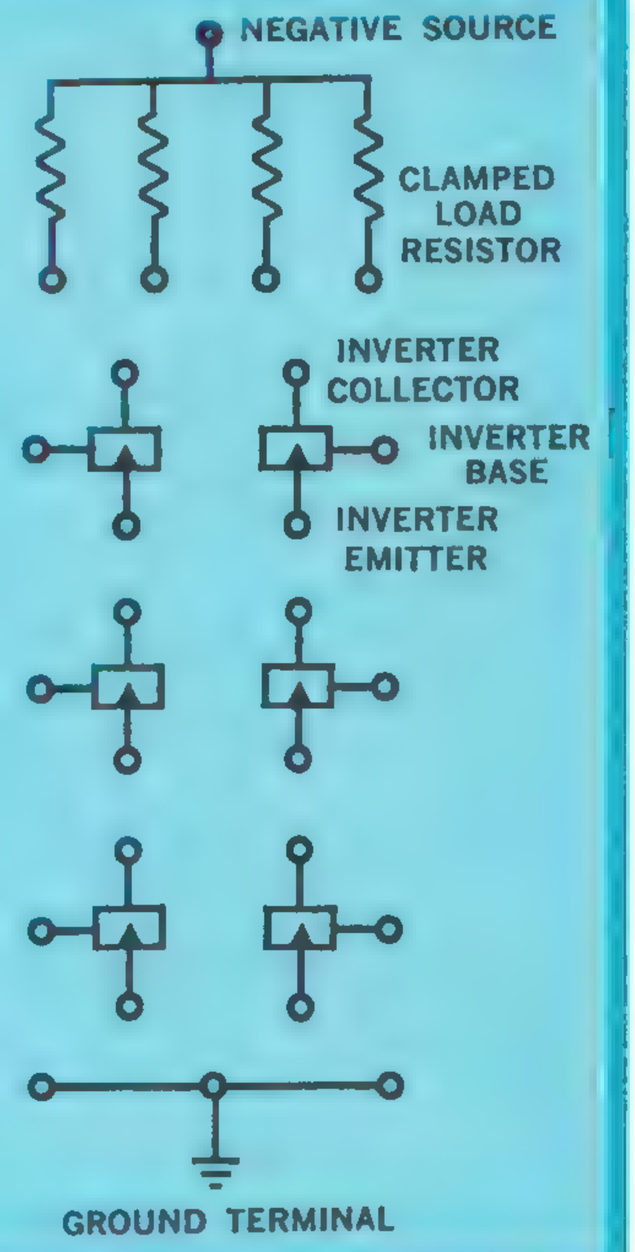
3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

3101
INVERTERS



Type 3101 contains six transistor inverters for use as pulse gates or level gates, and four load resistors clamped to −3 volts. Delay through an inverter is approximately 0.3 microseconds. Each inverter is analogous to a switch. If −3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base if brought to ground, the emitter-collector path is open.

INPUT: Base — DEC Standard 0.4 microsecond Negative Pulses when the inverter is used as a pulse gate at any frequency up to 500 kilocycles (1 unit of Pulse Load). DEC Standard Levels or equivalent when the inverter is used as a level gate (1 unit of Base Load). **Emitter** — The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 7 units of Base Load and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: −15 volts/40 ma; −3 volts/37 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

INVERTER USAGE

DEC Transistor Inverters serve two functions. When used as level gates, they are placed in series and parallel configurations to perform logic. When used as pulse gates, the inverter will sample the logic performed by the level gates and read the results into a flip-flop or other active element.

When used as a pulse gate, an inverter will drive one and only one pulsed unit. Inverters serving as level gates are usually considered as simple switches when designing logical networks, but because they are not ideal switches, there are certain limitations which have to be taken into account. The voltage drop across saturated inverters is not zero; it is closer to 0.1 volt. As a result, inverters cannot be stacked indefinitely. Three inverters is the maximum which can be put in series if the output is to drive another inverter, as in Figure 1.

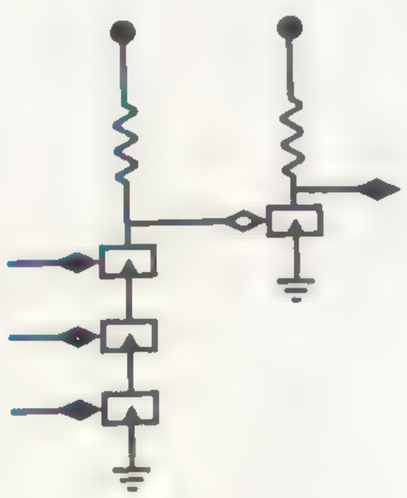


Figure 1

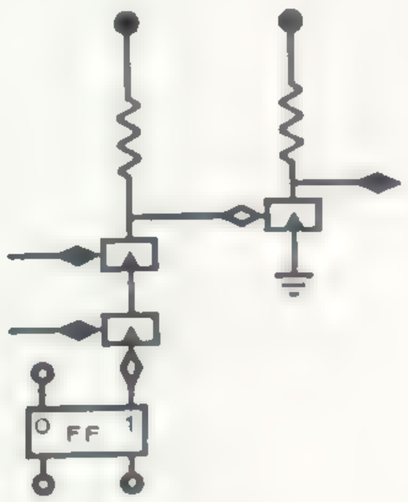


Figure 2

If inverters are in series with the output of a flip-flop, as in Figure 2, the flip-flop buffer inverter is considered to be one of the three allowed series transistors.

When the output of a series of inverters is driving the input of a pulse amplifier or delay unit or the set or clear input of a flip-flop, as in Figure 3, a fourth transistor serving as a pulse gate may be added in series. Only three may be used in series when driving the complement input of a flip-flop.

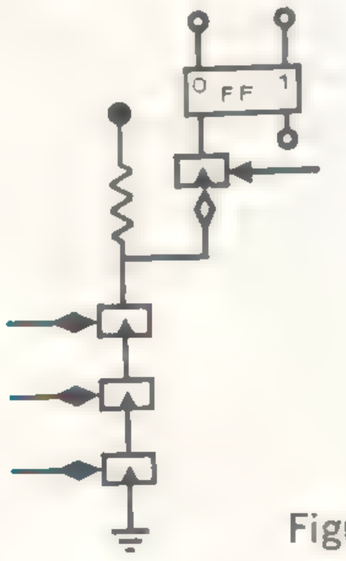


Figure 3

It is important to note that a clamped load resistor is tied to the emitter of each pulse transistor when it is being driven from an inverter or a network of inverters, as in Figure 3. (This clamped load resistor can be replaced by a 1N276 diode from the emitter of the pulse inverter to ground, connected so as to prevent this point from going positive.)

Because inverters are not really ideal switches, each collector of a series string of DC inverters supplying a pulse inverter will go somewhat negative during the pulse. This means that, if a series of inverters is supplying both pulse current and a DC signal, care must be taken because a signal will occur in the DC output during the pulse.

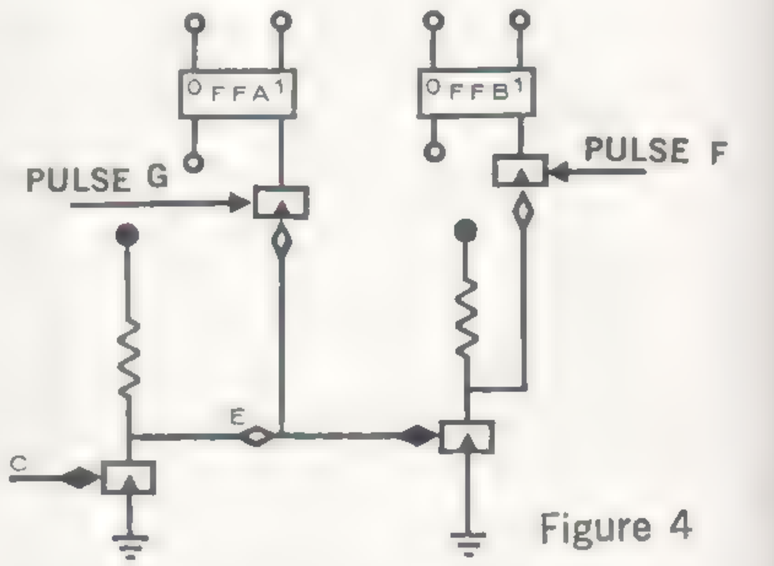


Figure 4

In Figure 4, if pulses F and G are simultaneous and the input C is negative, flip-flop A should be set by the pulse, but flip-flop B should not be set. However, during the pulse, collector E of the DC inverter feeding flip-flop A will go slightly negative. It will partly turn on the DC inverter feeding flip-flop B, and sometimes it will set flip-flop B as well as flip-flop A. This network will work only if the pulses F and G are not simultaneous.

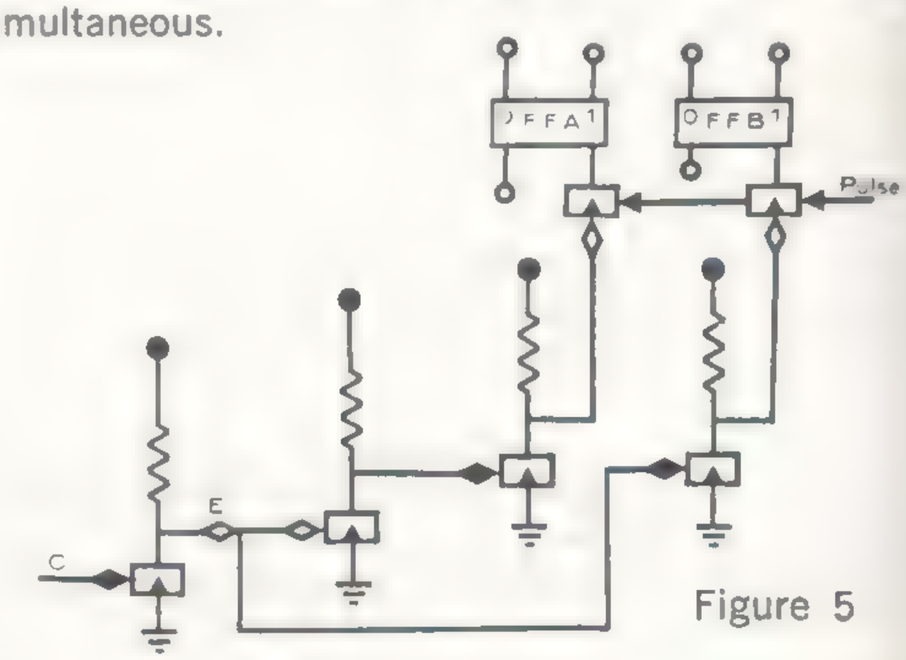
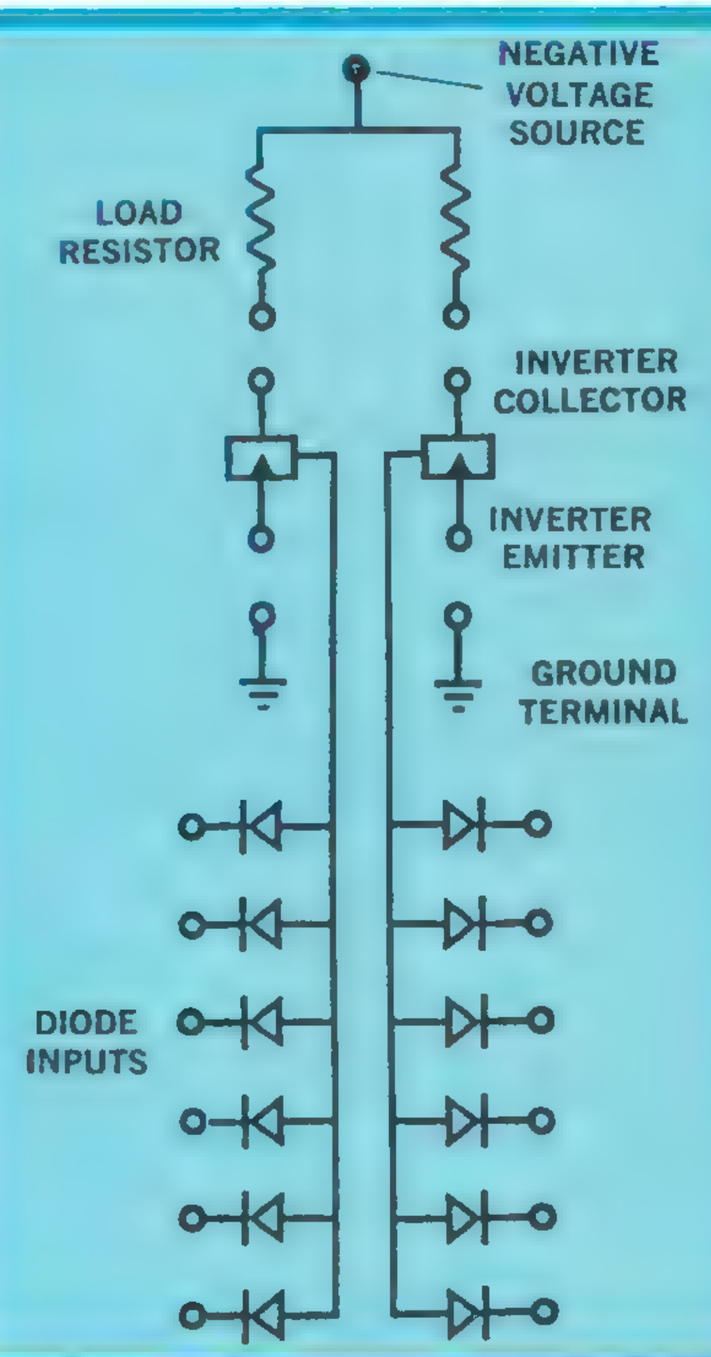


Figure 5

The network shown in Figure 5 will work whether or not the pulses are simultaneous. Two additional inverters have been added so that collector E will no longer be pulled negative by the pulse, since the pulse current will now come directly from ground instead of collector E. (If both outputs are feeding the same flip-flop, the network shown in Figure 4 can be used safely because the output of the A side will be much greater than that of the B side.)

3110
DIODE



The Type 3110 contains 2 six-input diode gates, each gate being connected to the base of a transistor inverter similar to a DEC Inverter Type 3101. The gates serve as OR circuits for negative level inputs and AND circuits for ground inputs. They may also be used to mix pulses. The emitter and collector of each transistor are available for external connections. Delay of a level through a diode and its inverter is approximately 0.4 microsecond.

INPUT: Diodes — DEC Standard Levels, DEC Standard 0.4 microsecond Negative Pulses or the equivalent will supply the input. When the diodes are used as a level gate, the load is 2 units of Base Load shared among those inputs which are at a negative voltage. When the diodes are used for pulse mixing, each input is 1 unit of Pulse Load. **Emitter** — DEC Standard Levels or equivalent drive the inverter emitter; the emitter may be grounded if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, the load on the emitter is 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, the load on the emitter is 1 unit of Pulsed Emitter Load.

OUTPUT: The inverter collector may be connected directly to a clamped load resistor, to the emitter of an inverter, or to the gated input terminal of a flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 7 units of Base Load and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

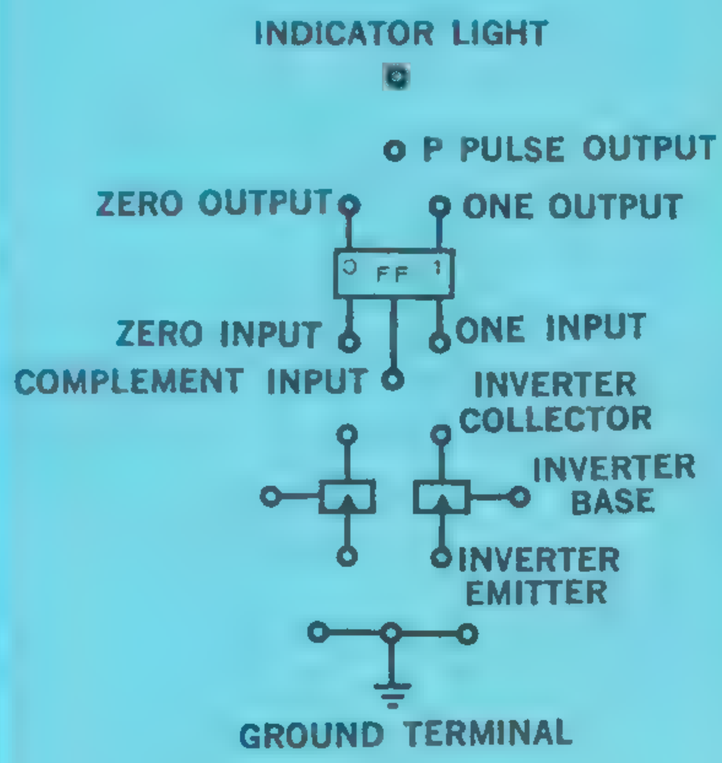
A collector with no clamped load can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: −15 volts/20 ma; −3 volts/37 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma.

digital

3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

3201
FLIP-FLOP



The Type 3201 is a static flip-flop with built-in output amplifiers, indicator light, source of counting Carry pulses (P Pulse), and Complement Set and Clear inputs. Two inverters are included for gating the flip-flop inputs. It has sufficient gating to be used as one bit of a shift register or binary counter. This flip-flop can also be used for all general type logical operations. The output terminals have a built-in delay so that the flip-flop can be sensed at the same time an input terminal is being pulsed. The output voltage swing is diode clamped at −3 volts, to provide a constant output voltage quite independent of loading.

INPUT: ZERO input, ONE input and Complement input each must come from the collector of a pulse gate. More than one pulse gate can be connected to the same terminal. The above signals can occur in any sequence, at any frequency, and at any time intervals which have a minimum of 2.0 microseconds between any two signals (maximum frequency is 500 kilocycles). The two inverters are similar to those included in the DEC Inverter Types 3101 and 4105.

OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving: (a) 14 units of Base Load; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. The output signals have built-in delays so they can be sensed reliably at the same time that the input is being pulsed. This is very useful in counter, shift register and adder applications. Each time the Complement terminal is pulsed, a DEC Standard 0.4 microsecond Negative Pulse, capable of driving 1 unit of Pulse Load, will occur on the P terminal. Delay from the time the input inverter is pulsed to the time the P Pulse occurs is approximately 0.05 microsecond.

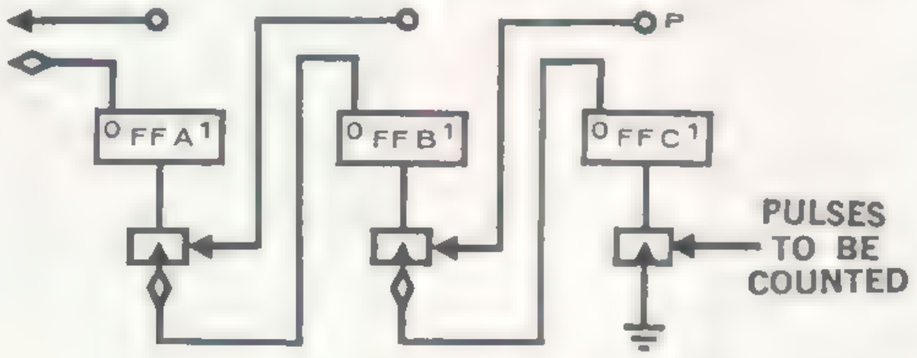
POWER: −15 volts/88 ma; −3 volts/21 ma; +10 volts (A)/1.1 ma; +10 volts (B)/1.0 ma.

BINARY COUNTERS

A typical counter arrangement using DEC Complementing Flip-flops is shown below. The pulses being counted enter on the right. They always complement flip-flop C and generate a standard pulse at P. This P Pulse complements flip-flop B when flip-flop C holds a ONE. When this P Pulse gets through the gate and actually complements B, it will generate a P Pulse out of B. The process is continued down the length of the counter. Only one inverter and one flip-flop are needed for each bit in the counter.

The series connection of P Pulses and gates forms a high-speed carry chain. The carry propagate time per digit (0.05 microsecond) is much less than the flip-flop's total transition time. To assure that flip-flop C will not be in the process of changing state while flip-flop B is receiving its carry pulse, a delay has been built into each flip-flop package. This insures that the ONE and ZERO output terminals will not change until after the carry pulse has been gated.

A down counter may be constructed by conditioning each pulse gate from the ONE terminal of the previous flip-flop (instead of the ZERO terminal).

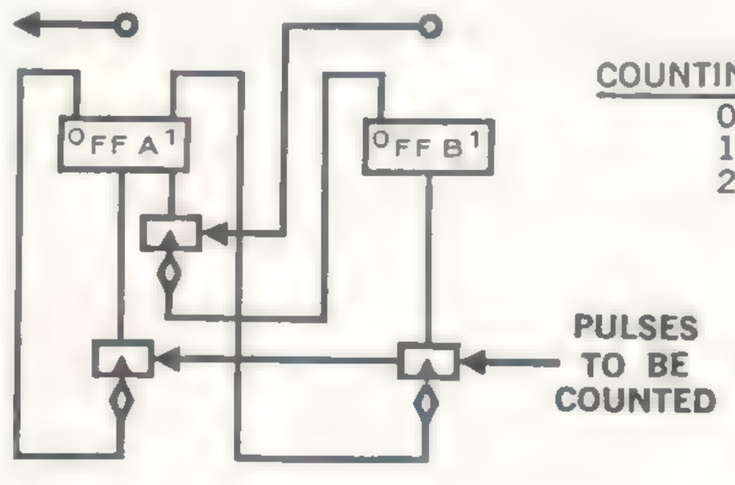


COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 1 — BINARY COUNTER

SPECIAL COUNTERS

The extra inverters included in the Type 3201 package allow additional flexibility for performing special counts, such as the "count of three" illustrated. The inverters are connected to assure that the counter will reset after the count of two. Since only one pulse in three will enter the complement input of flip-flop A, the P Pulse output of that flip-flop provides a convenient carry signal.



COUNTING SEQUENCE	
0	00
1	01
2	10

Figure 2 — COUNT OF THREE

SHIFT REGISTERS

Each Type 3201 package will make one stage of a shift register. DEC Shift Registers employ simultaneous jam transfer. As illustrated in Figure 3, the contents of all flip-flops are simultaneously moved to the right when the shift pulse occurs. Since the flip-flop outputs do not change until after the shift pulse has passed, no logical delays are needed between flip-flops.

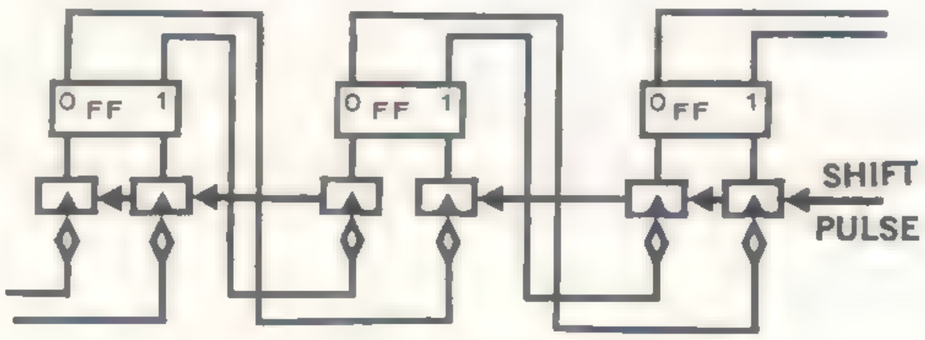


Figure 3 — SHIFT REGISTER

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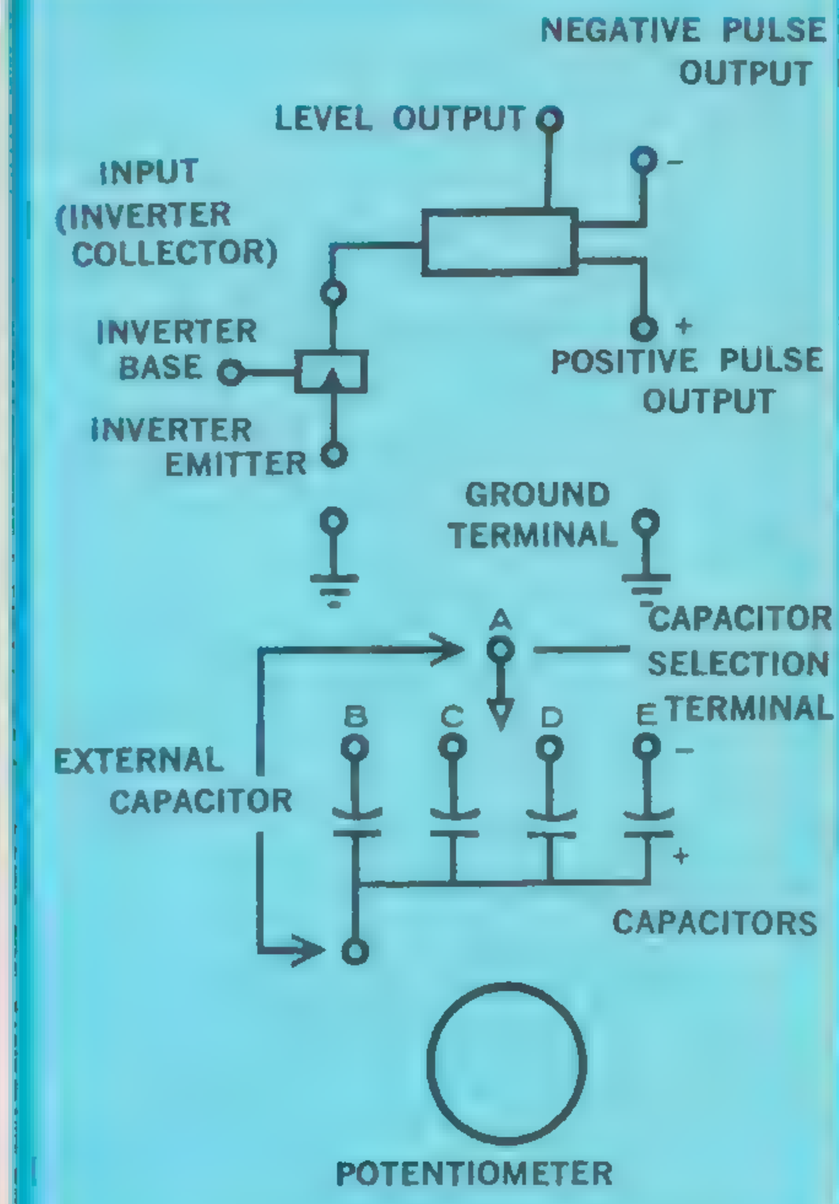
3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

3301
DELAY
(ONE SHOT)



The Type 3301 Delay unit is a mono-stable multivibrator. When the input terminal is grounded through an inverter, the level output terminal will switch from its normal ground level to −3 volts for a predetermined, but adjustable, period of time and then back to ground. A pulse transformer generates a DEC Standard 0.4 microsecond Pulse at the pulse output during the final transition. The pulse transformer has both positive and negative terminals so that either polarity pulse may be obtained. Typical output and input wave forms are shown in Figure 1.

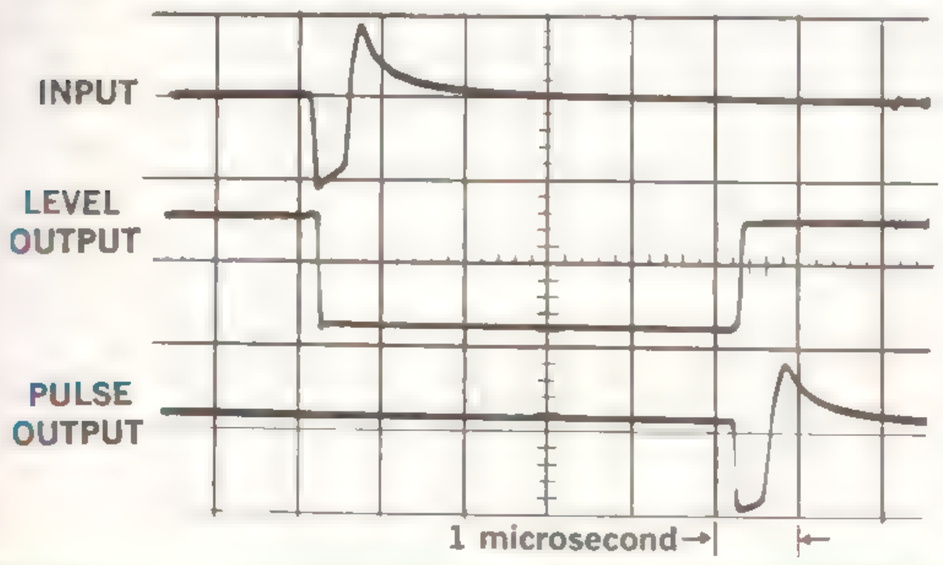


Figure 1 — OUTPUT AND INPUT WAVE FORMS

The delay duration is variable from 2.5 microseconds to 0.2 second. The five internal capacitors determine the coarse range. Capacitor A is internally connected to provide delays in the range of 2.5 to 25 microseconds. Connecting the capacitor selection terminal to capacitors B, C, D, or E increases the delay in approximate factors of 10, with capacitor E representing the maximum delay range available with an internal capacitor. By installing an additional external capacitor to the indicated terminals, the delay range may be further extended.

An internal potentiometer controlled by a knob on the front panel allows fine adjustment for the delays. Circuit recovery time is equal to 20% of the maximum delay available on the coarse range being used. A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.5%, peak to peak.

INPUT: The input to the delay is a DEC Standard 0.4 microsecond Negative Pulse on the base of a pulse gate, such as the one included in the delay module. The base of the built-in pulse gate represents 1 unit of Pulse Load; the emitter represents 1 unit of Pulsed

Emitter Load. If more logical inputs are desired, they can be provided by connecting other pulse gate collectors to the collector of the built-in pulse gate. Mixing of several pulses can also be accomplished by using half of a DEC Diode Type 3110 with DEC Standard 0.4 microsecond Negative Pulses applied to the diodes and the collector tied to the collector of the built-in pulse gate.

OUTPUT; Level — When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval. This level is capable of simultaneously driving: (a) 12 units of Base Load; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. **Pulse** — At the end of the delay interval, a DEC Standard 0.4 microsecond Pulse occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/74 ma; −3 volts/0 ma; +10 volts (A)/0.8 ma; +10 volts (B)/0 ma.

TYPICAL APPLICATIONS

WAVE FORM GENERATOR

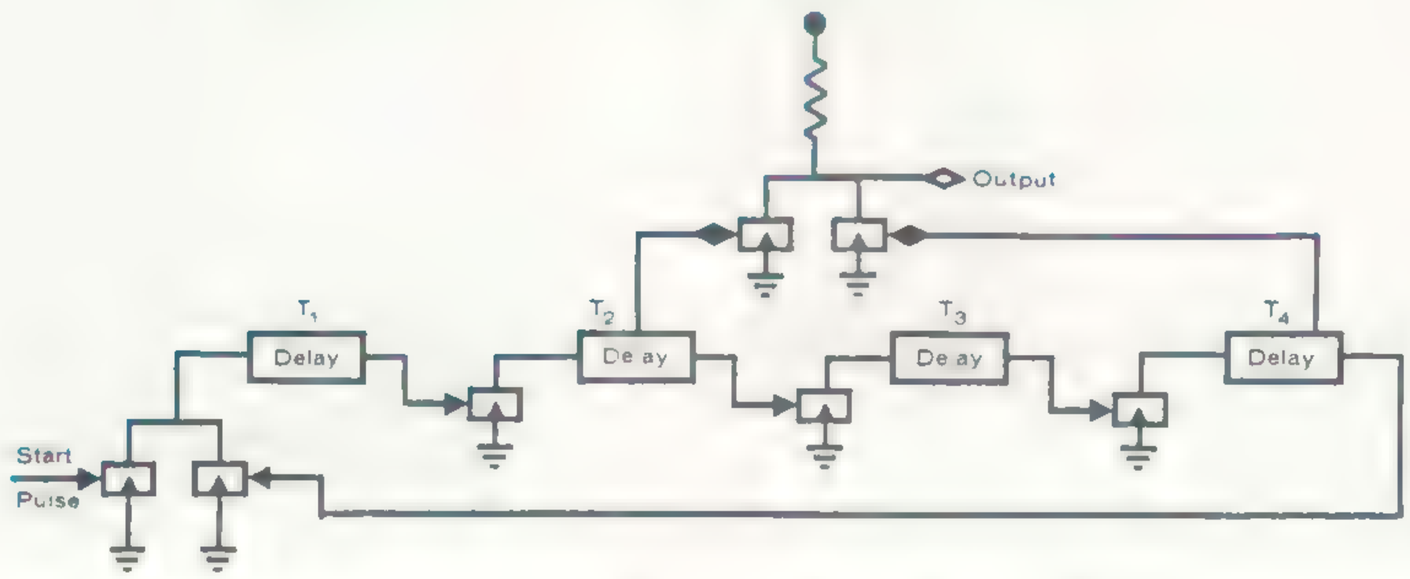


Figure 2 — WAVE FORM GENERATOR

Delay units are particularly useful in generating signals of arbitrary width. The network of delays in Figure 2 will produce the wave form in Figure 3.
The 1st and 3rd delays, not being connected to the output inverters, will produce no signal during their delay period. The 2nd and 4th, however, will produce a ground output for the duration of their respective delays. The wave form is periodic, since the pulse output from T_4 goes back to T_1. Due to delay recovery time, more than one delay unit is necessary to recycle the pulse.

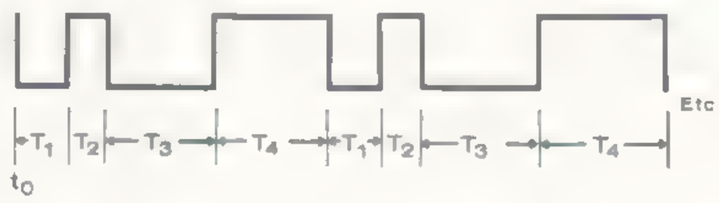


Figure 3 — OUTPUT WAVE FORM

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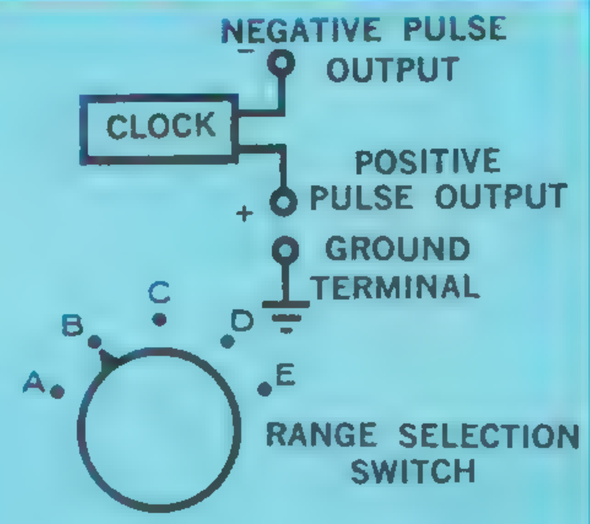
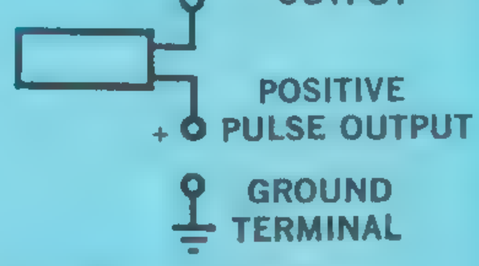
3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

3401-3407
CLOCKS



POTENTIOMETER (FINE CONTROL)

3401 VARIABLE CLOCK



3407 CRYSTAL CLOCK

The DEC Variable Clock Type 3401 produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies available. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the Type 3407 Crystal Clock, which contains a single-frequency crystal oscillator, may be used.

The Type 3401 variable frequency oscillator is variable from 5 cycles/second to 500 kilocycles/second. Five ranges provide magnitude control, and a built-in potentiometer permits fine adjustment. Lower frequencies may be obtained by adding a capacitor internally in parallel with the capacitor for the lowest scale.

The Type 3407 employs a series resonant crystal oscillator circuit and pulse shaping buffer amplifiers to provide very precise timing. The amplifiers produce DEC Standard 0.4 microsecond Pulses in the 5 kilocycle to 500 kilocycle range. The clock frequency, specified by the customer, is stamped on the front panel.

OUTPUT: The output is a DEC Standard 0.4 microsecond Pulse which occurs at the preselected frequency. The pulse may be made positive by grounding the negative output terminals; it may be made negative by grounding the positive output terminal. The signal can drive 8 units of Pulse Load. **Crystal Clock:** The stability of the crystal clock's output frequency is 0.01% between −20 and +55°C. **Variable Clock:** A 20% change in the power supply voltage on the Type 3401 Clock will change the prf less than 1% and its pulse-to-pulse jitter is less than 0.2%.

POWER: Type 3401: −15 volts/47 ma; −3 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. **Type 3407:** −15 volts/81 ma; −3 volts/0 ma; +10 volts (A)/5 ma; +10 volts (B)/4.5 ma.

TIMERS

Either the Type 3401 or 3407 could be used as part of the timer circuit shown in Figure 1. The start of an event triggers the pulse generator which grounds the ONE input of flip-flop E through an inverter. This brings the ZERO output of flip-flop E to a ground level which permits the next clock pulse to set flip-flop D. All following clock pulses will be gated into the counter. When a stop pulse arrives, the same procedure is used in stopping the counter.

The purpose of flip-flops D and E is to change the randomly occurring start, stop pulses into a synchronous level for gating the counter. The input pulses are converted to asynchronous levels by flip-flop E. Flip-flop D converts these asynchronous levels into synchronous levels. This assures that a split or partial pulse will never enter the counter; such a pulse could propagate only part of the way down the carry chain and result in an erroneous number.

The timer circuits such as shown in Figure 1 are useful in counting the delay between the occurrence of two events. A variation of the timer circuit is to replace the individual start, stop inputs with a single input going to the complement terminal of flip-flop E. This would allow the measurement of the time between the occurrence of two events on the same line.

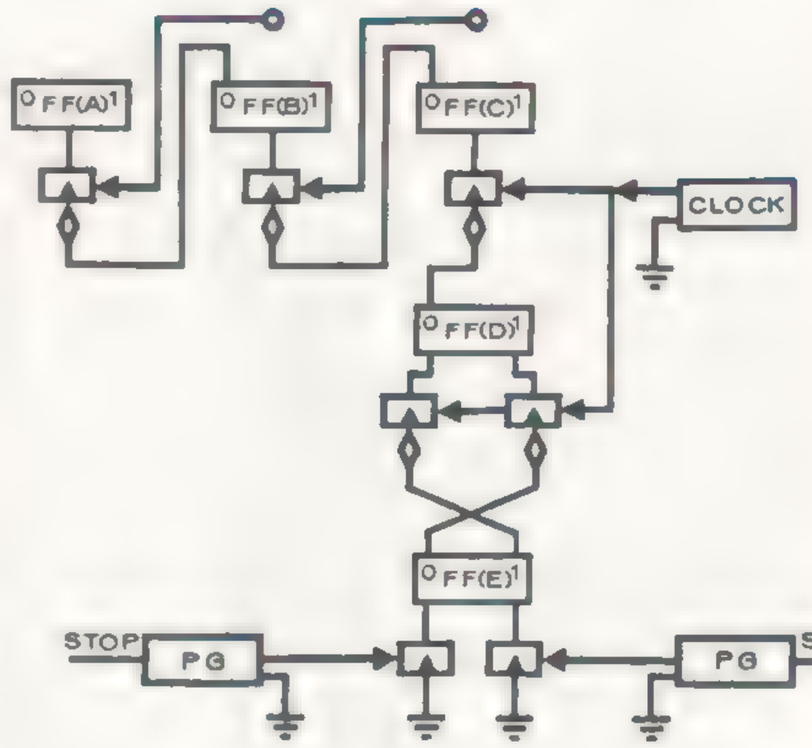
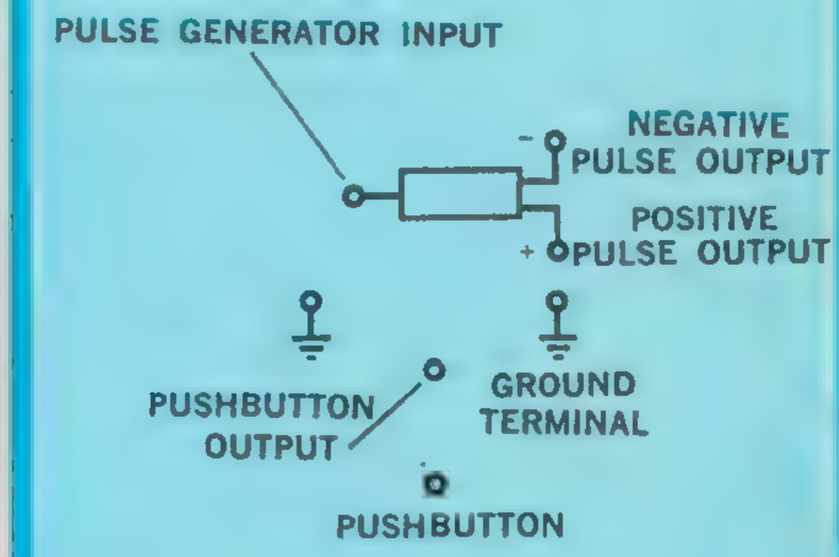


Figure 1 — Timer

3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

3410
PULSE GENERATOR



The Type 3410 converts external signals to DEC Standard Pulses. A Schmitt circuit produces a DEC Standard 0.4 microsecond Pulse at the output every time the input voltage goes more negative than −2.5 volts after having been more positive than −1.0 volts. This unit also contains a push button and an integrating circuit, the output of which may be connected to the pulse generator input.

INPUT: The input is a DC connection, thereby eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. The input signal should stay between +10 volts and −10 volts. The input can come from an external source or from the push button via the integrating circuit.

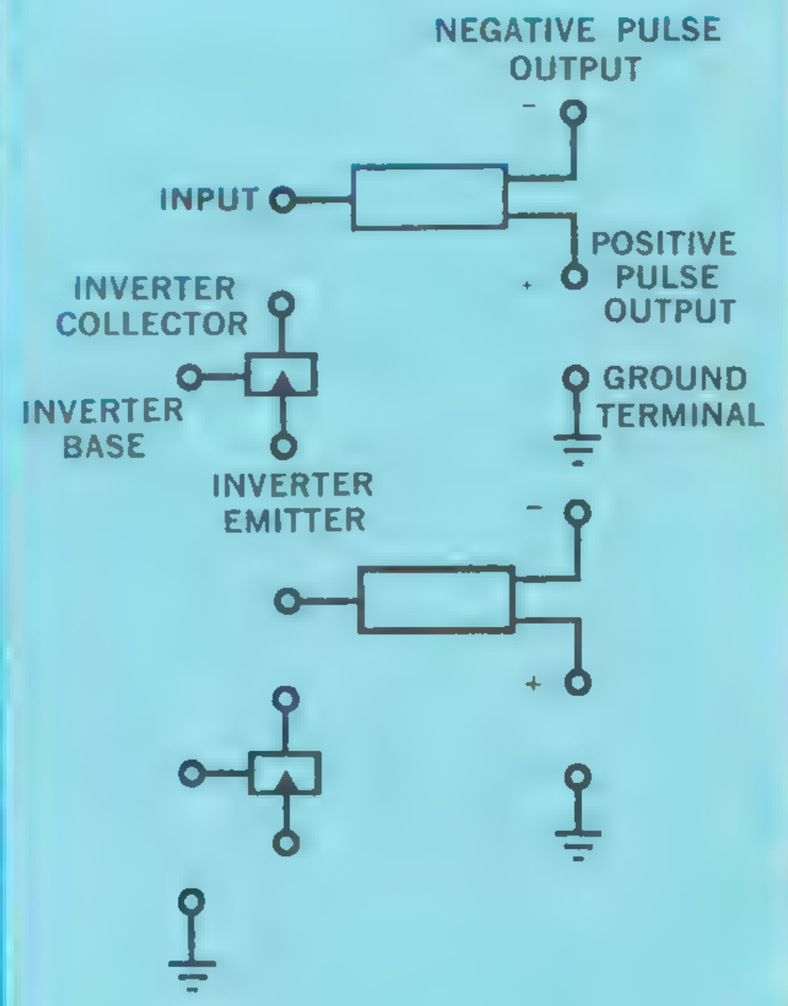
OUTPUT: The output is a DEC Standard 0.4 microsecond Pulse. The pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. The maximum prf is 500 kilocycles. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/34 ma; −3 volts/0 ma; +10 volts (A)/5.4 ma; +10 volts (B)/5.3 ma.

digital

3000 SERIES
LABORATORY MODULES
500 KILOCYCLES

3602
PULSE AMPLIFIER



The Type 3602 contains two pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Two standard inverters are included for gating the input. The inverters are similar to those in the DEC Inverter Type 3101. Delay through the pulse amplifier is approximately 0.05 microseconds. Input pulses may occur at any frequency up to 500 kilocycles. The DEC Diode Type 3110 may be used in conjunction with the pulse amplifier for conveniently mixing pulses from several sources.

INPUT: The input must come from the collector of one or more pulse gates. The signal on the base of the pulse gate is normally a DEC Standard 0.4 microsecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 0.2 microsecond and width greater than 0.3 microsecond may be used. Input pulses of less than −0.5 volts will not generate an output pulse. Several remote pulse gate collectors may be connected together to mix pulse sources.

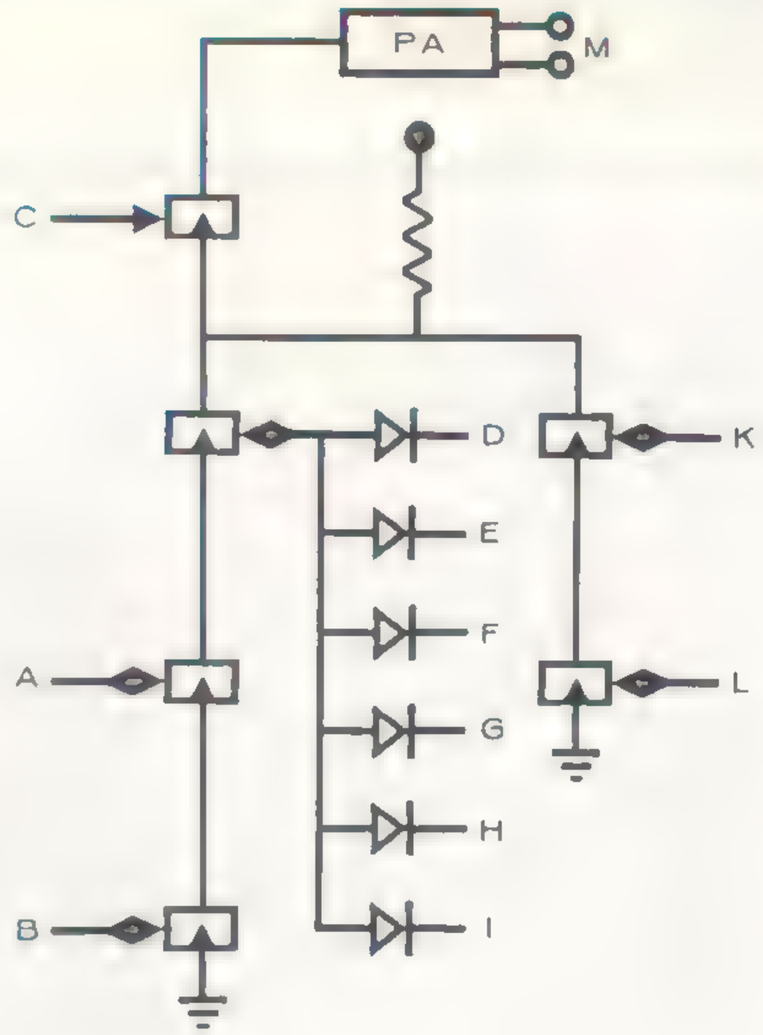
A DEC 70 nanosecond Negative Pulse may be used as an input, provided high speed pulse gates such as those in Types 103 or 1105 are used as the input and feedback pulse gates, and feedback loop is used as shown in Figure 2 of the applications section.

OUTPUT: The output is a DEC Standard 2.5 volt 0.4 microsecond Pulse which occurs at the output every time the input signal meets the input requirement. The pulse will be negative if the positive output is grounded; it will be positive if the negative output is grounded. Each output is capable of driving 16 units of Pulse Load.

POWER: −15 volts/87 ma; −3 volts/0 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma.

LOGICAL GATING

When a large amount of gating must be performed in several places, it is often economical to perform this gating at the input of a pulse amplifier. The output pulse may then go directly to flip-flops and other pulsed units with the same results as if the gating had been performed at each unit being pulsed. Figure 1 illustrates a typical gated pulse amplifier.



$$M = C[A \cdot B(D + E + F + G + H + I) + K \cdot L]$$

Figure 1
PULSE AMPLIFIER GATING

PULSE STANDARDIZATION

DEC Pulse Amplifiers are also useful in providing compatibility between the different series of DEC Modules. Since the modules are designed with compatibility in mind, the only differences between frequency lines are in the timing characteristics. In particular, pulses in the 10 megacycle line have a duration of 40 nanoseconds; in the 5 megacycle line, 70 nanoseconds; and in the 500 kilocycle line, 400 nanoseconds (0.4 microseconds).

To produce an 0.4 microsecond pulse from a 70 nanosecond pulse, a pulse amplifier with feedback is used. The output is a full duration 0.4 microsecond pulse with slightly less than the usual driving ability. This method, as illustrated in Figure 2, uses a Type 3602 Pulse Amplifier and two high speed inverters.

For more information on mixed systems, see "Integrating Different Series of DEC Modules".

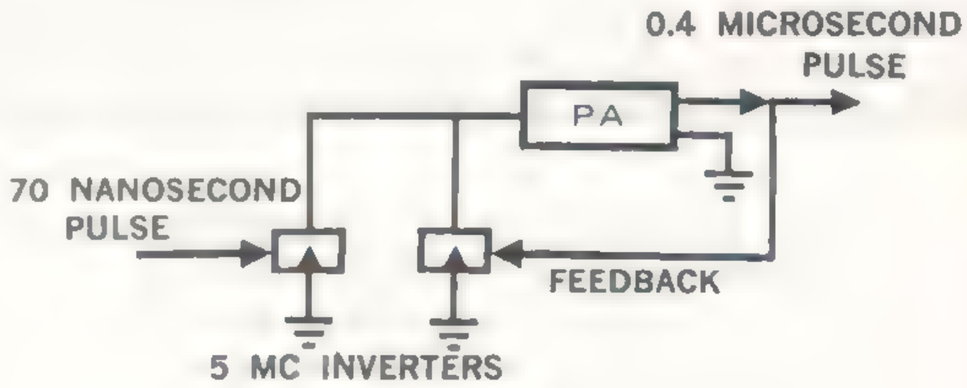


Figure 2
INCREASING PULSE DURATION

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

SERIES CHARACTERISTICS

System Modules may be removed from the mounting panel without disrupting the logical wiring

DEC 4000 Series System Modules are a coordinated set of solid state digital circuits operating at frequencies up to 500 kilocycles. They are mounted on protective aluminum frames measuring ½ x 4½ x 7 inches overall. All logic and power connections are through 22-pin Amphenol plugs electrically connected to the circuit boards by flexible wires to minimize strain. Plug-in mounting panels for System Modules are available in various widths, capacities and wiring options.

System Modules offer a unique combination of advantages for the design and construction of all types of digital systems. They are built for long, dependable service, whether used interchangeably in different applications or installed in permanent systems. In addition, they are available in a wide choice of circuits to meet various systems requirements.

General purpose circuits permit systems to be implemented with a minimum number of different types of modules. Special purpose units provide economy

in the construction of large-scale systems. Input-output units enable DEC circuits to accept a variety of different input signals, such as analog voltages, and to drive many types of special output equipment, such as electro-mechanical devices.

Since all Digital Modules are compatible across speed lines, it is possible to extend system capabilities or to achieve important savings in systems construction by incorporating units from other lines. The 4000 Series units are electrically and mechanically compatible with 1000 and 6000 Series System Modules, and they are electrically compatible with 100, 3000 and 5000 Series Laboratory Modules.

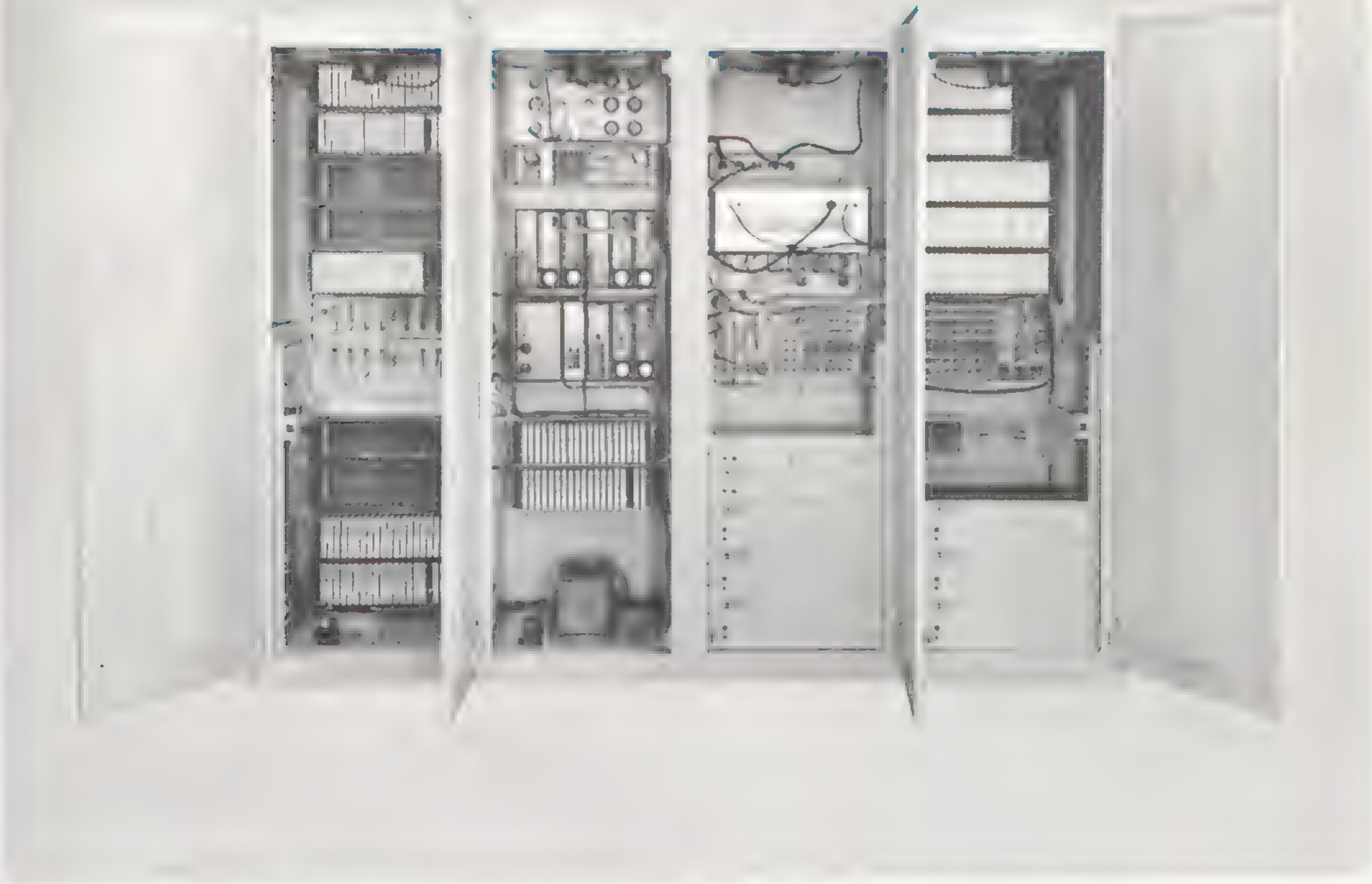
Two types of flip-flops are available in the 4000 Series, each employing a different method of logic. Level logic with pulse sampling, the method employed in most Digital Modules, is implemented with buffered flip-flops Types 4201, 4202 and 4209. Differentiating level logic, which may be used where space is limited and high driving capabilities are not required, is performed with unbuffered quadrupled flip-flops Types 4213, 4214, 4215, 4216, and 4218. The 4000 Series pulse amplifiers, pulse generators, clocks, delay units, and special input-output devices are used with both forms of logic.

The buffered flip-flops have built-in delays and high output driving capabilities. The delay allows the level outputs to be pulse-sampled at the same time the flip-flop inputs are being triggered. The high driving capabilities permit emitter gating, which is performed with saturating transistor inverters and diode gates internally connected to inverters. This method of transistor gating and pulse sampling allows the construction of systems with a minimum concern over wiring techniques and lead lengths. Isolation of the output circuit from the basic flip-flop assures that overloading of the circuit will not accidentally set or clear the flip-flop.

The economical unbuffered flip-flops utilize a simple two-transistor circuit which permits packing densities of four flip-flops per card. Since there is no isolation between the basic circuit and the output, the flip-flops may be set and reset through their outputs. This feature is very useful in many applications, but it imposes much stricter loading and wiring requirements than are necessary with the buffered flip-flops.

The Type 4215 is the most adaptable of the unbuffered quadruple flip-flops. Special built-in gates enable its use with no additional gating as a special counter for counts of 2, 3, 4, 5, 6, 8, 9, 10, 12, and 16. When used with the negative capacitor-diode gates Types 4125, 4127, and 4129, this unit will serve all general purpose flip-flop applications.

The quadruple flip-flop Type 4214 may be used with the positive capacitor-diode gates Types 4126 and 4128 for all set, reset flip-flop applications. Other unbuffered quadruple flip-flops are special purpose units designed for buffer or shift register applications.



Many large-scale systems utilize high reliability DEC System Modules

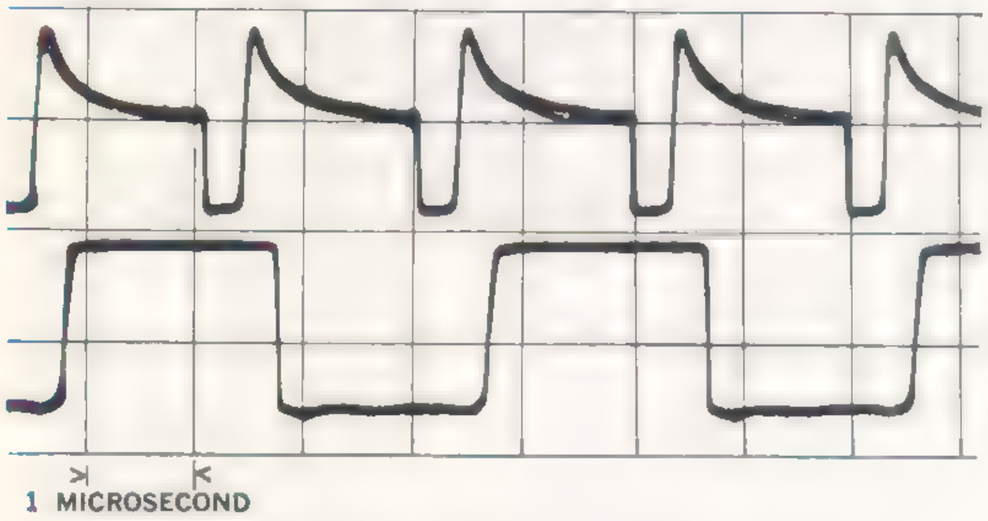
Capacitor-diode gate circuits are used for the differentiation of changing levels and for gating. The "set-up time" requirements on the conditioning level input serves as a logical delay. This permits the simultaneous changing and sampling of unbuffered flip-flops. When diode NORs are used as multiple input gates, their outputs may be sampled with capacitor-diode gates when the delay is needed.

In addition to the buffered flip-flops, the basic selection of general purpose logic modules in the 4000 Series includes inverter packages for logical gating, negative and positive diode NORs, a delay one-shot with built-in pulse amplifier, an integrating one-shot with no recovery time, a variable frequency clock, and two triple pulse amplifier packages for logical gating and standardization of input pulses.

Special purpose units available in the 4000 Series, other than the unbuffered flip-flops, include a variety of diode gates and special gates (such as the binary-to-octal decoders), signal conversion devices, special amplifiers, drivers, single-ended bridges, and a crystal clock.

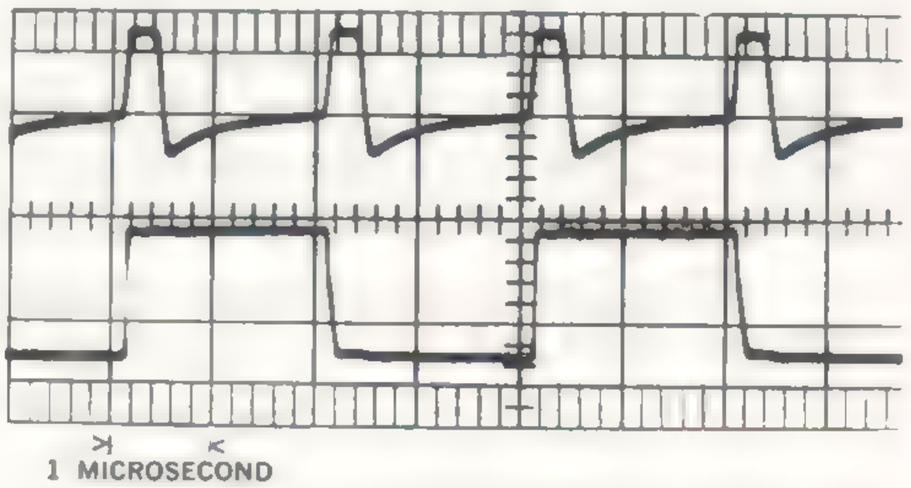
DEC Standard Levels, used in Digital Modules for performing logical gating functions, are 0 and −3 volts. DEC Standard Negative Pulses, used for sampling logic levels, are 2.5 volts in amplitude. The pulse width, which is commensurate with the speed line, is 0.4 microseconds in the 4000 Series. Other pulses may be converted to 4000 Series pulses with the Type 4604 Amplifier. External signals may be used as DEC Pulses if they meet the requirements outlined for the Type 4604 Pulse Amplifier or the 4610 Pulse Generator.

DEC STANDARD 0.4 MICROSECOND NEGATIVE PULSES



DEC TYPE 4201 FLIP-FLOP OUTPUT

DEC STANDARD 0.4 MICROSECOND POSITIVE PULSES

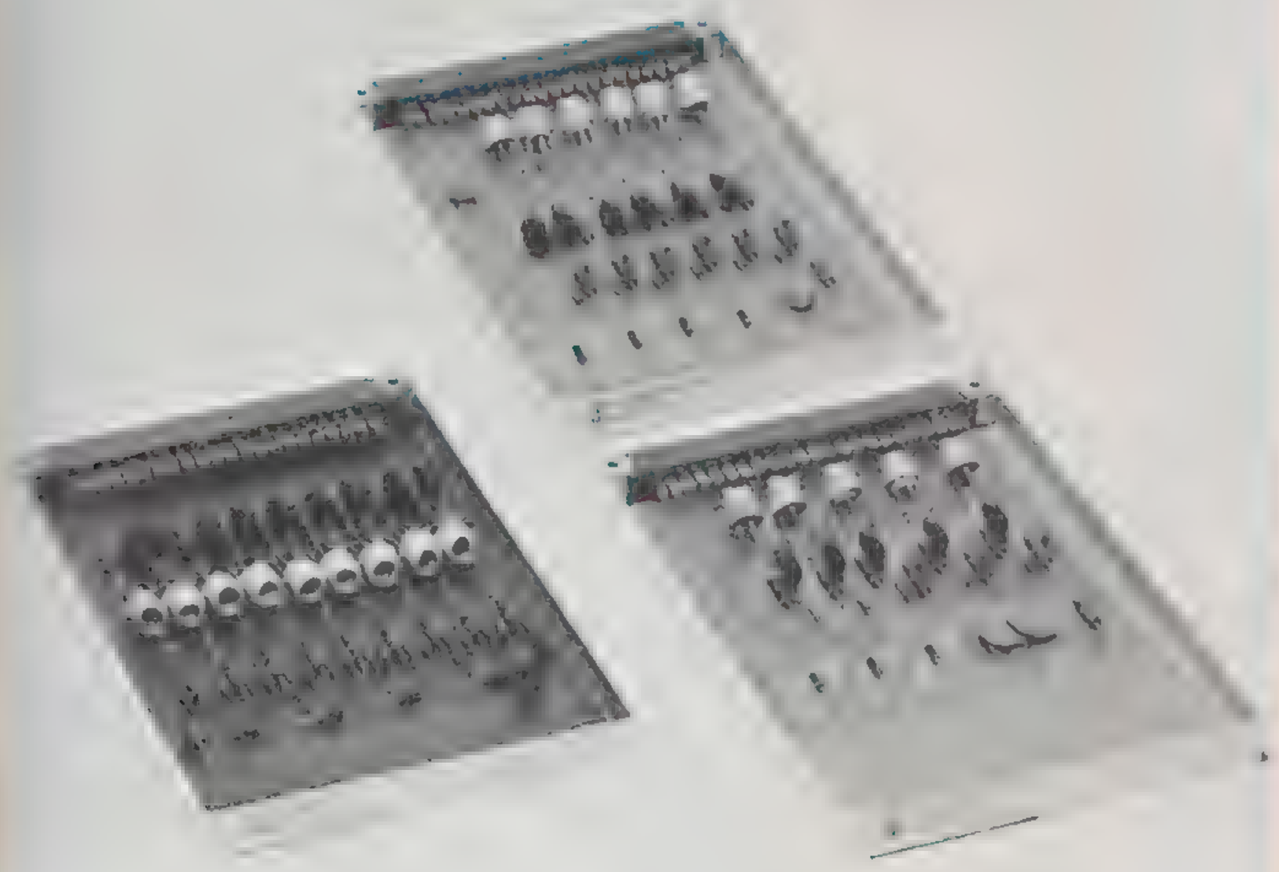


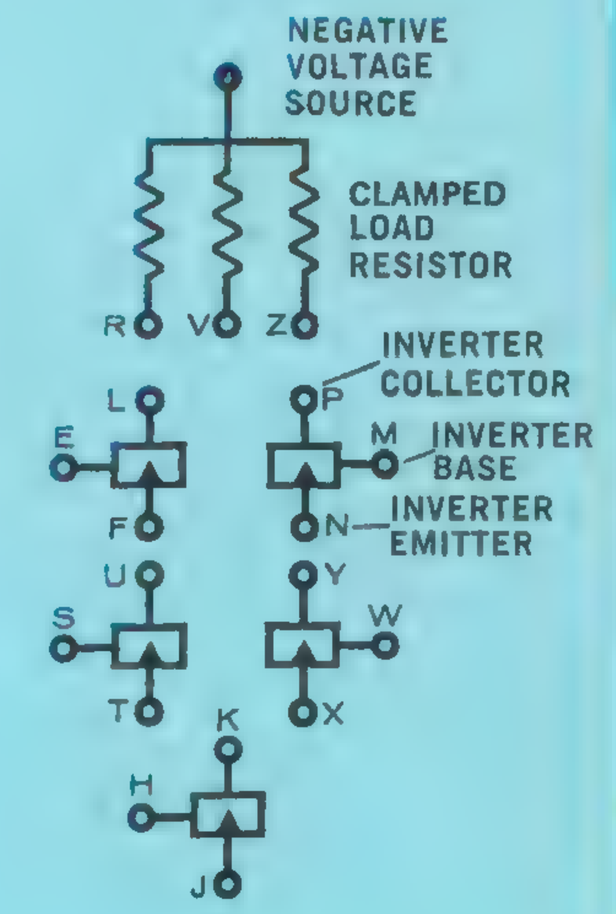
DEC TYPE 4215 FLIP-FLOP OUTPUT

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4102-4105-4106
INVERTERS





4105 INVERTER

The Types 4102, 4105, and 4106 contain transistor inverters for use as pulse or level gates. Each inverter is analogous to a switch. If —3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base is brought to ground, the emitter-collector path is open. Delay through each inverter is approximately 0.3 microsecond.

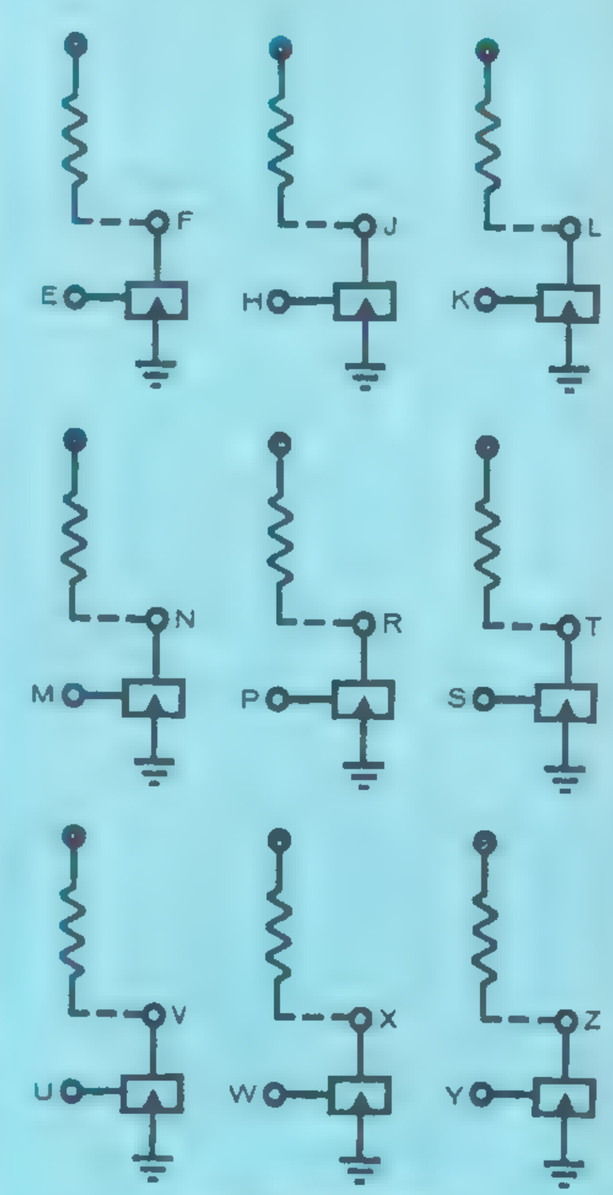
The Type 4102 contains nine inverters with grounded emitters. Each inverter has a clamped load resistor which may be internally jumpered to the collector, if desired. The Type 4105 contains five inverters and three clamped load resistors. The Type 4106 contains six inverters, each with a clamped load resistor which may be internally jumpered to the inverter collector, if desired.

INPUT: Base — Inputs are DEC Standard 0.4 microsecond Negative Pulses when the inverter is used as a pulse gate at any frequency up to 500 kilocycles (1 unit of Pulse Load). Inputs are DEC Standard Levels or equivalent when the inverter is used as a level gate (1 unit of Base Load). **Emitter** — The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

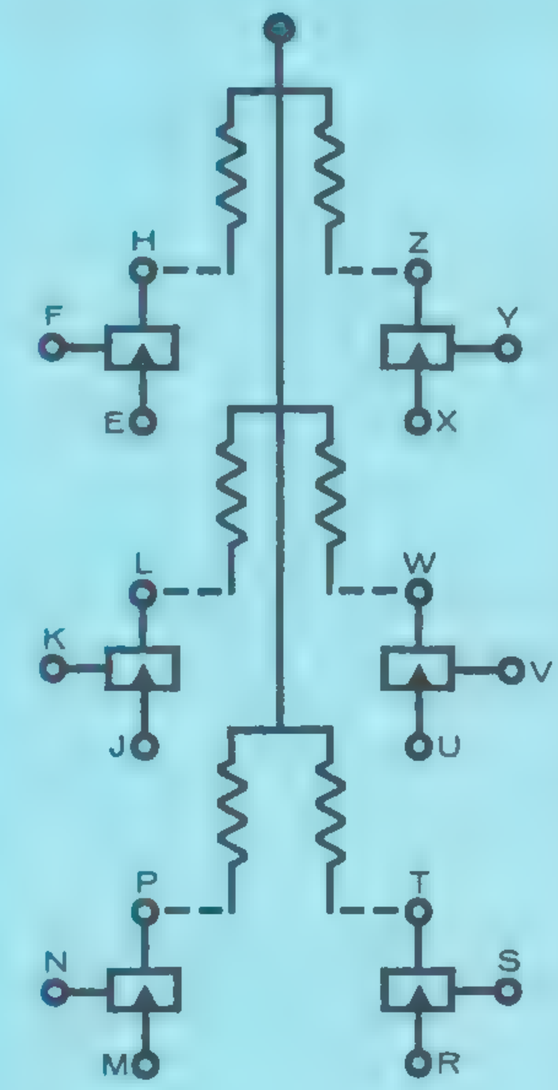
OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive 7 units of Base Load and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than three level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, four gates may be connected in series.

POWER: Type 4102 —15 volts/112 ma; +10 volts (A)/1.4 ma; +10 volts (B)/0 ma. **Type 4105** —15 volts/52 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.3 ma. **Type 4106** —15 volts/72 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

Additional information on 500 Kilocycle Inverter Usage is included in the Type 3101 Product Bulletin.



4102 INVERTER

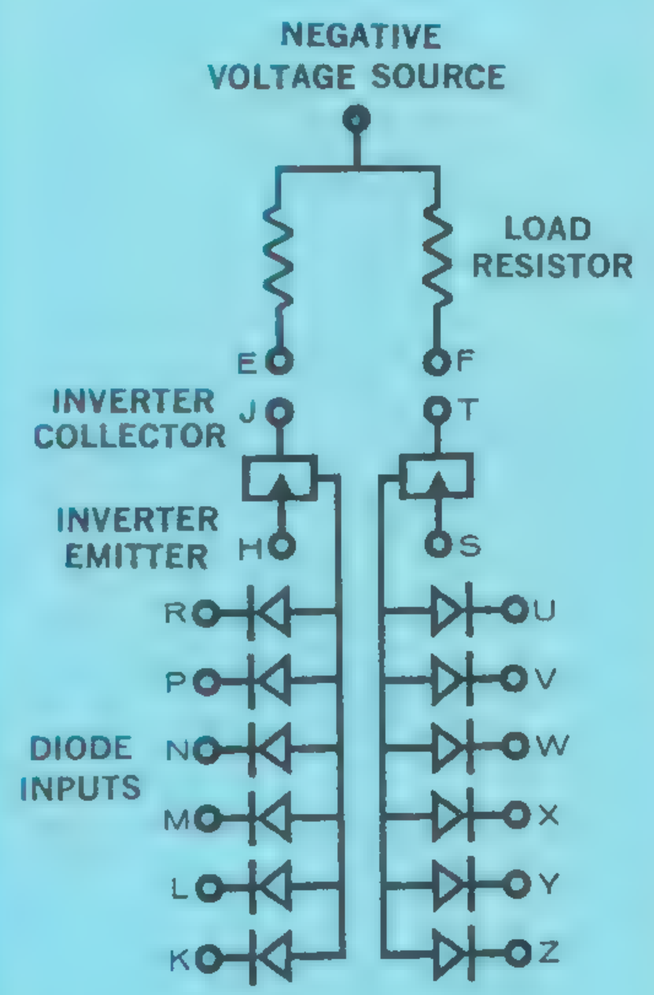


4106 INVERTER

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4110
DIODE



Two six-input diode gates are OR circuits for negative level inputs and AND circuits for ground inputs. Each diode gate is connected to the base of a transistor inverter which is similar to those in the DEC Inverter Type 4105. The emitter and collector are available for external connections. Delay of a level through a diode and its inverter is approximately 0.4 microsecond. This unit may also be used for pulse mixing. Since it will widen pulses, it should not be used at the Complement input of a Type 4201 flip-flop.

INPUT: Diodes — The inputs are DEC Standard Levels or equivalent (2 units of Base Load shared among the negative inputs) or DEC 0.4 microsecond 2.5 volt Negative Pulses (1 unit of Pulse Load). **Emitter** — DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

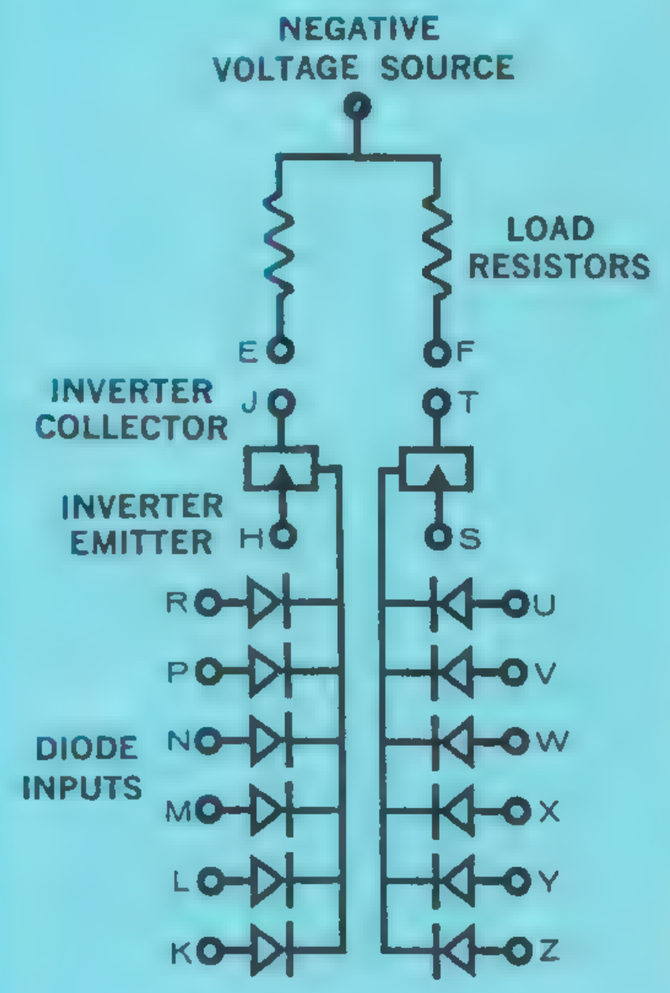
OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter or to the gated input of a flip-flop or other pulsed unit. A collector connected to a clamped load resistor can simultaneously drive 7 units of Base Load and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no load resistor attached can be connected to several emitters, providing not more than one inverter is conducting at a time. No more than two inverters may be added in series with the diode gate. If one inverter is used as a pulse gate, then three inverters may be connected in series with the diode gate.

POWER: −15 volts/42 ma; +10 volts (A)/0.9 ma; +10 volts (B)/0.9 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4111
DIODE



The Type 4111, like the Type 4110, contains 2 six-input diode gates, each connected to the base of a transistor inverter; however, this unit is an OR circuit for ground level inputs and an AND circuit for negative level inputs. The diode inputs of this unit may not be used for gating pulses since the turn-on time for the transistor may be too long. The emitter and collector of each inverter are available for external connections. Delay of a level through a diode and its inverter is approximately 0.4 microsecond.

INPUT: Diodes — DEC Standard Levels or equivalent supply the input to the diodes; the load is ⅛ unit of DC Emitter Load, shared by the ground inputs. **Emitter** — DEC Standard Levels or equivalent drive the inverter emitter; the emitter may be grounded if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

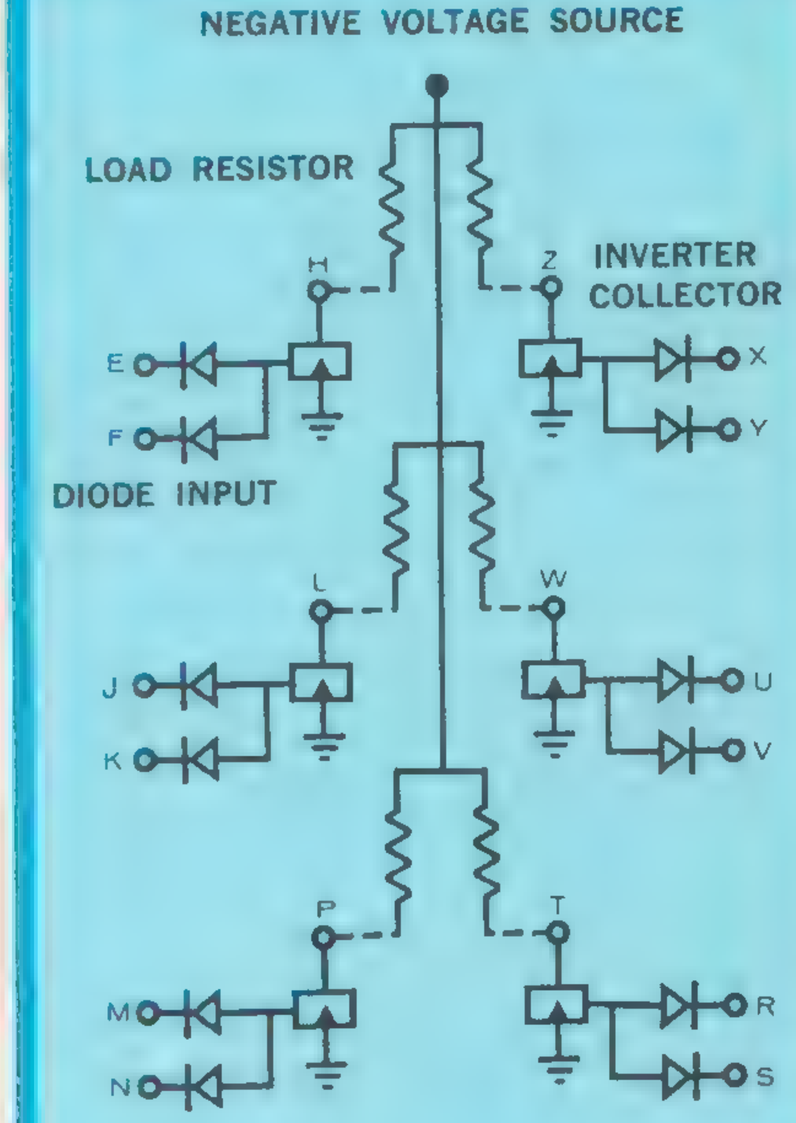
OUTPUT: Although the Type 4111 cannot be used as a pulse gate, it may be used to control a pulse gate when it is in a series string of inverters. The Type 4111 must be placed near the beginning of the series (the end farthest from the load). The inverter collector may be connected directly to a clamped load resistor or to the emitter of another inverter. A collector connected to a load resistor can simultaneously drive 7 units of Base Load and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no load resistor attached, can be connected to several emitters, providing not more than one inverter is conducting at a time. No more than two inverters may be added in series with the diode gate. If one inverter is used as a pulse gate, then three inverters may be connected in series with the diode gate.

POWER: −15 volts/45 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4112-4114
NEGATIVE DIODE NOR



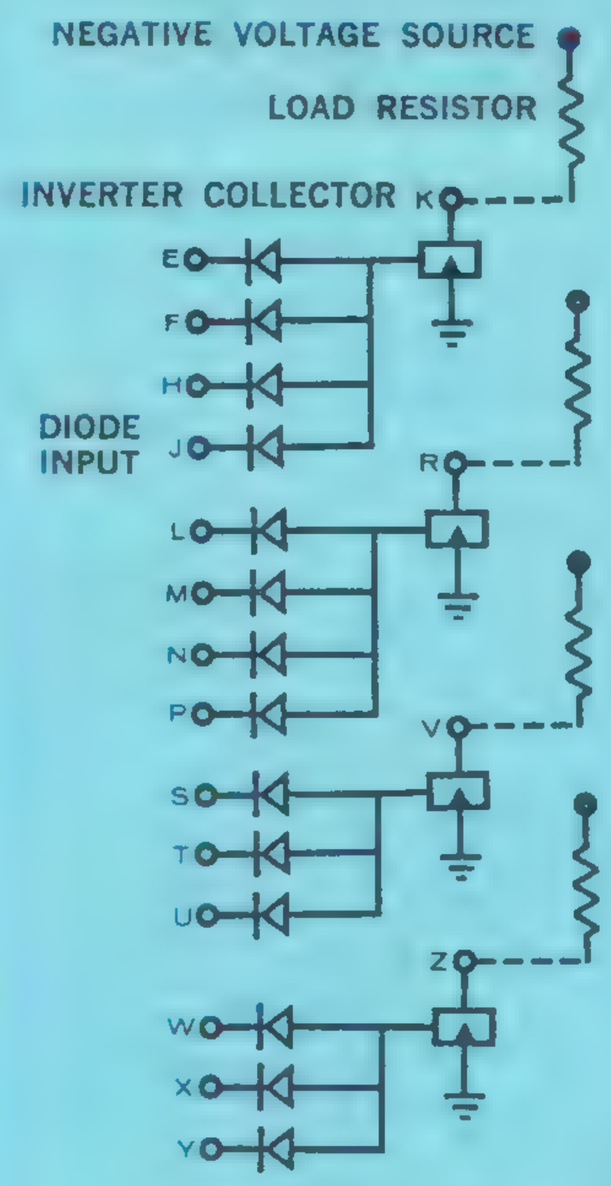
4112 NEGATIVE DIODE NOR

The diode gates form an AND circuit for ground levels or an OR circuit for negative levels. These units may also be used as pulse OR circuits for DEC Standard Negative Pulses. For power amplification each diode gate is connected to the base of a transistor inverter with a permanently grounded emitter. There are clamped load resistors which can be internally jumpered to the collector of each inverter. The maximum frequency for these units is 1 megacycle. Maximum delay before output rise is 0.05 microsecond. Maximum delay before output fall is 0.3 microsecond. The Type 4112 contains 6 two-input diode gates; the Type 4114, 2 three-input and 2 four-input diode gates.

INPUT: Inputs may be pulses or levels. The DC Load presented by the input is 1 unit of Base Load shared among the negative inputs. The transient load presented to a pulse input is 1 unit of Pulse Load.

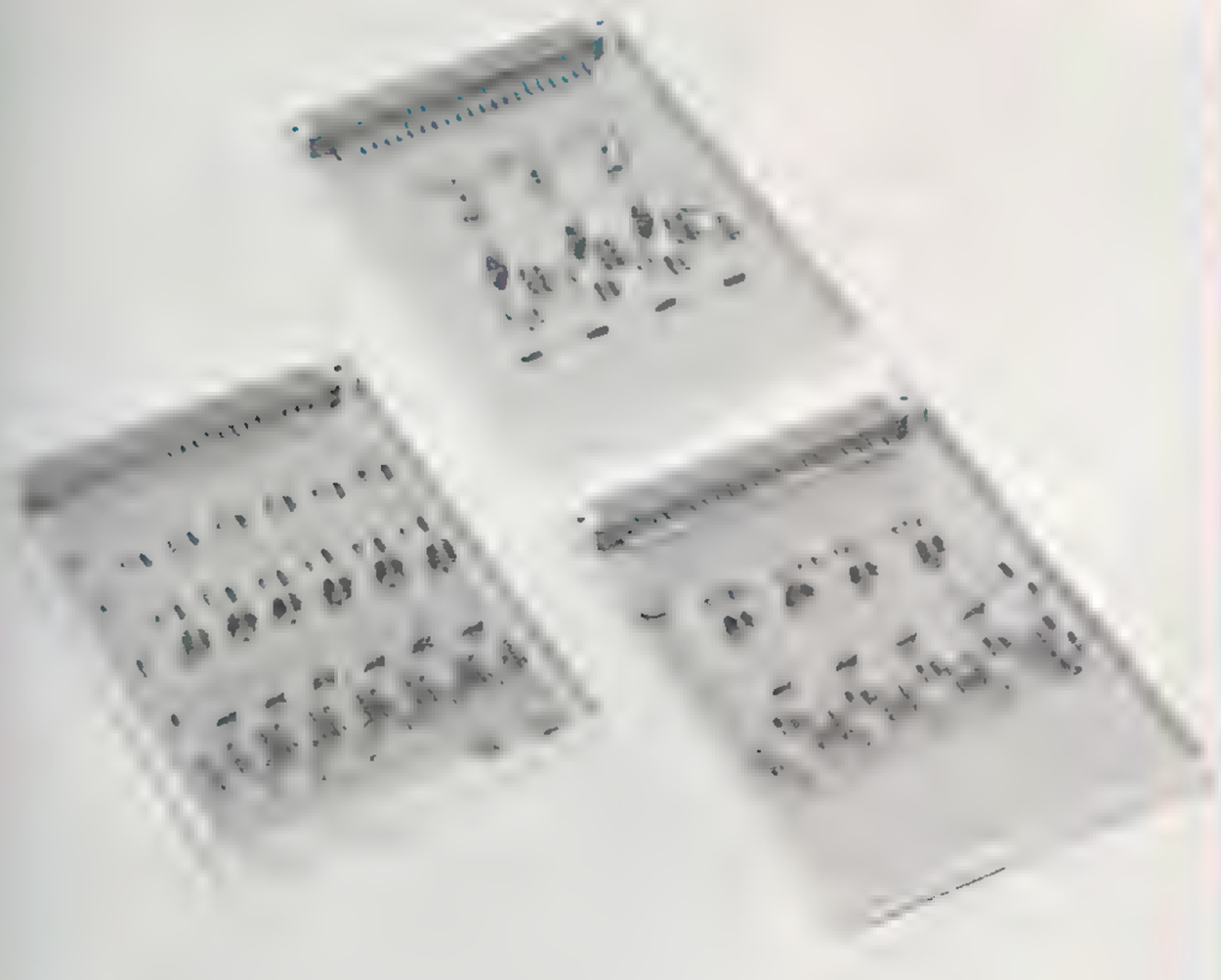
OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input of a flip-flop or other pulsed unit. A collector connected to a clamped load resistor can simultaneously drive 7 units of Base Load and any number of Pulsed Emitter Loads, provided not more than one is pulsed at a time. A collector, with no load resistor attached, can be connected to several emitters, provided not more than one inverter is conducting at a time. No more than one inverter may be added in series with the diode gate. A second inverter may be connected in series if it is used as a pulse gate.

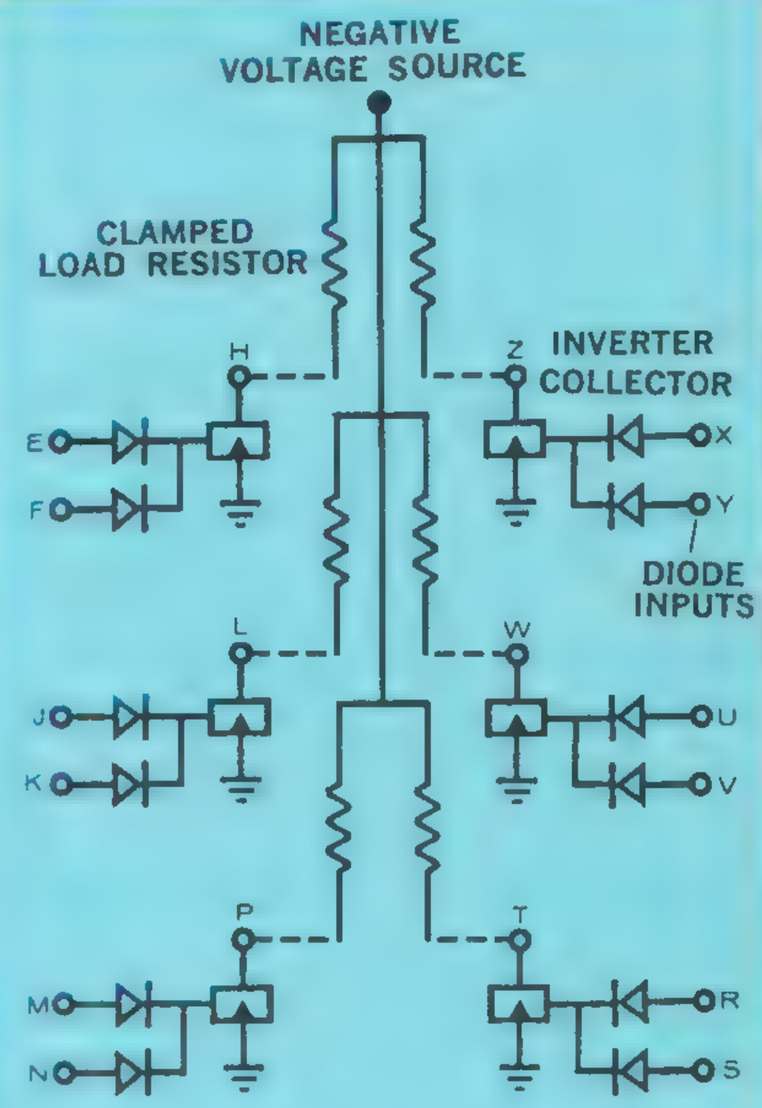
POWER: Type 4112: −15 volts/82 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma. **Type 4114:** −15 volts/62 ma; +10 volts (A)/0.35 ma; +10 volts (B)/0.35 ma.



4114 NEGATIVE DIODE NOR

4113-4115-4117
DIODES





4113 POSITIVE DIODE NOR

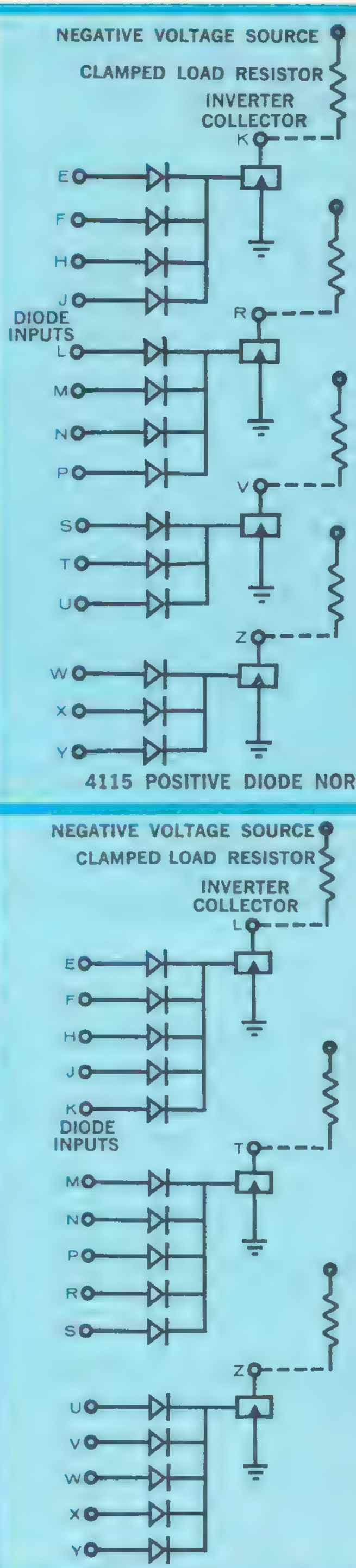
These diode gates are OR circuits for ground level inputs and AND circuits for negative level inputs. This type of gate may also be used to AND a single Negative Pulse with a number of conditioning levels. Each diode gate is connected to the base of a transistor inverter with a grounded emitter. Clamped loads are available and may be internally jumpered to the transistor collectors.

The Type 4113 contains 6 two-input diode gates; the Type 4115, 2 three-input, and 2 four-input diode gates; and the Type 4117, 3 five-input diode gates. These gates will operate at speeds up to 1 megacycle. Maximum delay for output fall is 0.08 microsecond; for output rise, 0.16 microsecond.

INPUT: DEC Standard Levels or DEC Standard 0.4 microsecond Pulses may be used for the inputs. The DC load presented by the inputs is ⅛ unit of DC Emitter Load. This load is shared by those inputs which are at ground. The transient load presented to a pulse input is 1 unit Pulse Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can simultaneously drive: (a) 7 units of Base Load, and (b) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. A collector with no clamped load resistor can be connected to several emitters, provided there is not more than one simultaneous emitter-collector path to a DC Emitter Load or to the pulse input of a flip-flop or other unit being pulsed. No more than one level gate can be connected in series with a diode gate. One additional pulse gate may also be connected in series.

POWER: Type 4113 −15 volts/88 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma. **Type 4115** −15 volts/67 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. **Type 4117** −15 volts/55 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.15 ma.



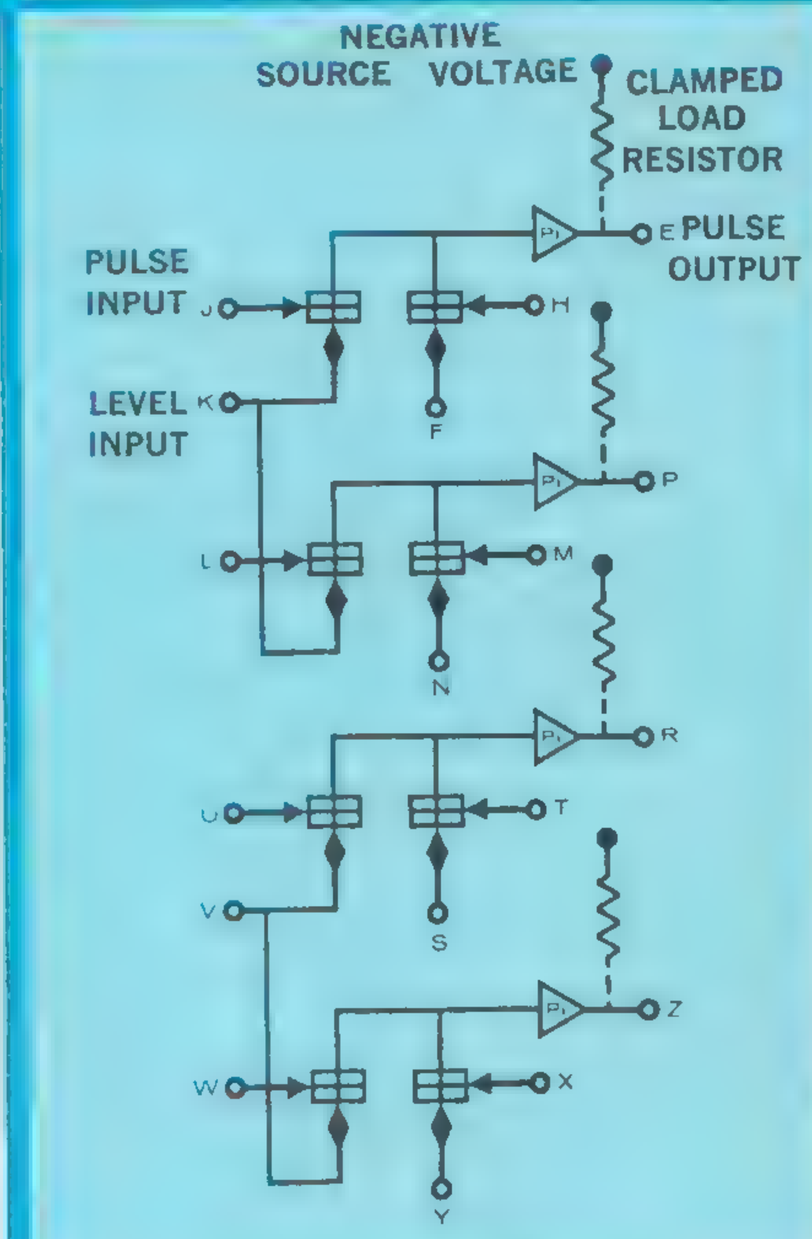
4115 POSITIVE DIODE NOR

4117 POSITIVE DIODE NOR

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4125-4127-4129
CAPACITOR-DIODE GATES



4125 PULSE INVERTER

The negative capacitor-diode gates contained in the Types 4125, 4127, and 4129 have a capacitor resistor diode circuit on the input and a standard DEC Inverter on the output for high driving capability. A clamped load resistor may be internally jumpered to each output.

Capacitor-diode gates will provide a logical delay for sampling a changing level and also differentiate a changing level to produce a pulse. When a changing level is to be differentiated, it is applied to the pulse input. If a level is to be pulse sampled at a time when it may be in the process of changing, it is applied to the conditioning level input. Since the internal capacitor will not discharge as fast as the level input will change, the output will be conditioned by the state of the level before the change occurred. The level set-up time required for negative capacitor-diode gate is one microsecond, hence, the maximum prf is 1 megacycle.

The Type 4125 contains four pair of 1500 ohm capacitor-diode gates with the output of each pair ORed together into a pulse inverter. Each pair of gates has two independent pulse input terminals, one independent conditioning level input, and one conditioning level input which is shared with the similar input of one of the other gates in the package. The Type 4127 contains six independent 1500-ohm capacitor-diode gates, each with a pulse inverter. The Type 4129 contains two circuits, each with four 1500-ohm negative capacitor-diode gates ORed into a single pulse inverter.

INPUT: Level — Inputs are DEC Standard Levels of 0 and −3 volts. The gate is enabled by a negative level, present at least 1 microsecond before the gate is pulsed. There is no DC load at the level input; the transient load is 2 units Base Load or ¼ unit DC Emitter Load, depending on the direction of the level change. (Note that two gates are driven from pins K and V of Type 4125.) **Pulse** — The pulse input may be driven from a Standard DEC 0.4 microsecond −2.5 volt Negative Pulse, or it may be driven from a negative-going level change. The level change should be 2.5 to 3.3 volts, with a maximum fall time of 0.5 microseconds. This input represents 1 unit of Pulse Load.

OUTPUT: The output circuit is similar to that of a DEC Type 4105 Inverter when the inverter is used as a pulse gate. Each time the capacitor-diode gate input conditions are met, a positive going pulse, three volts in amplitude and 0.15 to 0.4 microsecond in width is produced at the output. The output, (with no clamped load resistor attached) may drive the set, or clear input of a 4000 Series buffered flip-flop or the input to a 4301 Delay. With a clamped load resistor attached, a capacitor-diode gate may drive the input to a Type 4215 Flip-Flop, a 4303 Integrating One Shot, or a Type 4604 Pulse Amplifier.

POWER: Type 4125 −15 volts/62 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.3 ma. **Type 4127** −15 volts/82 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma. **Type 4129** −15 volts/42 ma; +10 volts (A)1.2 ma; +10 volts (B)/1.2 ma.

Figure 1 illustrates how pulse sampling of an unbuffered flip-flop is performed with a negative capacitor-diode gate. The unit being sampled is assumed to be a Type 4213 shift register and the sampling pulse is the same pulse which is used in shifting the register. The set-up time of the capacitor-diode gates assures that the output signal will not be split by a change in the conditioning level while it is being sampled.

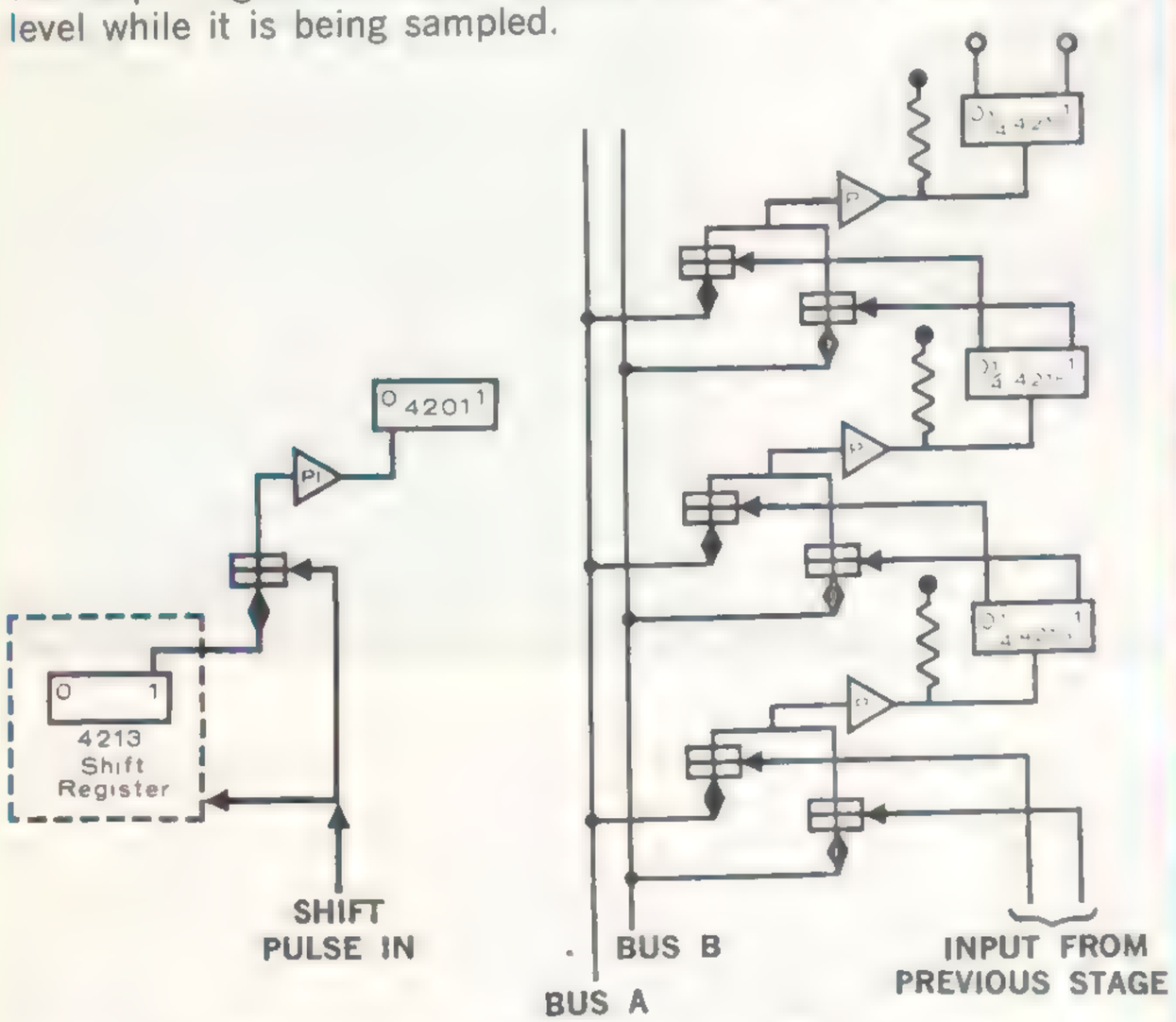
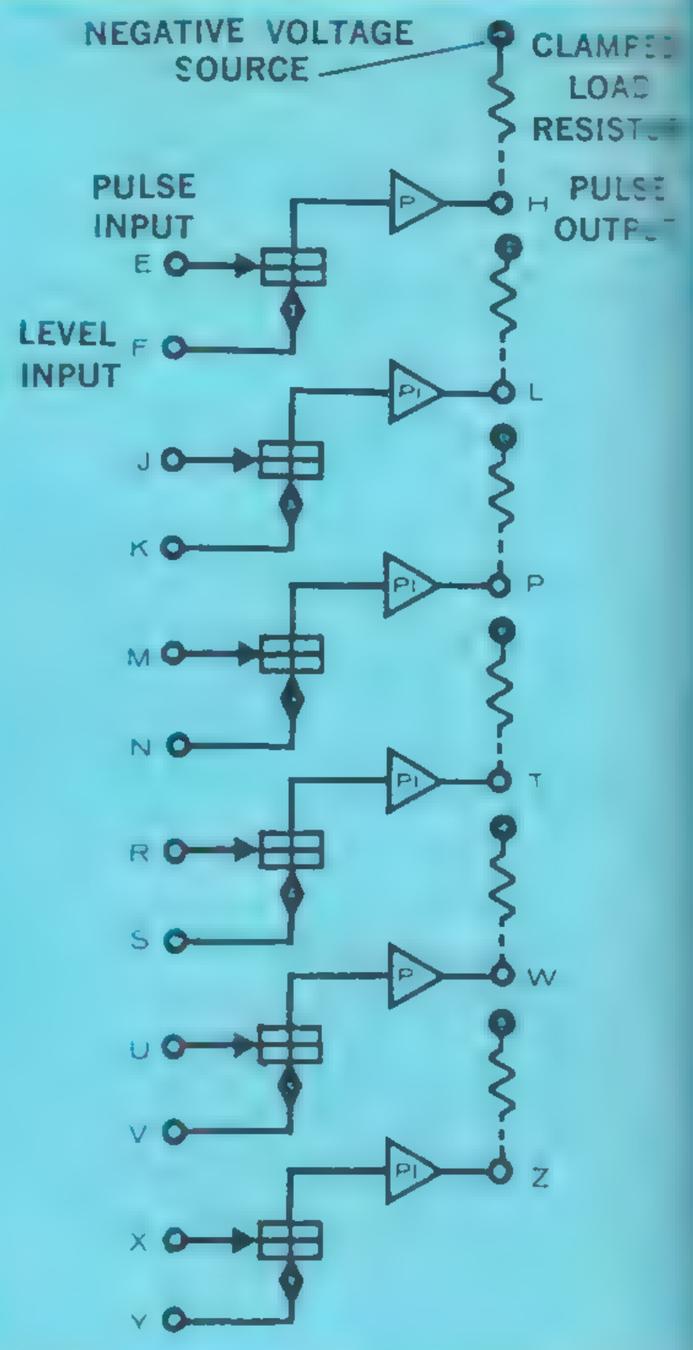


Figure 1

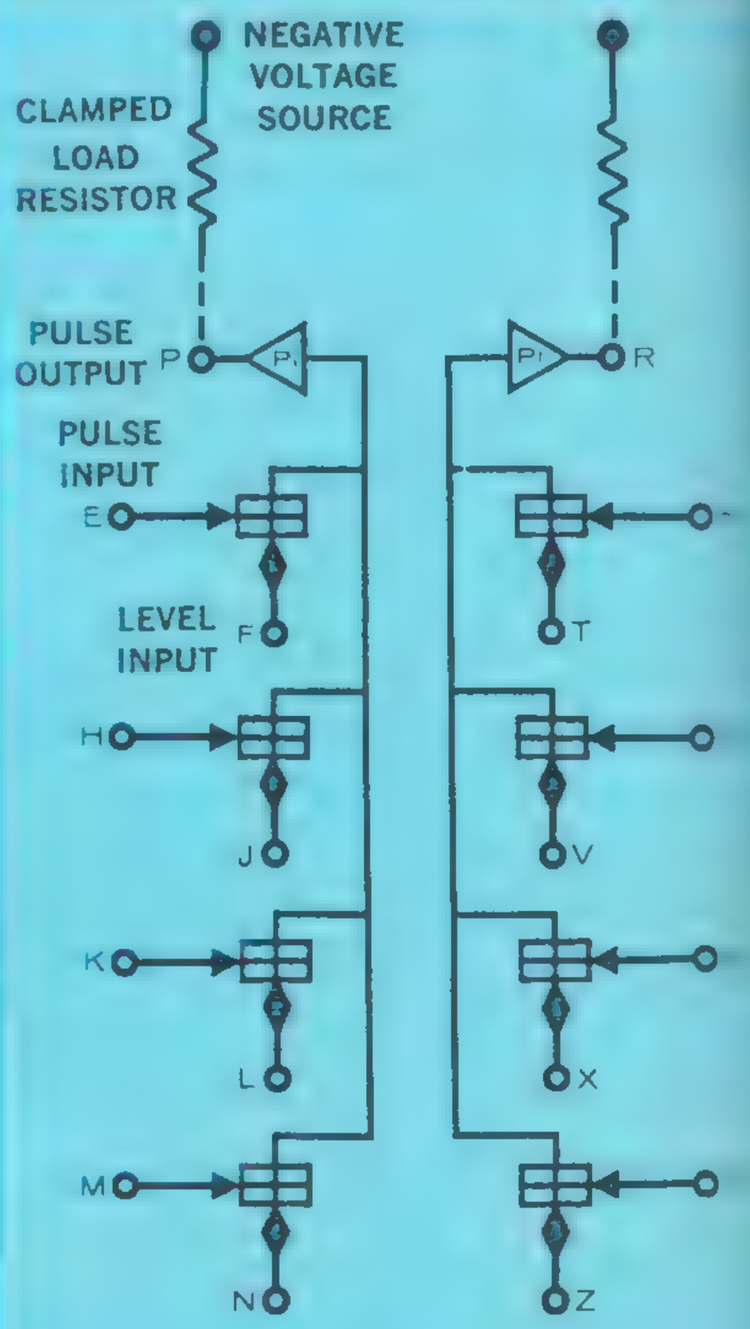
Figure 2 illustrates a binary up-down counter constructed from Type 4215 Flip-flops and Type 4125 Negative Capacitor-Diode Gates.

When Bus A is negative the carry chain is enabled and the system is in the up count mode. When Bus B is negative the borrow chain is enabled and the system is in the down count mode.

Carry and Borrow pulses are produced by differentiation of negative-going level changes which occur at the pulse input of enabled gates. Because of the set-up time requirements on the capacitor-diode gates, the enabling levels must be brought to their final at least 1 microsecond before the input pulse occurs and must remain at this value until the Carry (or Borrow) has had sufficient time to propagate the entire length of the counter. In this application the carry propagate time is 0.1 microsecond per bit; 50 nanoseconds for the gate and 50 nanoseconds for the flip-flop.

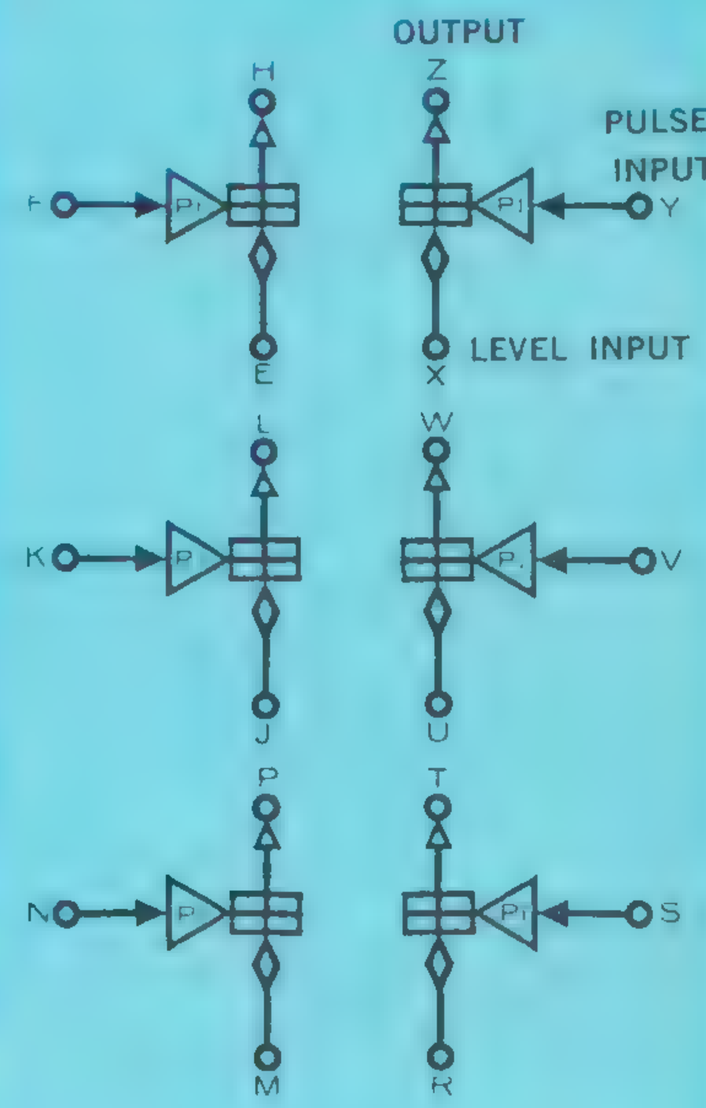


4127 PULSE INVERTER



4129 PULSE INVERTER

4126-4128
CAPACITOR-DIODE GATES



4126 PULSE INVERTER

The positive capacitor-diode gates Types 4126 and 4128 are for use in driving the ONE and ZERO inputs on the Type 4214 quadruple flip-flop package. The Type 4126 contains six individual gates. Each gate consists of a pulse inverter followed by a 2200-ohm capacitor-diode gate. The Type 4128 contains two circuits, each with a pulse inverter driving four 2200-ohm capacitor-diode gates.

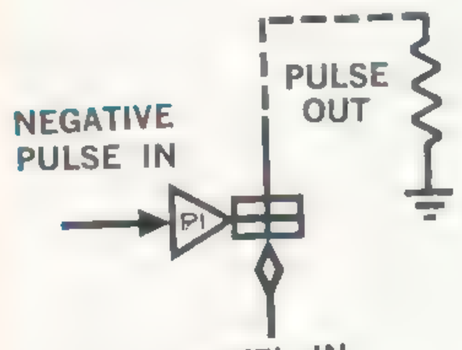
INPUT: The pulse inverter input requires DEC Standard 0.4 microsecond Negative Pulses and represents 1 unit of Pulse Load. The level inputs are ground for assertion. Level inputs must be present at least 1.5 microseconds before a shift or jam transfer type of read-in or at least 4.5 microseconds before a single ONE or ZERO read-in operation. See the circuit description.

OUTPUT: The output of the capacitor-diode gate is a positive going pulse from ground. Each capacitor-diode gate output will drive one input of a Type 4214 Flip-flop, and many such gates may be OR'ed into the same flip-flop input terminal.

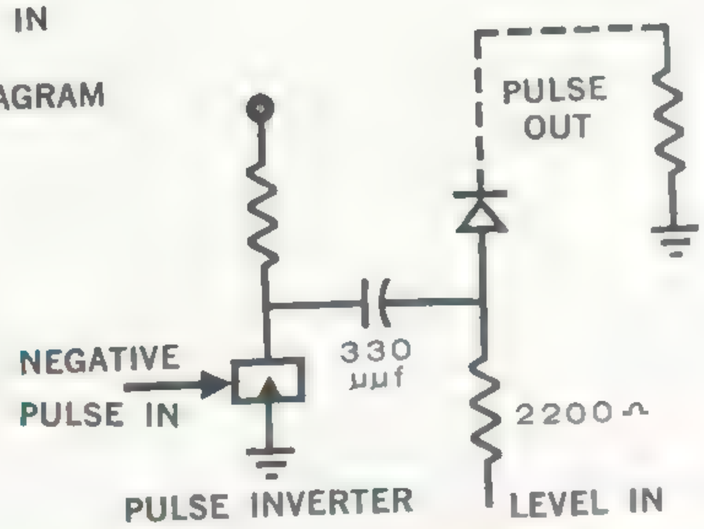
POWER: Type 4126: −15 volts/60 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma; **Type 4128:** −15 volts/35 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0 ma.

CIRCUIT DESCRIPTION

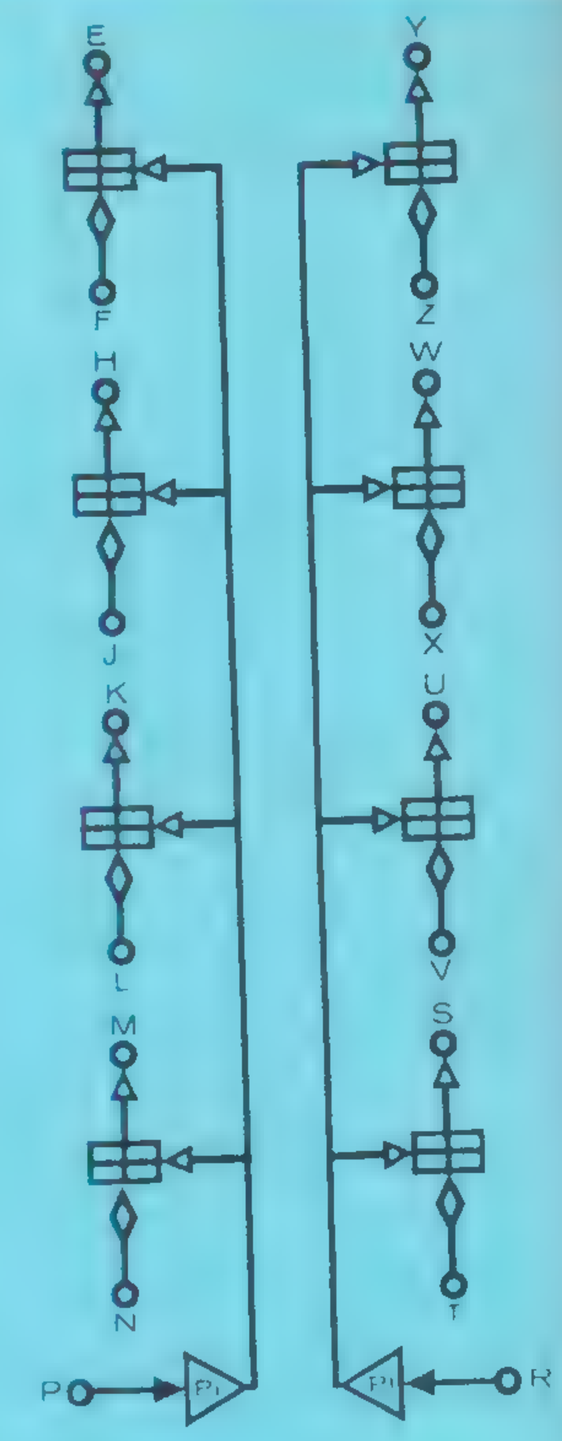
A negative pulse into the pulse inverter will cause the pulse inverter to generate a positive going pulse (from −3 volts to ground), which is applied to the capacitor of the capacitor-diode gate. If the input level had been at −3 volts for many time constants, there would be no output. If the input level had been at ground for many time constants, there would be a positive output pulse. The load on the gate must be at a ground level as shown; the inputs to a Type 4214 Flip-flop are of this type.



LOGIC DIAGRAM



CIRCUIT SCHEMATIC



4128 PULSE INVERTER

TYPICAL APPLICATION

In the shift or jam transfer, the gates are safely set up in 1.5 microseconds, just two time constants. After two time constants the correct gate surely will put out a considerably larger pulse than the other, and the flip-flop will follow it.

With the read-in connection 4.5 microseconds (six time constants) is a safe amount of time to allow for inhibiting a gate so that the capacitor will be fully discharged and no noise pulse will come out. Only 1.5 microseconds is needed to enable the gate. however. If the read-in information is coming from a flip-flop register that is also being cleared and read into, then these gates may be sampled 1.5 microseconds after the input data register is set. provided the input data register has been cleared for 3 microseconds before it was set.

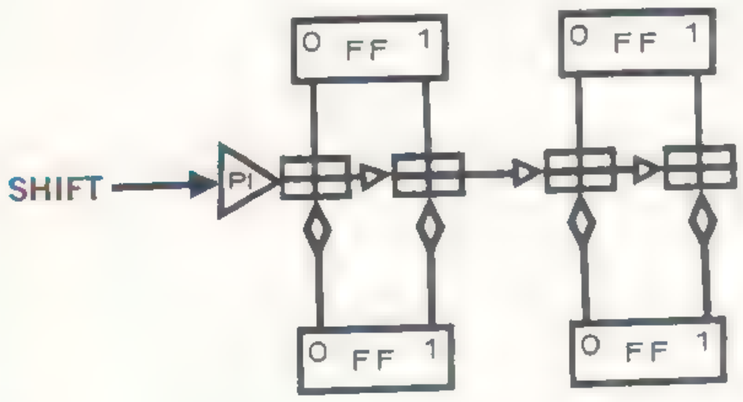


Figure 1 — SHIFT OR JAM TRANSFER, TYPE 4214 FLIP-FLOP AND TYPE 4128 GATE

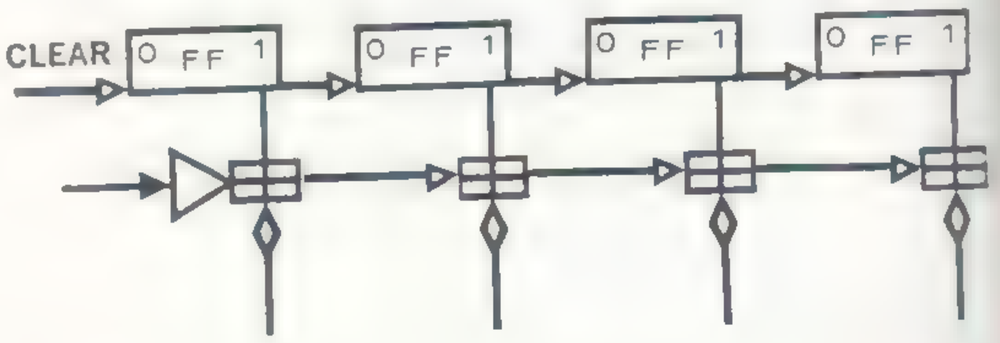
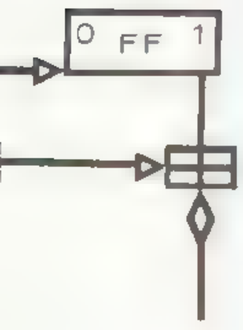


Figure 2 — READ-IN, TYPE 4214 FLIP-FLOP AND TYPE 4128 GATE

VERTER



P-FLOP AND

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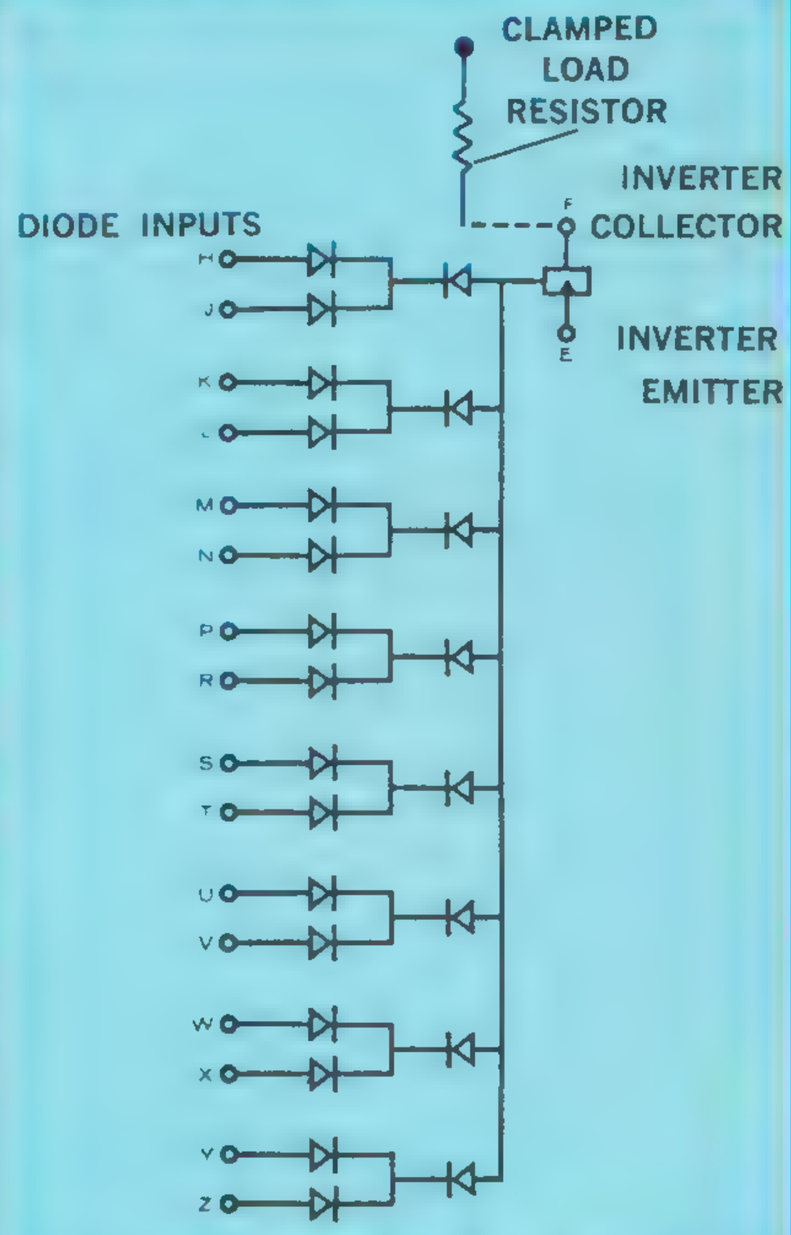
cleared and
sampled 1.5
gister is set,
been cleared

gtl

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4139-4141
NEGATIVE AND-OR DIODE GATES



4139 POSITIVE AND GATES

The Types 4139 and 4141 are versatile diode gates for performing two levels of logic. Each module contains one circuit whose output is a standard DEC inverter for signal amplification.

For negative input signals, the Type 4139 serves as eight 2-input AND gates ORed together. For ground input signals, this unit acts as eight 2-input OR gates ANDed together. A common use for this module is in the comparison of two 4-bit flip-flop registers to determine equality.

In the Type 4141, the diodes are brought to lugs on the circuit board so that a variety of logical interconnections can be made. Typical uses (for negative input signals) are as a 16 input AND gate or as four, 4 input AND gates ORed together. For ground input signals, the OR-AND functions are reversed. A typical application of this circuit is in determining the parity of three binary bits by the use of four, 3-input AND gates ORed together.

Back-to-back diode circuitry is possible because of an internal bias resistor connected to the input of each second stage diode. This bias holds the input of the second stage diode at −3 volts unless there is a ground connection from a first stage diode (or internally for the 4141). Total transition time for output rise is 0.2 microseconds, for output fall, 0.5 microseconds.

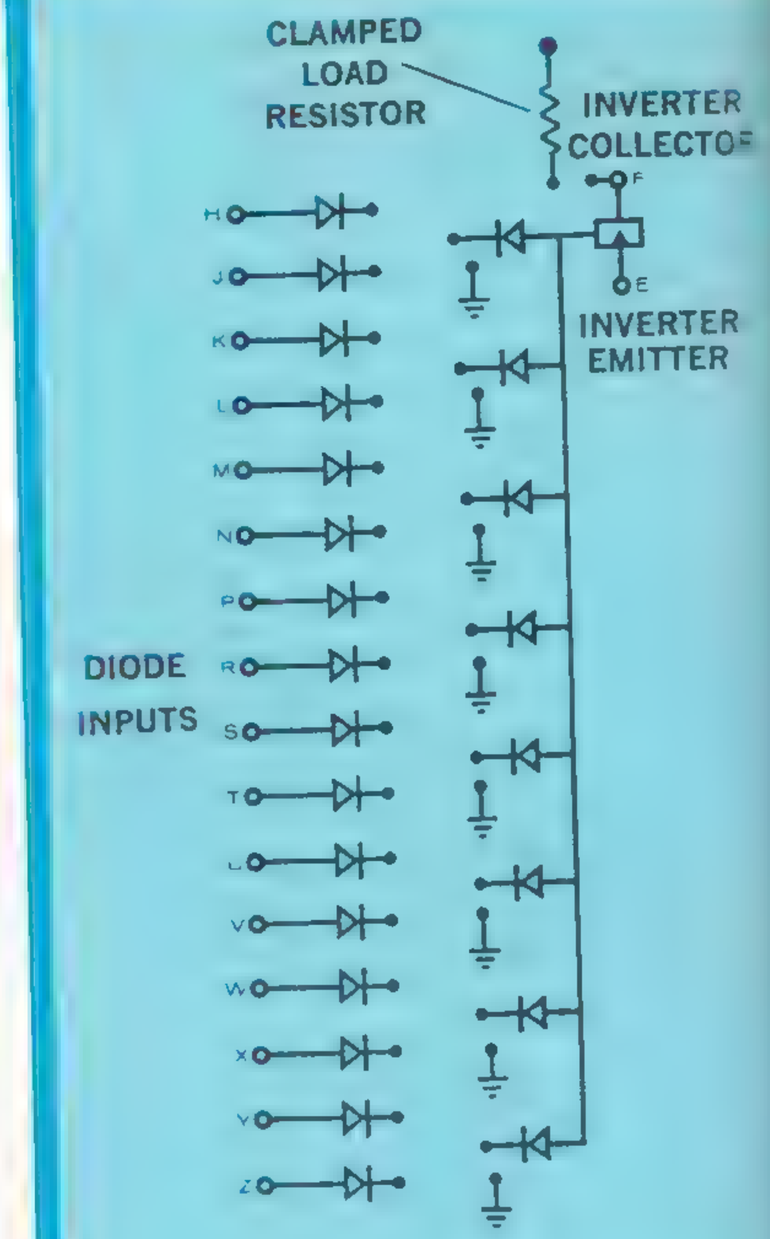
INPUT: The inputs are DEC Standard Levels. For the Type 4139, the DC load is ⅛ unit DC Emitter Load shared by each pair of inputs. When any pair of inputs is not being used, at least one of the pair should be grounded.

For the Type 4141, the input loading is determined by the bias resistor on the second stage diode. This load (⅛ unit DC Emitter Load) is shared by all first stage inputs connected to this point. All second stage diodes not in use should be grounded.

OUTPUT: The collector may be connected directly to a clamped load resistor or to the emitter of another inverter. A collector, connected to a clamp load resistor, can simultaneously drive 7 units of Base Load and any number of Pulsed Emitter Loads,

provided that not more than one is pulsed at a time. A collector, with no load resistor attached, can be connected to several inverter emitters, provided that not more than one inverter is conducting simultaneously. Only one level gate may be connected in series with the diode gate. If one of the series string is a pulse gate, then up to two inverters may be connected in series with the diode gate.

POWER: Type 4139: −15 volts/42 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0 ma. **Type 4141:** −15 volts/42 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0 ma.



4141 POSITIVE AND GATES

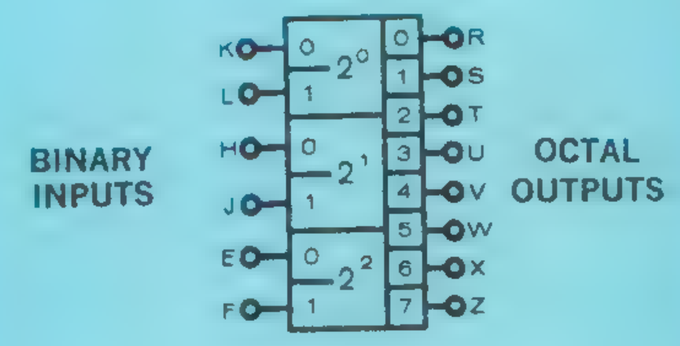
D GATES

digital

4000 SERIES
SYSTEM MODULES

500 KILOCYCLES

4150-4152
BINARY-TO-OCTAL
DECODER



The Types 4150 and 4152 convert three-bit binary information into eight lines of octal information with the selected output line at a negative voltage and the other seven output lines at ground. Decoding is accomplished with 8 three-input diode gates similar to those used in a DEC Type 4110 with all emitters grounded. The selected output line of the Type 4150 will be at −3 volts; for the Type 4152, the selected output line will be at −15 volts. For both modules, the total transition time is less than 0.2 microsecond for output rise and 0.9 microsecond for output fall.

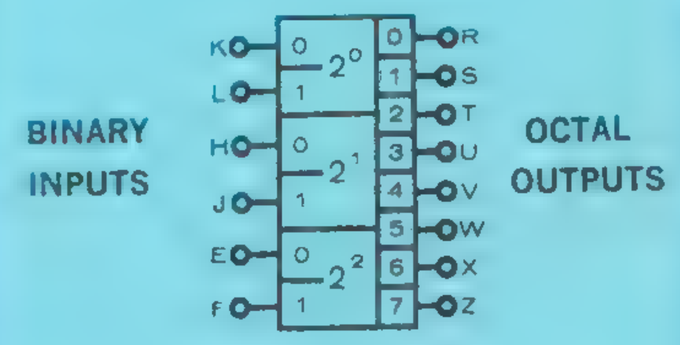
INPUT: DEC Standard Levels or equivalent drive the decoder which represents 5 units of Base Load per input when driven by three flip-flops. If inputs L, J, and F are at ground, output R is selected and is at its lower level of −3 volts for the Type 4150, and −15 volts for the Type 4152.

OUTPUT: Type 4150: Each output is a standard inverter collector connected to a clamped load resistor. Each output can simultaneously drive 4 units of Base Load (7 where speed is not a problem), and any number of Pulsed Emitter Loads,, providing not more than one is pulsed at a time.

Type 4152: Each output is a standard inverter collector connected internally to a 1500-ohm load resistor to −15 volts (no clamp). When the output is at ground, this unit can supply 7 ma. When the output is a negative voltage, the current is determined by the load resistor.

POWER: Type 4150: −15 volts/100 ma; +10 volts (A)/4.4 ma; +10 volts (B) 3 ma. **Type 4152:** −15 volts/70 ma; +10 volts (A)/ 4.4 ma; +10 volts (B)/3 ma.

4151-4153
BINARY-TO-OCTAL DECODER



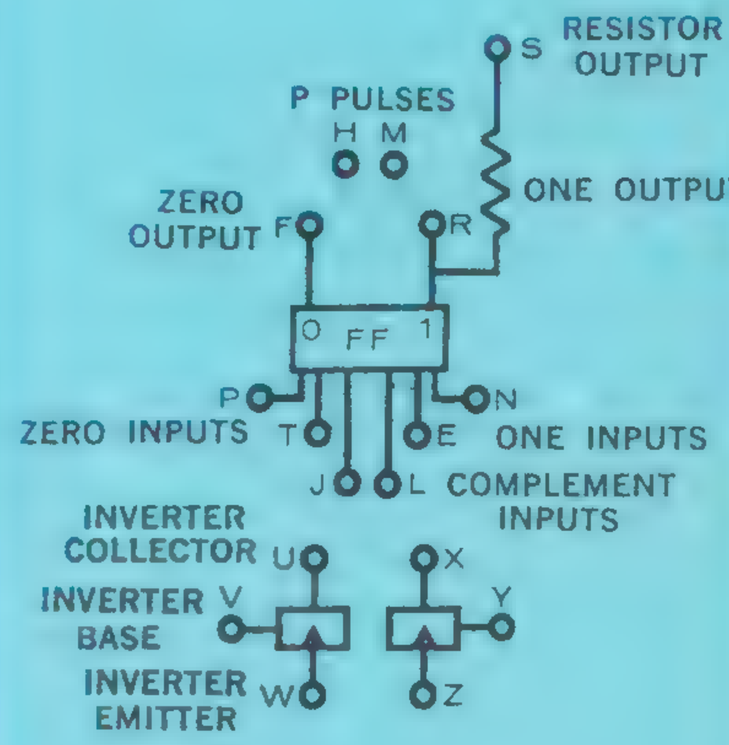
These units enable binary information in three flip-flops to be decoded into octal form with the selected output line at ground and the other seven output lines at a negative voltage. For the Type 4151, the unselected lines are at −3 volts; for the Type 4153, they are at −15 volts. Decoding is accomplished with 8 three-input diode gates similar to those used in the DEC Type 4111 with all emitters grounded. Total transition time is less than 0.8 microsecond.

INPUT: Inputs are DEC Standard Levels or equivalent. When driven by flip-flops, the load is 0.3 unit of DC Emitter Load. If inputs K, H and E are at −3 volts, output R is selected and is at ground.

OUTPUT: Type 4151: Each output is a standard inverter collector connected to a clamped load resistor. Each output can simultaneously drive 4 units of Base Load (7 where speed is not a problem), and any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. Total transition time is less than 0.8 microsecond. **Type 4153:** Each output is a standard inverter collector connected internally to a 1500-ohm resistor to −15 volts (no clamp). At ground the output can supply 7 ma. At −15 volts the output driving ability is determined by the load resistor. Total transition time is less than 0.8 microsecond.

POWER: Type 4151 — −15 volts/103 ma; +10 volts (A)/0.9 ma; +10 volts (B)/0 ma. **Type 4153 —** −15 volts/20 ma; +10 volts (A)/0.9 ma; +10 volts (B)/0 ma.

4201
FLIP-FLOP



The flip-flop in the Type 4201 has built-in output amplifiers, two gatable ZERO inputs, two gatable ONE inputs, and two independent sets of gatable Complement inputs with Carry output pulses. Two inverters, similar to those in the Type 4105, are included in the package for use as pulse or level gates. This general purpose flip-flop is very useful in making a high-speed carry counter or parallel adder.

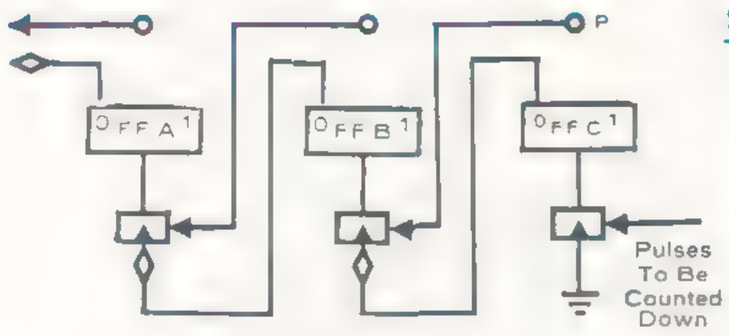
INPUT: The Complement signals (C_1 and C_2) must come from the collectors of one or more pulsed inverters. The ONE and ZERO inputs may also come from inverter collectors or they may be treated as Direct Set or Clear inputs. The driving signals for direct inputs are DEC Standard 0.4 microsecond Positive Pulses such as obtained from a DEC Pulse Amplifier Type 4603, Delay Type 4301 or Pulse Generator Type 4410. Any input which is used as Direct input cannot be driven by a pulse gate. The load presented by any flip-flop input is 1 unit Pulse Load. Input signals may occur in any sequence, but a minimum of 2 microseconds is required between consecutive signals (maximum frequency 500 kilocycles).

OUTPUT: ZERO and ONE outputs provide DEC Standard Levels each capable of simultaneously driving: (a) 14 units of Base Load, (b) 1 unit of DC Emitter Load, and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. The output signals have built-in delays which are greater than the input pulse widths, so the output can be sensed reliably at the same time as the input is pulsed. A resistor-coupled output suitable for driving a transistor indicator amplifier is provided. Each time the C_1 (or C_2) terminal is pulsed a DEC Standard 0.4 microsecond Negative Pulse, capable of driving 1 unit of Pulse Load, will occur at P_1 (or P_2) terminal. The carry propagate time is 0.05 microseconds per bit.

POWER: −14 volts/90 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

UP COUNTER

A typical up counter arrangement is shown in Figure 1. The pulses being counted enter on the right. They always complement flip-flop C and generate a Standard Pulse at P. This pulse complements flip-flop B whenever flip-flop C's state previous to its complement was a ONE. When B is complemented, a P Pulse is generated out of B that complements A if B held a ONE before it was complemented. This process is continued up the length of the counter until a flip-flop in the ZERO state is reached.



COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 1 — UP COUNTER

UP-DOWN COUNTER

The binary up-down counter, shown in Figure 2, subtracts as well as adds, using the two independent sets of Complement and P Pulse terminals. The C_1 and P_1 terminals are connected to form an up counter with a high speed carry chain, while the C_2 and P_2 form a down counter with a high speed borrow chain. Add and subtract pulses may arrive at any rate up to 500 kilocycles. (i.e. There must be 2 microseconds between two pulses on either the same or opposite terminals.)

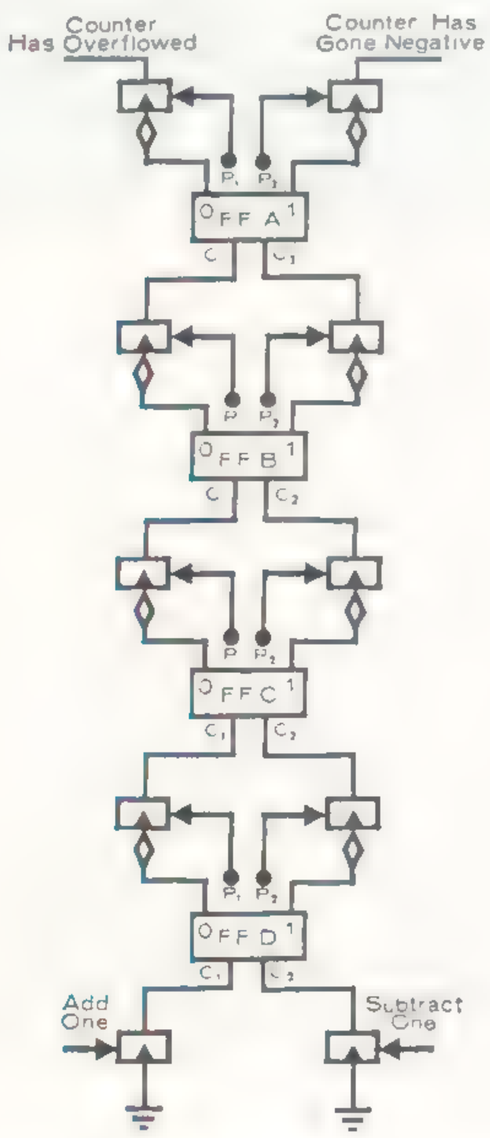
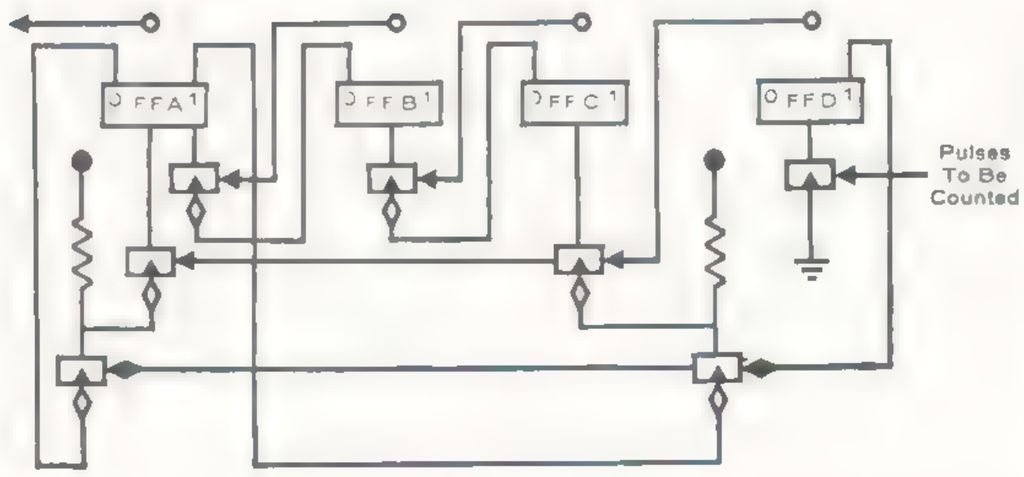


Figure 2 — UP-DOWN COUNTER

BINARY CODED DECIMAL COUNTER

The binary coded decimal counter, shown in Figure 3, converts the inherent binary count of a counter to binary coded decimal. The counter counts to 8, as in a standard up counter, except that no P Pulse is produced from flip-flop A. The count of 8 cuts off the path from flip-flop D to flip-flop C. The count of 9 establishes a path from the P output of flip-flop D to the Complement terminal of flip-flop A. The 10th count complements both flip-flop D and flip-flop A: the P Pulse of flip-flop A indicates a count of 10, and all the flip-flops in the counter are in the ZERO state ready to count to 10 again.



COUNTING SEQUENCE	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Figure 3 — BINARY CODED DECIMAL COUNTER

COUNTING SEQUENCE

0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

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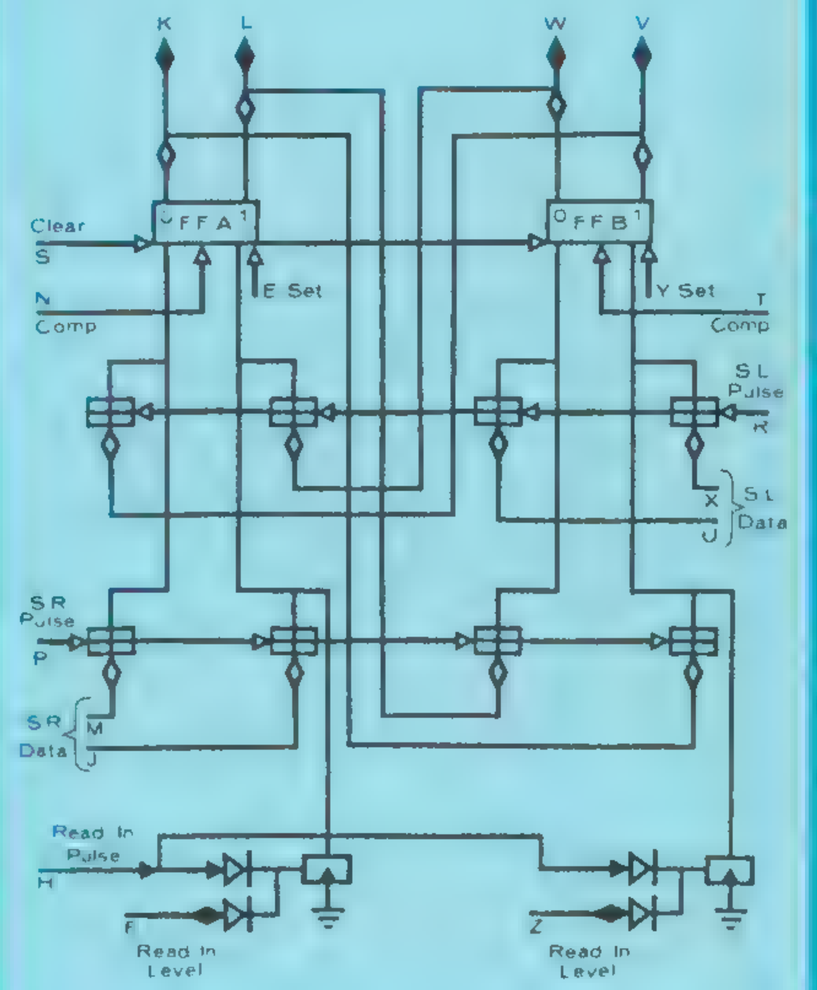
no P Pulse is
of 8 cuts off
The count of
of flip-flop D
A. The 10th
d flip-flop A;
nt of 10, and
e ZERO state

COUNTING SEQUENCE

0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4202
DUAL FLIP-FLOP



The DEC Type 4202 contains two flip-flops which perform shift-left or shift-right operations through internal connections. Read-in gates to the ONE side of each flip-flop are also built into the unit. Each of the 4202's flip-flops contains a buffer amplifier at each output. The flip-flops can be individually complemented, directly set or commonly cleared. Maximum operational frequency is 500 KC.

INPUT: Pulses: Complement, set, clear, and shift pulse inputs may be driven by DEC Standard 0.4 microsecond 2.5 volt positive pulses. Complement input (one unit pulse load) or shift pulse input (two units pulse load) may also be driven by the collector of a pulsed inverter or a negative capacitor-diode gate with clamped load resistor. Set input (one unit pulse load) may also be driven by the output of a positive capacitor diode gate. Clear input (two units pulse load) may be driven by two positive capacitor diode gates in parallel. **Levels:** The read-in level is negative for assertion. Load presented by this input is ⅛ unit DC Emitter load (1.25 ma when the input signal is at ground). Shift left data and shift right data inputs are 1500-ohm capacitor diode gates. Data inputs are complementary levels and must be present at least 1 microsecond before the corresponding shift pulse.

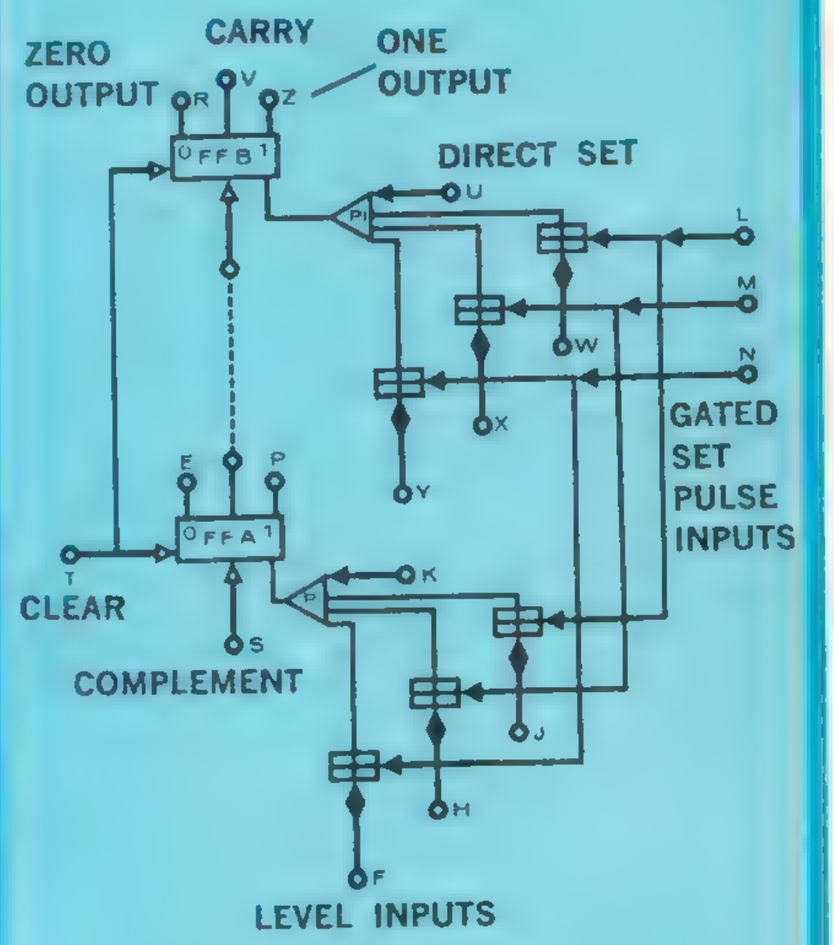
OUTPUT: ZERO and ONE outputs provide DEC standard levels each capable of simultaneously driving: (a) 14 units of Base Load, (B) 1 unit of DC Emitter Load, (C) any number of non-synchronously pulsed Emitter Loads. The output signals have built-in delays which are greater than the input pulse width so that they can be sensed reliably, at the same time that the input is being pulsed.

POWER: −15 volts/120 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4204
DUAL FLIP-FLOP



The Type 4204 dual flip-flop package is useful in flip-flop registers where high driving capability, counting, and several source read-ins are required. Each flip-flop is equipped with output buffers but there is no logical delay included in the unit. Total transition time is approximately 300 nanoseconds. The frequency limit is 1 megacycle.

Three gated set inputs and one direct set input are provided for each flip-flop. The three pulse lines drive two gates, one for each flip-flop. All six gates have separate conditioning lines. The clear terminal is common to both flip-flops.

The complement input of Flip-flop B may be internally connected to the carry of Flip-flop A; thereby forming an up counter. This connection is by means of lugs on the printed circuit board.

INPUT: Clear — Clear requires a 0.4 microsecond positive pulse (1 microsecond if the carry is connected). The Clear represents 1 unit of Pulse Load per flip-flop. **Complement** — Positive going level changes or positive pulses will complement Flip-flop A. This terminal represents 1 unit of Pulse Load and may be driven by an inverter, negative capacitor-diode gate or a DEC Standard 0.4 microsecond Positive Pulse. **Direct Set** — A direct set requires a DEC Standard 0.4 microsecond Negative Pulse or negative-going level change. If the level change is employed, the level must be ground for at least 0.5 microseconds before the negative transition occurs. It must have an amplitude of −2.5 to −3.5 volts and a fall time less than 0.25 microseconds. This terminal represents 1 unit of Pulse Load. **Gated Set** — The gated set inputs are negative capacitor-diode gates like those in the 4129. The pulse requirements for the gated set are the same as for the ungated set. The conditioning levels are −3 volts and they must be present at least 1 microsecond before the pulse is applied. There is no DC load, the transient load is ±2 ma. The equivalent circuit is 1500 ohms in series with 330 pf.

OUTPUT: ZERO and ONE outputs provide DEC Standard Levels each capable of simultaneously driving: a) 14 units of Base Load, b) 1 unit of DC Emitter Load, and c) any number of pulsed Emitter Loads

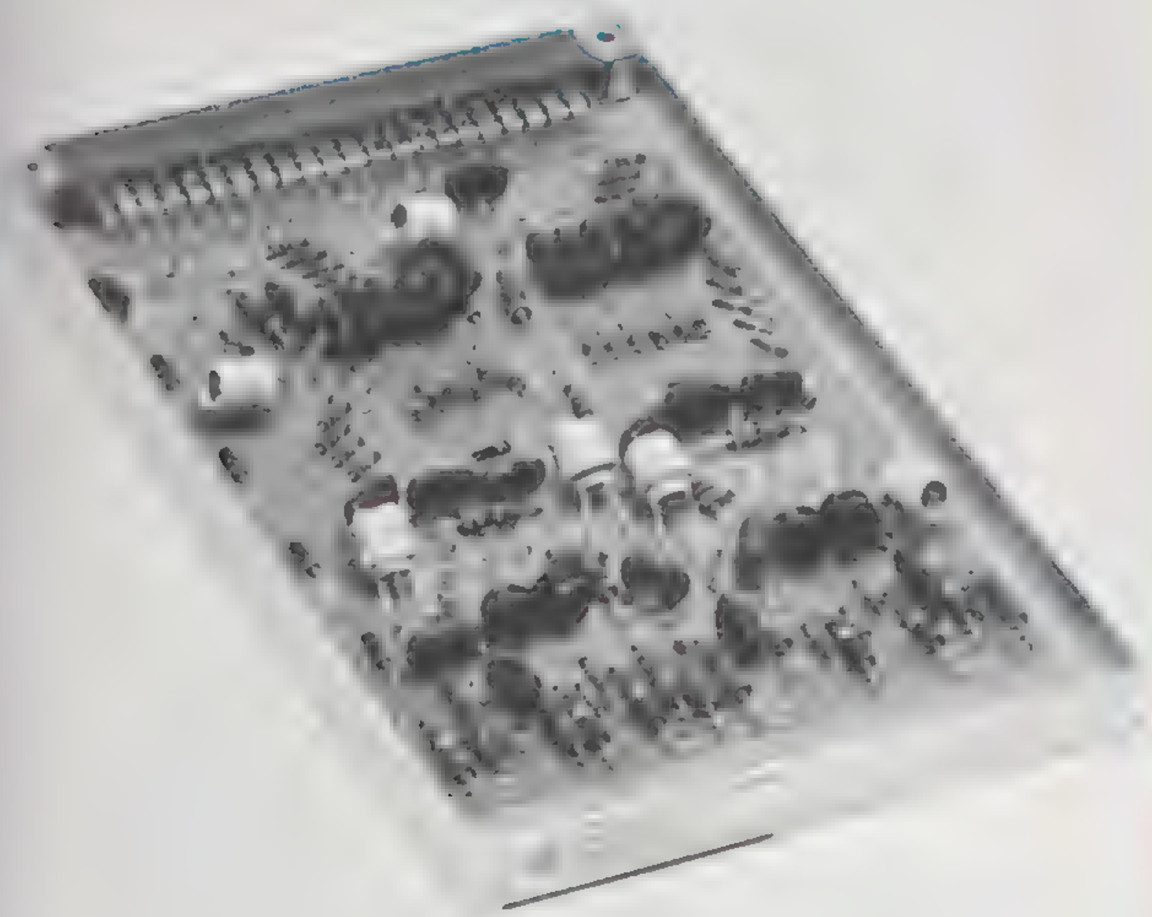
provided not more than one is pulsed at a time. The carry output of Flip-flop B is capable of driving up to two complement inputs.

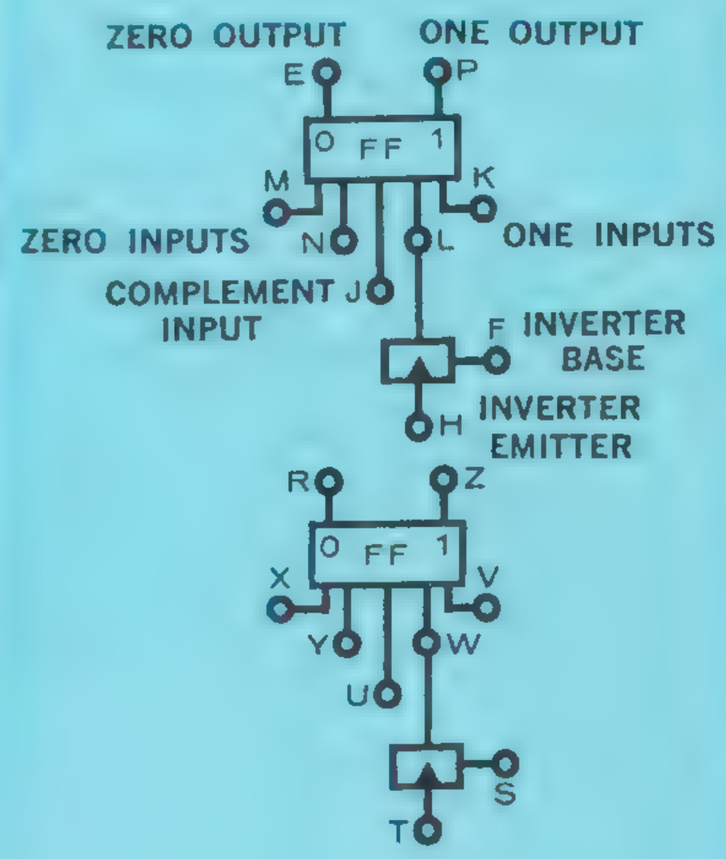
POWER: −15 volts/140 ma; +10 volts (A)/1.3 ma; +10 volts (B)/2.0 ma.

(A)/1.3 ma;

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4209
DUAL FLIP-FLOP





Each of two identical flip-flops have built-in output amplifiers, a gatable Complement input, and two gatable ONE and ZERO inputs. Each flip-flop also contains a pulse gate similar to the inverters in Types 4105, 4106 and 3101, which is internally connected to one of the gatable ONE input terminals. The output signals have built-in delays that are greater than the input pulse width. This module makes an efficient shift register, since the flip-flop can be sensed at the same time it is pulsed.

INPUT: Flip-flop inputs may be treated either as gated or as direct inputs; however, a single input may not be used in both manners. Each flip-flop input represents 1 unit Pulse Load. When used as a gatable input terminal, the input signal must come from the collector of one or more pulse gates. The base of the pulse gate must be driven by a DEC Standard 0.4 microsecond Negative Pulse or equivalent. When a flip-flop input is treated as a direct input, it must be driven by a DEC Standard 0.4 microsecond Positive Pulse (such as obtained from the output of a DEC Pulse Amplifier). Direct inputs may be tied in parallel for simultaneously clearing, setting or complementing all flip-flops in a register. The input signals may occur in any sequence, providing the minimum time between any two consecutive pulses is 2 microseconds (maximum frequency 500 kilocycles).

Inverter inputs are the same as those in Type 4105 when used as a pulse gate.

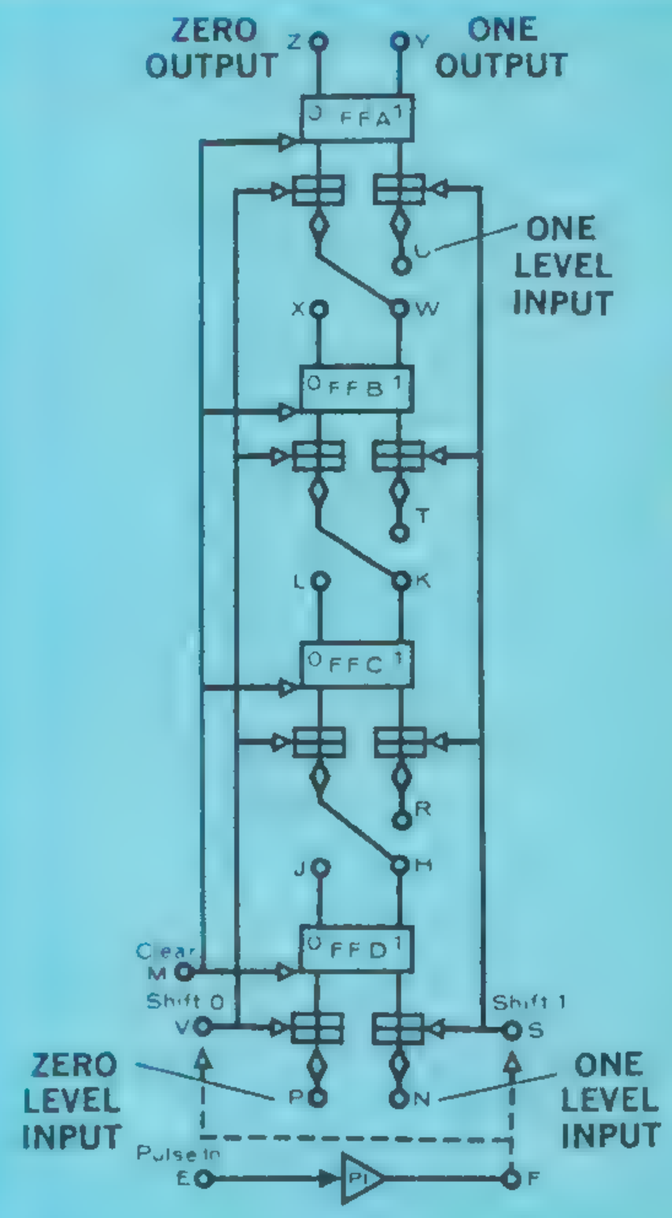
OUTPUT: ZERO and ONE outputs provide DEC Standard Levels each capable of simultaneously driving: (a) 14 units of Base Load; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads providing only one is pulsed at a time. The outputs have built-in delays, greater than the input pulse width, so that the flip-flop may be reliably sensed and pulsed simultaneously.

POWER: −15 volts/120 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4213
QUADRUPLE FLIP-FLOP



The Type 4213 contains four flip-flops with associated gates for connection as a shift or buffer register. A pulse inverter is included for driving the capacitor-diode gates during either a read-in or a shift operation. The flip-flops can be individually set or cleared by connecting appropriate pulse gates (such as DEC Type 4113 Diode units or Type 4127 Negative Capacitor-Diode Gates) to the proper output terminals. The maximum operating frequency is 1 megacycle.

INPUT: Pulse Inverter Input — a DEC Standard 0.4 microsecond Negative Pulse (1 unit of Pulse Load). **Clear Input** — a DEC Standard 0.4 microsecond Positive Pulse (1 unit of Pulse Load per flip-flop). Clear pulses may precede read-ins by as little as 1 microsecond. **Shift One** and **Shift Zero Inputs** — may be driven only by the output of the included pulse inverter. **Level Inputs** — are DEC Standard Levels or equivalent (ground assertion). There is no DC Load at these points. The transient load approximates 1 unit of Base Load. The level must be present at least 1 microsecond before a shift operation and 3 microseconds before a read-in operation.

The flip-flops may be set or cleared by connecting a Type 4113 Diode Gate to the appropriate output terminal. The gate will then be turned on by the coincidence of 2 Negative Levels, or of a Negative Level and a DEC Standard 0.4 microsecond Negative Pulse. The Type 4127 Capacitor-Diode Gate may also be used for this purpose.

OUTPUT: Each flip-flop provides DEC Standard Levels of 0 and −3 volts and may be loaded as described in the output loading rules. The outputs are unbuffered, and the delay is, therefore, short compared to the 0.4 microsecond pulse width. Typical delay is 0.05 microseconds. When the flip-flop output is to be sampled and changed at the same pulse time, provision must be made for logical delay. This delay may be provided by the use of a capacitor-diode gate (such as those in the 4125-4129 Series).

Output Loading

1. Each output may drive ±4 ma, 1500 pf, and a 1500-ohm capacitor-diode gate. Such gates are built into the 4213.
2. Loading of the ZERO and ONE outputs is independent.
3. An output cannot be used to gate emitters directly.
4. When an output is used to drive an inverter base, the emitter of that inverter must be grounded.
5. If the flip-flop is set by grounding the appropriate output terminal with an inverter, the emitter of that inverter must be grounded.
6. A 500 kc Base Load is 1 ma load at −3 volts in parallel with 680 pf. Five and 10 mc Base Loads are 1 ma load at −3 volts in parallel with 82 pf.

Typical Maximum Loading Applications

One internally-connected Capacitor-diode gate and any of the following:

1. Two 500 KC bases
2. One 500 KC base and three 5 MC bases
3. Four 5 MC bases
4. Three 1500-ohm capacitor-diode gate level inputs (as used in the 4213, 4216, and 4218)
5. Four 2200-ohm capacitor-diode gate level inputs (as used in the 4126 and 4128)
6. One 4110 diode and two 5 MC bases
7. Three 4111, 4112, or 4113 diodes

No Internally-connected capacitor-diode gate and any of the following:

1. Two 500 KC bases
2. One 500 KC base and three 5 MC bases
3. Four 5 MC bases
4. Two 1500-ohm capacitor-diode gate level inputs (as used in the 4213, 4216, and 4218)
5. Three 2200-ohm capacitor-diode gate level inputs (as used in the 4126 and 4128)
6. One 4110 diode and two 5 MC bases
7. Three 4111, 4112, or 4113 diodes

POWER: −15 volts/98 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

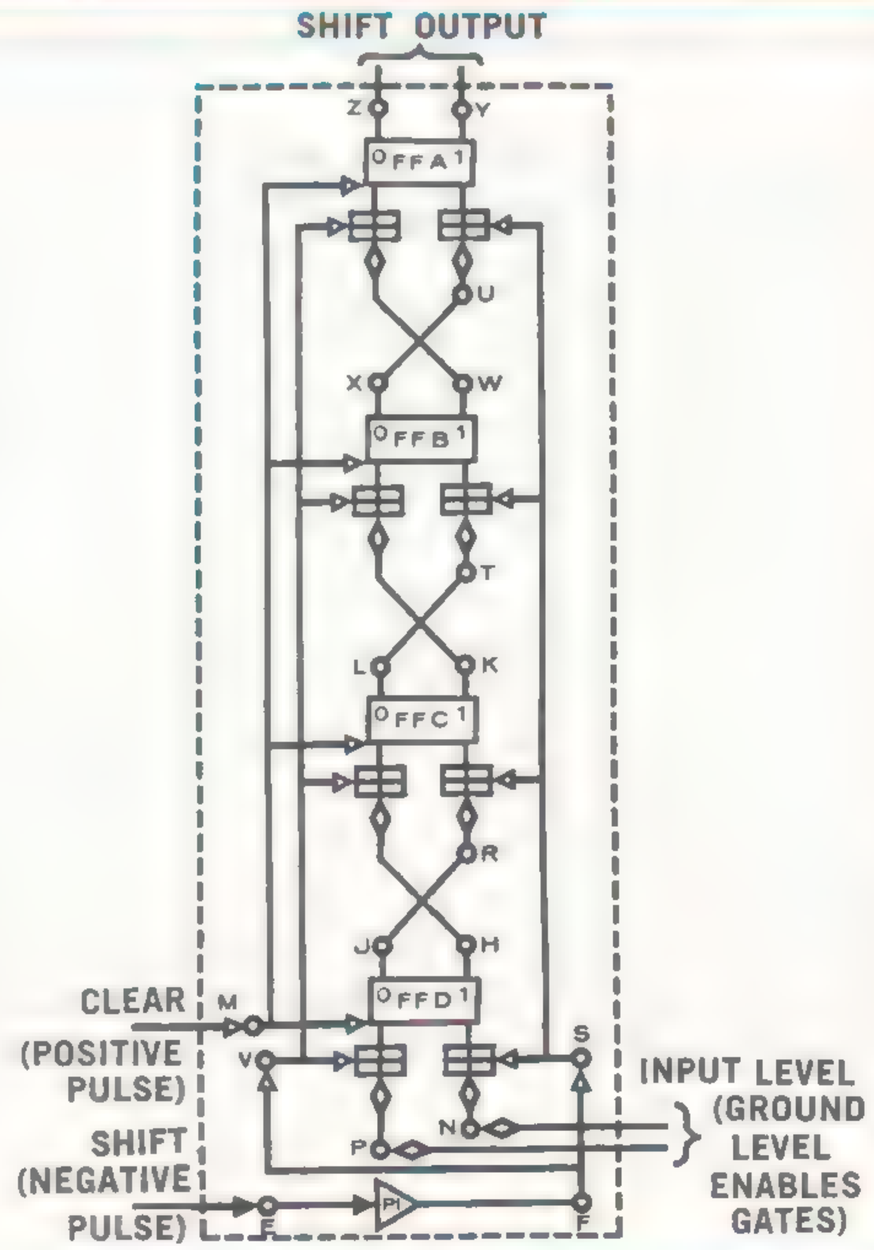
TYPICAL APPLICATIONS

SHIFT REGISTER

When connections are made as shown, each flip-flop controls the level inputs to the capacitor-diode gates in the next flip-flop in the shift register. For this application the pulse amplifier output is connected to both the Shift 1 and Shift 0 terminals. The contents of the flip-flops will advance one flip-flop upward for every input pulse. Maximum shift prf is 1 megacycle.

BUFFER REGISTER

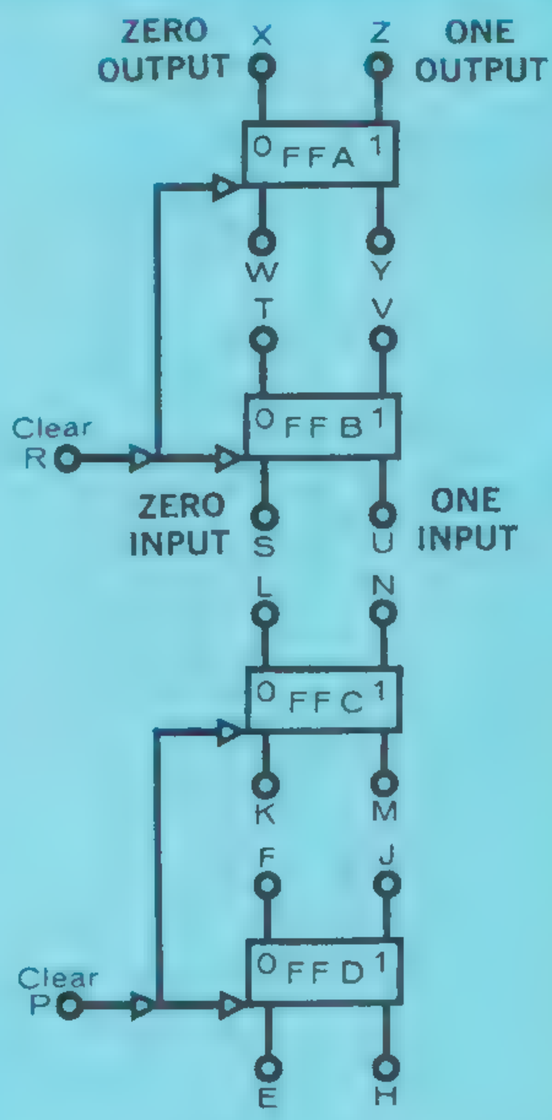
When used as a buffer register, the pulse amplifier output is connected to the Shift 1 terminal only. The input levels are connected to the ONE input gates. A ground level enables the gates. The gating level must be present at least 3 microseconds before the read-in pulse. The common Clear input is pulsed with a positive pulse to clear the entire register before reading in a new word. The Clear may precede the read-in by as little as 1 microsecond.



digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4214
QUADRUPLE FLIP-FLOP



The Type 4214 with its four flip-flops has been specially designed to meet Set-Reset application requirements. Two flip-flops share a Direct-Clear terminal. Flip-flop Set and Reset inputs should be driven from positive capacitor-diode gates (such as included in DEC Types 4126 or 4128). The Type 4214 operates up to 1 megacycle.

INPUTS: Clear Input — is a DEC Standard 0.4 microsecond Positive Pulse (1 unit of Pulse Load per flip-flop). Pulses may precede read-ins by as little as 1 microsecond. **Set and Clear Inputs** — may be driven by the DEC Standard Positive Pulse (1 unit of Pulse Load per input) or from the outputs of the capacitor-diode gates Types 4126 and 4128. The flip-flops may be set, or cleared, by connecting a Type 4113 Diode Gate to the appropriate output terminal. The gate will then be turned on by the coincidence of 2 Negative Levels; or of a Negative Level and a DEC Standard 0.4 microsecond Negative Pulse. The Type 4127 Capacitor-Diode Gate may be used for the same purpose.

OUTPUT: Each flip-flop output provides DEC Standard Levels of 0 and −3 volts and may be loaded as described in the output loading rules. The outputs are unbuffered, and the delay is, therefore, short compared to the 0.4 microsecond pulse width. Typical delay is 0.05 microsecond. When the flip-flop output is to be sampled and changed at the same pulse time, provision must be made for logical delay. This delay may be provided by the use of a capacitor-diode gate (such as those in the 4125-4129 Series).

Output Loading

1. Each output may drive ±4 ma, 1500 pf and a 1500-ohm capacitor diode gate.
2. Loading of the ZERO and ONE outputs is independent.
3. An output cannot be used to gate emitters directly.
4. When an output is used to drive an inverter base, the emitter of that inverter must be grounded.
5. If the flip-flop is set by grounding the appropriate output terminal with an inverter, the emitter of that inverter must be grounded.
6. A 500 kc Base Load is 1 ma load at −3 volts in parallel with 680 pf. Five and 10 mc Base Loads are 1 ma load at −3 volts in parallel with 82 pf.

Typical Maximum Loading Applications

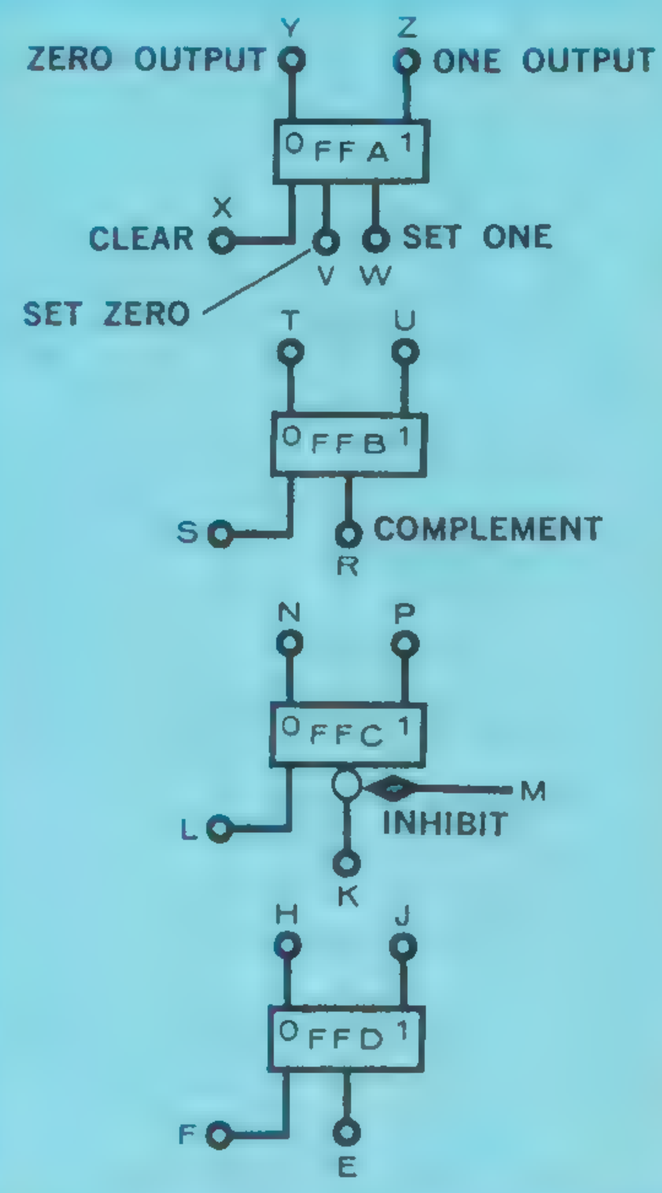
1. Two 500 kc bases and one 2200-ohm capacitor-diode gate.
2. One 500 kc base, three 5 mc bases and one 2200-ohm capacitor-diode gate.
3. Four 5 mc bases and one 2200-ohm capacitor-diode gate.
4. Three 1500-ohm capacitor-diode gate level inputs (as used in the 4213, 4216 and 4218).
5. Four 2200-ohm capacitor-diode gate level inputs (as used in the 4126 and 4128).
6. One 4110 diode, two 5 mc bases and one 2200-ohm capacitor-diode gate.
7. Three 4111, 4112, or 4113 diodes and one 2200-ohm capacitor-diode gate.

POWER: −15 volts/93 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4215
FOUR-BIT COUNTER



The DEC Four-Bit Counter Type 4215 contains four flip-flops which operate in the 0 to 1 megacycle range. Each flip-flop is logically independent, thus permitting complete versatility in system design applications. All logic connections are available at the connector, and separate Clear inputs are provided. All gating functions are performed internally. Carry propagate time per flip-flop is approximately 0.05 microsecond. Each flip-flop is provided with a Complement input which will accept either positive pulses or positive-going level changes. The Complement input of flip-flop A is divided so that the two terminals may be used as Set ONE and Set ZERO inputs. Flip-flop C is provided with an Inhibit so that a Negative Level applied to that terminal prevents the flip-flop from complementing from the ZERO to the ONE state. All counts from 1 to 12 (except 7 and 11), and the count of 16 can be obtained without additional logic.

INPUT: Complement — The Complement input may be a DEC Standard 0.4 microsecond Positive Pulse (1 unit of Pulse Load), a positive going pulse from an inverter or negative capacitor-diode gate, or a positive step of 3 volts with less than 0.2 microsecond rise time. Flip-flops will not complement on negative steps. Maximum Complement frequency is 1 megacycle. Set ONE and Set ZERO (flip-flop A) input requirements are the same as for Complement input. The Set ZERO will operate only when the flip-flop A is in the ONE state, and the Set ONE only when flip-flop A is in the ZERO state. Thus a Complement input terminal may be formed by connecting the Set ZERO and the Set ONE terminals. The load is then 1 unit of Pulse Load. **Inhibit** — A negative level of −3 volts at the Inhibit terminal prevents flip-flop C from complementing from the ZERO to the ONE state. However, flip-flop C will complement in the other direction. The load presented by this input is 2 units of Base Load. **Clear** — The Clear input must be a positive 1.0 microsecond, 2.5 volt pulse with less than 0.2 microsecond rise time that will inhibit carry propagation when the flip-flops are connected as a counter. When a flip-flop is not connected as a counter, a DEC Standard 0.4 microsecond Positive Pulse may be used. There is 1 unit of Pulse Load per input. Clear inputs may be tied in parallel, if desired. (The Type 4604 Pulse Amplifier will generate pulses of both widths.)

OUTPUT: Since positive going level changes are used for carry propagation, the Type 4215 is sensitive to capacitive loading. The fundamental load requirements are as follows:

1. Each output may drive a Type 4215 Complement input and ±4 ma of load with a maximum capacitance of 800 pf (above 500 kilocycles: ±1 ma load with 800 pf or ±4 ma with 200 pf).

2. Each output may drive an additional 200 pf capacitance if it is not driving a Complement input.

3. The ONE output of flip-flop C (pin P) can drive 2 ma less than the above at −3 volts.

4. The Inhibit input (M) represents 2 ma load at −3 volts with no appreciable capacitance.

5. Each input to flip-flop A is equivalent to 100 pf capacitance.

6. Loading of the ZERO and ONE outputs is independent.

7. The Type 4215 cannot be used to gate emitters directly.

8. When the Type 4215 is used to drive an inverter base, the emitter of that inverter must grounded.

9. If the Type 4215 is set by grounding the appropriate output terminal with an inverter, the emitter of that inverter must be grounded.

10. A 500 kilocycle Base Load is 1 ma load at −3 volts in parallel with 680 pf. Five and 10 megacycle bases are 1 ma load at −3 volts in parallel with 82 pf.

Typical Loading Applications
(at 500 kilocycles)

No Complement input and any of the following:

1. One 500 kilocycle base and three 5 megacycles bases. (One on P.)
2. Four 5 megacycle bases. (Two on P.)
3. Two capacitor-diode gate level inputs. (1500 ohm and 330 pf as used in Types 4213, 4216 and 4218.) (One on P.)
4. Three capacitor-diode gate level inputs. (2200 ohm and 330 pf as used in Types 4126 and 4128.) (Two on P.)
5. Two capacitor-diode gate pulse inputs.
6. One Type 4110 Diode. (None above 500 kilocycles.)
7. Three Type 4111 Diodes.
8. Four Types 4112, 4114 or 4116 Diodes. (Two on P.)
9. Three Type 4113, 4115 or 4117 Diodes.
10. One Type 4151 Binary-to-Octal Decoder.
11. One Type 1671 Binary Coded Decimal Light Driver.

One Complement input and any of the following:

1. One 500 kilocycle base and one 5 megacycle base.
2. Four 5 megacycle bases. (Two on P.)
3. One capacitor-diode gate level input, (1500 ohm and 330 pf as used in 4213, 4216 and 4218.) (None on P.)
4. Two capacitor-diode gate level inputs. (2200 ohm and 330 pf as used in 4126 and 4128.) (One on P.)
5. One capacitor-diode gate pulse input.
6. One Type 4110 Diode. (None above 500 kilocycles.)
7. Three Type 41-11 Diodes.
8. Four Type 4112 Diodes. (Two on P.)
9. Three Type 4113, 4115 or 4117 Diodes.
10. One Type 4151 Binary-to-Octal Decoder.
11. One Type 1671 Binary Coded Decimal Light Driver.

POWER: −15 volts/94 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

TYPICAL APPLICATIONS

Figure 1 illustrates how pulse sampling of an unbuffered flip-flop is performed with a negative capacitor-diode gate. The unit being sampled is assumed to be a Type 4213 shift register and the sampling pulse is the same pulse which is used in shifting the register. The set-up time of the capacitor-diode gates assures that the output signal will not be split by a change in the conditioning level while it is being sampled.

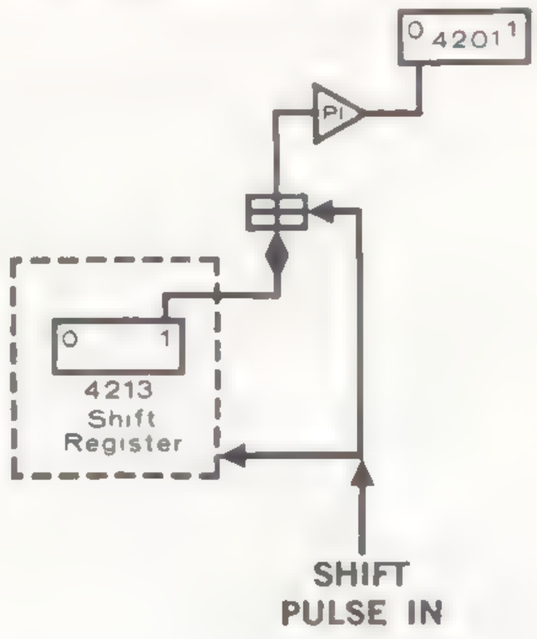


Figure 1

Figure 2 illustrates a binary up-down counter constructed from Type 4215 Flip-flops and Type 4125 Negative Capacitor-Diode Gates.

When Bus A is negative the carry chain is enabled and the system is in the up count mode. When Bus B is negative the borrow chain is enabled and the system is in the down count mode.

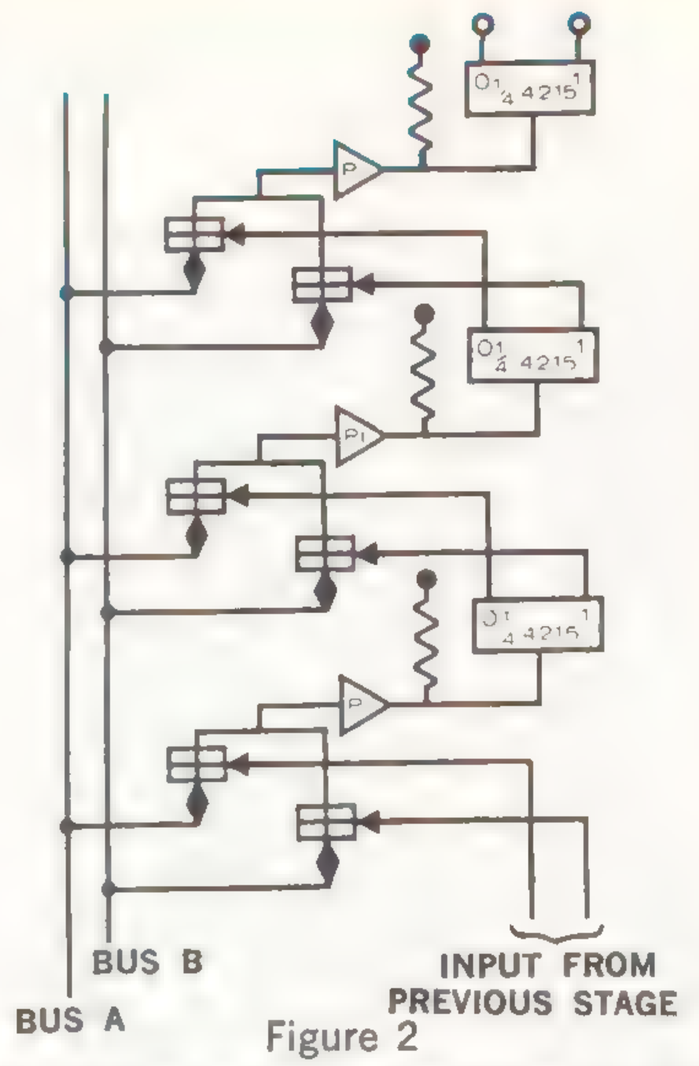
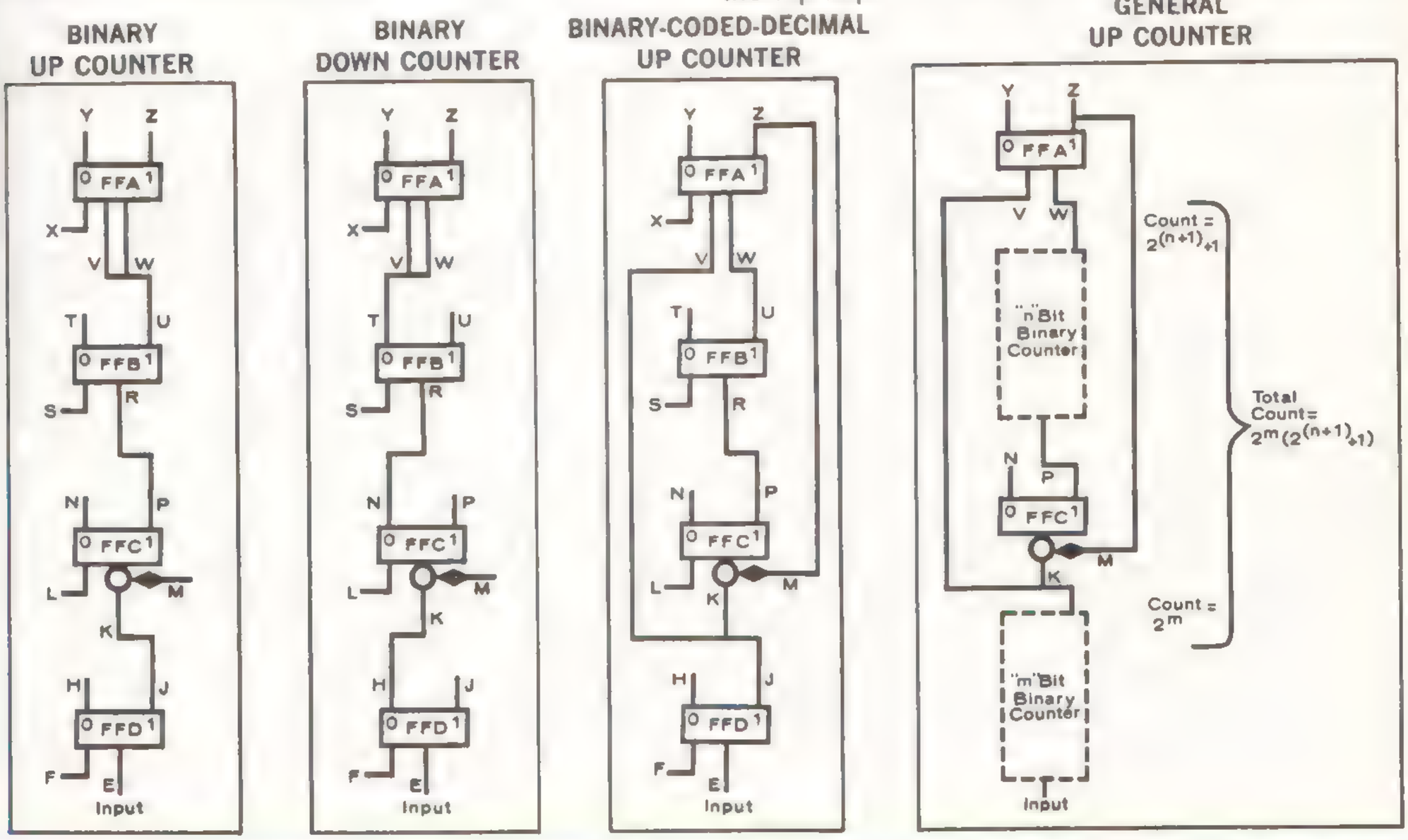


Figure 2

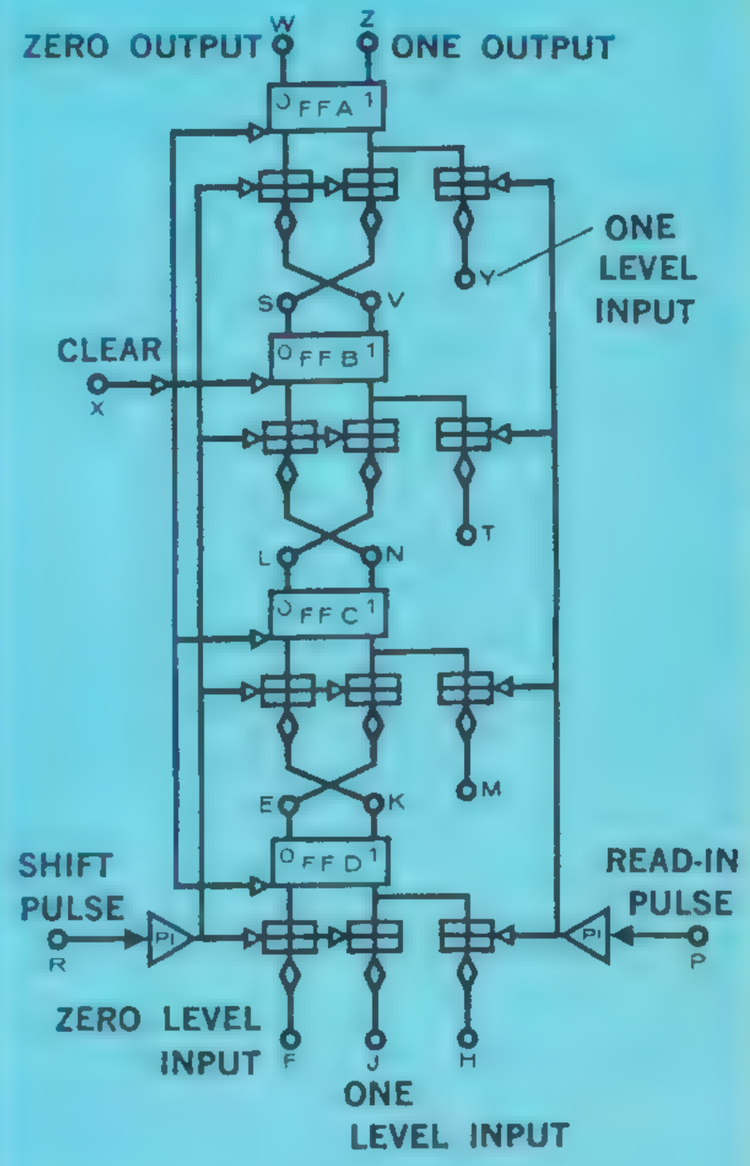
Carry and Borrow pulses are produced by differentiation of negative-going level changes which occur at the pulse input of enabled gates. Because of the set-up time requirements on the capacitor-diode gates, the enabling levels must be brought to their final at least 1 microsecond before the input pulse occurs and must remain at this value until the Carry (or Borrow) has had sufficient time to propagate the entire length of the counter. In this application the carry propagate time is 0.1 microsecond per bit; 50 nanoseconds for the gate and 50 nanoseconds for the flip-flop.



digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4216
QUADRUPLE FLIP-FLOP



The Type 4216 is a four flip-flop shift register package with gates included for parallel read-in of ONE's. This unit is particularly useful for parallel-to-serial conversion. All flip-flop output terminals are available. Level inputs are by 1500-ohm capacitor-diode gates. Two pulse inverters are included, one for driving each set of the above gates. For additional parallel inputs, pulse gates (such as DEC Type 4113 Diode units or Type 4127 Negative Capacitor-Diode Gates) may be attached to the appropriate output terminals. The maximum operating frequency is 1 megacycle.

INPUT: The **Read-In** and **Shift Inputs** are DEC Standard 0.4 microsecond Negative Pulses (1 unit of Pulse Load). **Clear** — is a DEC 0.4 Standard microsecond Positive Pulse (1 unit of Pulse Load per flip-flop). Clear pulses may precede read-ins by as little as 1 microsecond. **Level Inputs** are DEC Standard Levels or equivalent (ground for assertion). There is no DC Load at these points. The transient load approximates 1 unit of Base Load. The level must be present at least 1 microsecond before a shift operation and 3 microseconds before a read-in operation.

The flip-flops may be set, or cleared, by connecting a Type 4113 Diode Gate to the appropriate output terminal. The gate will then be turned on by the coincidence of 2 Negative Levels; or of a Negative Level and a Standard DEC 0.4 microsecond Negative Pulse. The Type 4127 Capacitor-Diode Gates may be used for the same purpose.

OUTPUT: Each flip-flop output provides Standard DEC Levels of 0 and −3 volts, and may be loaded as described in the output loading rules. The outputs are unbuffered, and the delay is, therefore, short compared to the 0.4 microsecond pulse width. Typical delay is 0.05 microseconds. When the flip-flop output is to be sampled and changed at the same pulse time, provision must be made for logical delay. This delay may be provided by the use of a capacitor-diode gate (such as those in the 4125-4129 Series).

Output Loading

1. Each output may drive ±4 ma, 1500 pf and a 1500-ohm capacitor-diode gate. Such gates are built into the 4216.
2. Loading of the ZERO and ONE outputs is independent.
3. An output cannot be used to gate emitters directly.
4. When an output is used to drive an inverter base, the emitter of that inverter must be grounded.
5. If the flip-flop is set by grounding the appropriate output terminal with an inverter, the emitter of that inverter must be grounded.
6. A 500 kc Base Load is 1 ma load at −3 volts in parallel with 680 pf. Five and 10 mc Base Loads are 1 ma load at −3 volts in parallel with 82 pf.

Typical Maximum Loading Applications

No internally-connected Capacitor-diode gate and any of the following:

1. Two 500 KC bases
2. One 500 KC base and three 5 MC bases
3. Four 5 MC bases
4. Three 1500-ohm capacitor-diode gate level inputs (as used in the 4213, 4216, and 4218)
5. Four 2200-ohm capacitor-diode gate level inputs (as used in the 4126 and 4128)
6. One 4110 diode and two 5 MC bases
7. Three 4111, 4112, or 4113 diodes

One Internally-connected Capacitor-diode gate and any of the following:

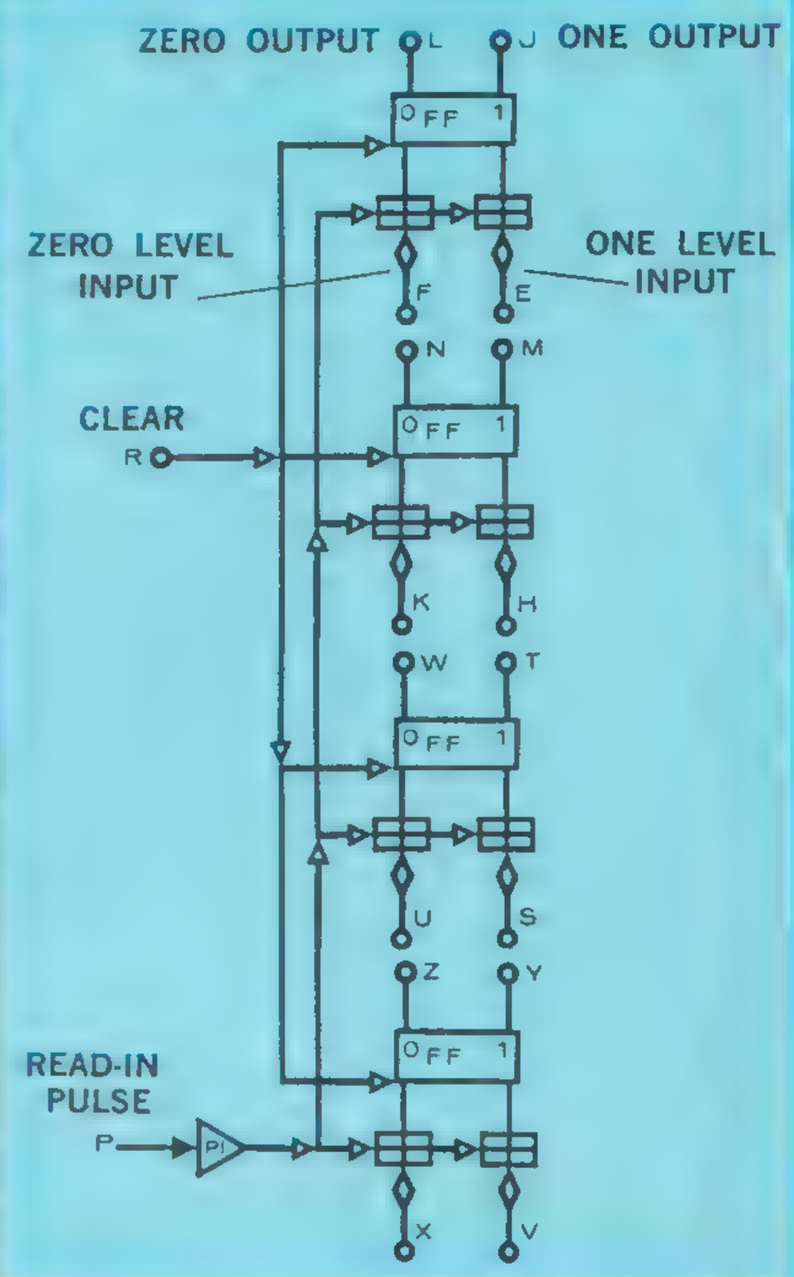
1. Two 500 KC bases
2. One 500 KC base and three 5 MC bases
3. Four 5 MC bases
4. Two 1500-ohm capacitor-diode gate level inputs (as used in the 4213, 4216, and 4218)
5. Three 2200-ohm capacitor-diode gate level inputs (as used in the 4126 and 4128)
6. One 4110 diode and two 5 MC bases
7. Three 4111, 4112, or 4113 diodes

POWER: −15 volts/100 ma; +10 volts (A)/0.65 ma; +10 volts (B)/0.5 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4218
QUADRUPLE FLIP-FLOP



The Type 4218 contains four flip-flops with associated gates for connection as a shift register or buffer register with jam transfer read-in. A pulse inverter is included for driving the capacitor-diode gates during either a read-in or a shift operation. The flip-flops may also be set or cleared by connecting the appropriate pulse gates (such as DEC Type 4113 Diode units or Type 4127 Negative Capacitor-Diode Gates) to the proper output terminals. The maximum operating frequency is 1 megacycle.

INPUT: The **Read-In Pulse Input** is a DEC Standard 0.4 microsecond Negative Pulse (1 unit of Pulse Load). The **Clear Input** is a DEC Standard 0.4 microsecond Positive Pulse (1 unit of Pulse Load per flip-flop). Clear pulses may precede read-ins by as little as 1 microsecond. **Level Inputs** for each flip-flop are complementary DEC Standard Levels (ground for assertion). There is no DC Load at these points. The transient load approximates 1 unit of Base Load.

Levels must be present at least 1 microsecond before gates are pulsed. If a conditional read-in is desired, the level may be brought to just one input gate (such as V), and the other input gate (pin X), biased off by connection to a clamped load resistor. The level at V must be at −3 volts for at least 3 microseconds to inhibit the read-in, and must be at ground for at least 1 microsecond to enable the read-in. Any number of level inputs may be inhibited with one clamped load resistor.

The flip-flops may be set or cleared by connecting a Type 4113 Diode Gate to the appropriate output terminal. The gate will then be turned on by the coincidence of two Negative Levels; or of a Negative Level and a DEC Standard 0.4 microsecond Negative Pulse. The Type 4127 Capacitor-Diode Gate may also be used for this purpose.

OUTPUT: Each flip-flop output provides Standard DEC Levels of 0 and −3 volts. The outputs are unbuffered and the delay is, therefore, short compared with the 0.4 microsecond pulse width. Typical delay is 0.05 microsecond. When the flip-flop is to be sampled and changed at the same pulse time, provision must be made for logical delay. This delay may be provided by the use of capacitor-diode gates (such as those used in the Types 4125 through 4129).

Output Loading

1. Each output may drive ±4 ma, 1500 pf and a 1500-ohm capacitor-diode gate. Such gates are included in the type 4213, 4216 and 4218.
2. Loading of the ZERO and ONE outputs is independent.
3. An output cannot be used to gate emitters directly.
4. When an output is used to drive an inverter base, the emitter of that inverter must be grounded.
5. If the flip-flop is set by grounding the appropriate output terminal with an inverter, the emitter of that inverter must be grounded.
6. A 500 kc Base Load is 1 ma load at −3 volts in parallel with 680 pf. Five and 10 mc Base Loads are 1 ma load at −3 volts in parallel with 82 pf.

Typical Maximum Loading Applications

1. Two 500 kc bases and one 1500-ohm capacitor-diode gate.
2. One 500 kc base, three 5 mc bases and one 1500-ohm capacitor-diode gate.
3. Four 5 mc bases and one 1500-ohm capacitor-diode gate.
4. Three 1500-ohm capacitor-diode gate level inputs (as used in the 4218).
5. Four 2200-ohm capacitor-diode gate level inputs (as used in the 4126 and 4128).
6. One 4110 diode two 5 mc bases and one 1500-ohm capacitor-diode gate.
7. Three 4111, 4112, or 4113 diodes and one 1500-ohm capacitor-diode gate.

POWER: −15 volts/98 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

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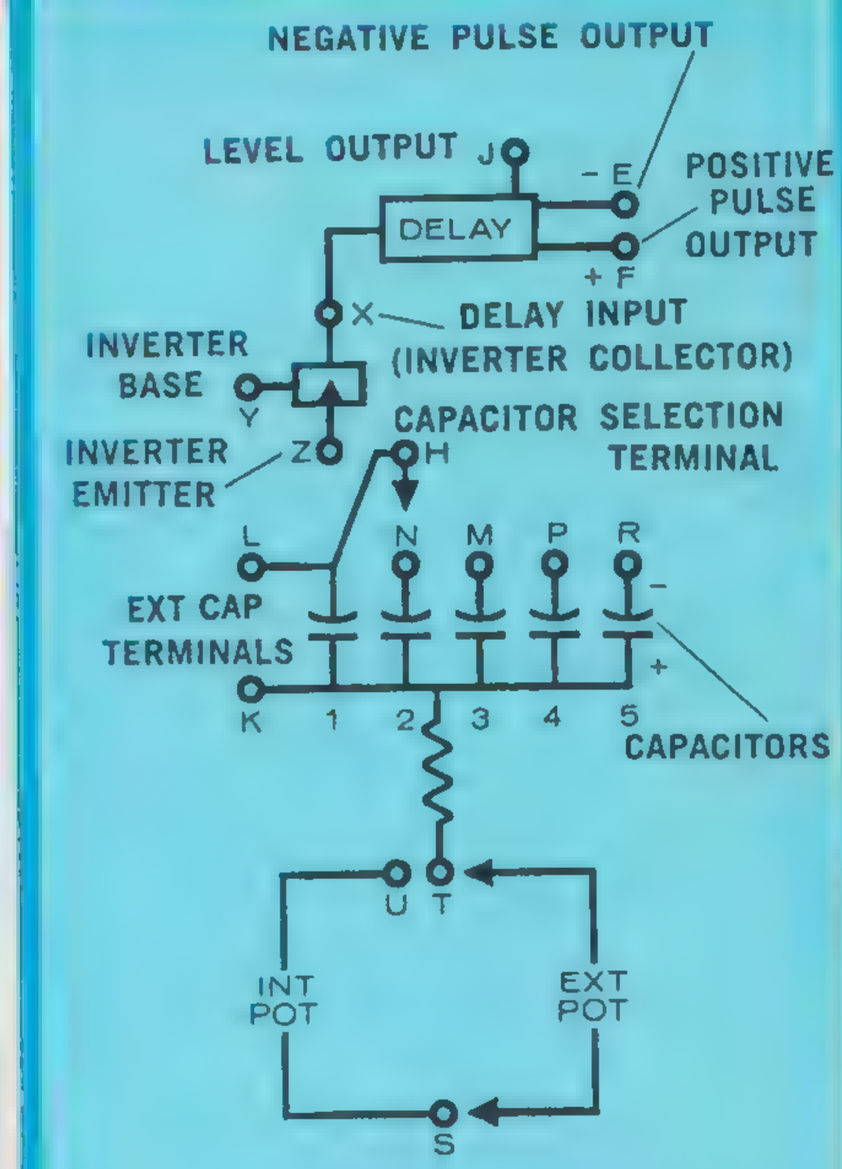
digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4301
DELAY (ONE SHOT)



The Type 4301 delay unit is a mono-stable multivibrator. When the input terminal is grounded through an inverter the level output terminal will switch from its normal ground level to —3 volts for a predetermined, but adjustable, period of time and then back to ground. A pulse transformer generates a DEC Standard 0.4 microsecond Pulse at the pulse output during the final transition. The pulse transformer has both positive and negative terminals so that either polarity pulse may be obtained. Typical output and input wave forms are shown in Figure 1.

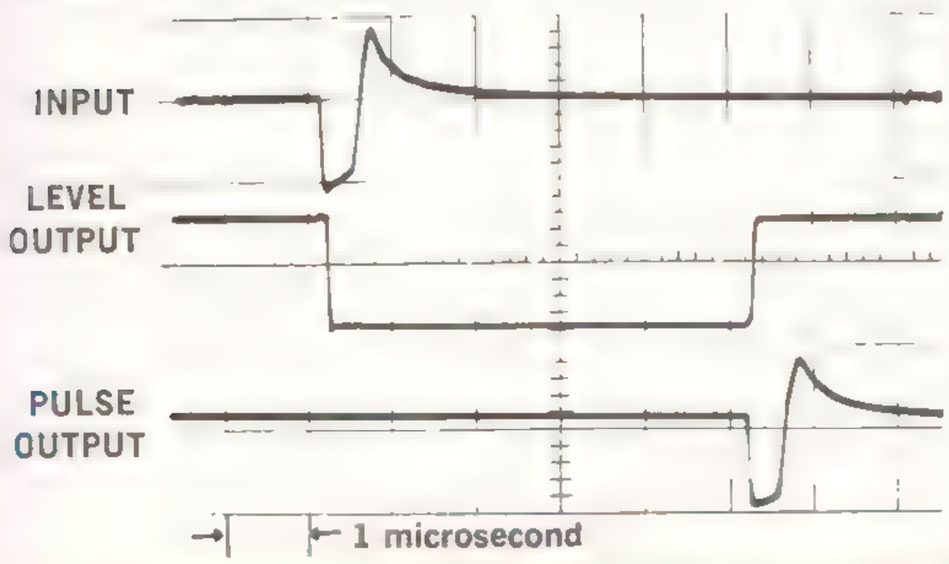


Figure 1 — INPUT AND OUTPUT VS. TIME

The delay duration is variable from 2.5 microseconds to 0.2 second. The five internal capacitors determine the coarse range. Capacitor 1 is internally connected to provide delays at the range of 2.5 to 25 microseconds. Connecting the capacitor selection terminal to capacitors 2, 3, 4 or 5 increases the delay in approximate factors of 10, with capacitor 5 representing the maximum delay range available with an internal capacitor. By installing an additional external capacitor to the indicated terminals, the delay range may be further extended.

An internal 15,500 ohm potentiometer may be used for fine adjustment if pin U is connected to pin T. An external potentiometer may also be used if desired. Circuit recovery time is equal to 20% of the maximum delay available on the coarse range being used. A 20% change in power supply voltage will change the delay less than 1%. Delay jitter (due to power supply ripple) is less than 0.5%, peak to peak.

INPUT: The input to the delay is a DEC Standard 0.4 microsecond Negative Pulse on the base of a pulse gate, such as the one included in the delay

module. The base of the built-in pulse gate represents 1 unit of Pulse Load; the emitter represents 1 unit of Pulsed Emitter Load. If more logical inputs are desired, they can be provided by connecting other pulse gate collectors to the collector of the built-in pulse gate. Mixing of several pulses can also be accomplished by using half of a DEC Diode Type 4110 with DEC Standard 0.4 microsecond Negative Pulses are applied to the diodes and the collector tied to the collector of the built-in pulse gate.

OUTPUT: LEVEL — When the input is pulsed, a negative DEC Standard Level occurs for the duration of the delay interval. This level is capable of simultaneously driving: (a) 12 units of Base Load; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time. PULSE — At the end of the delay interval, a DEC Standard 0.4 microsecond Pulse occurs. The output pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. This signal can drive 8 units of Pulse Load.

POWER: —15 volts/70 ma; +10 volts (A)/1.1 ma; +10 volts (B)/0 ma.

TYPICAL APPLICATIONS

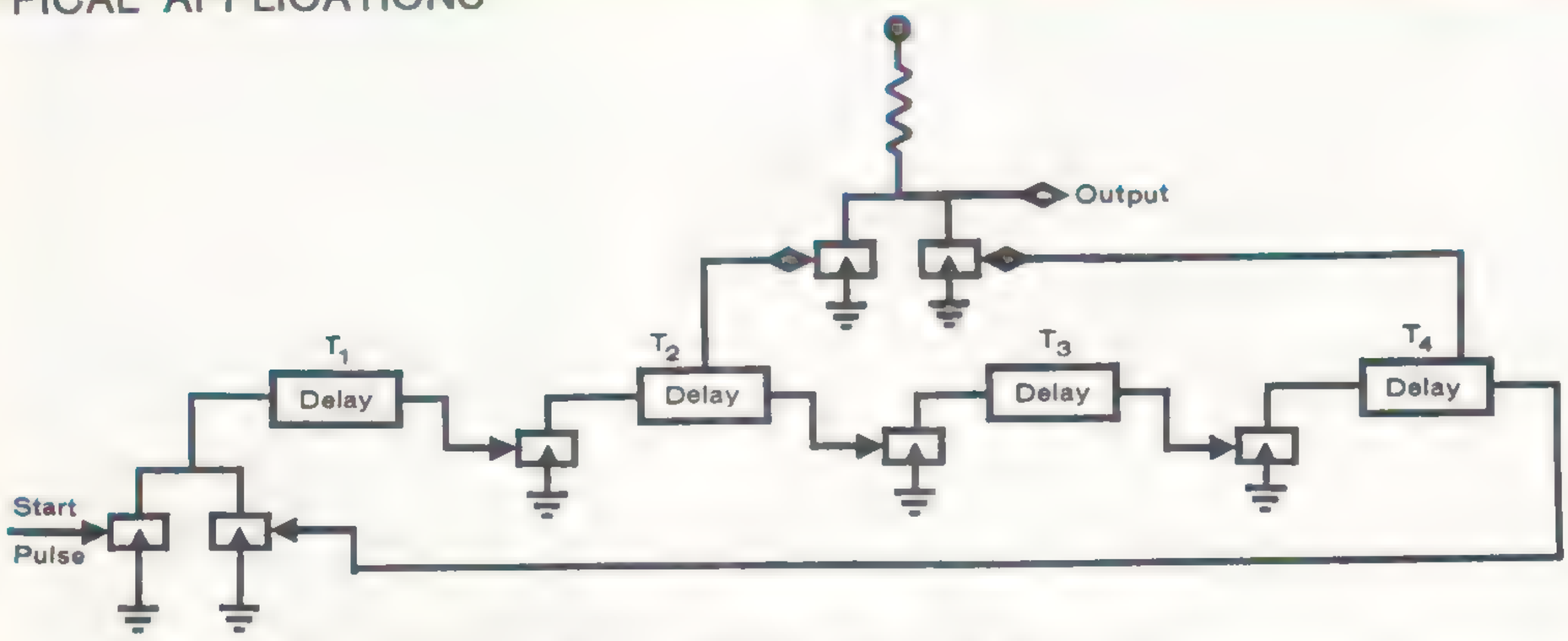


Figure 2 — WAVE FORM GENERATOR

Delay units are particularly useful in generating signals of arbitrary width. The network of delays in Figure 2 will produce the wave form in Figure 3.

The 1st and 3rd delays, not being connected to the output inverters, will produce no signal during their delay period. The 2nd and 4th, however, will produce a ground output for the duration of their respective delays. The wave form is periodic, since the pulse output from T_4 goes back to T_1. Due to delay recovery time, more than one delay unit is necessary to recycle the pulse.

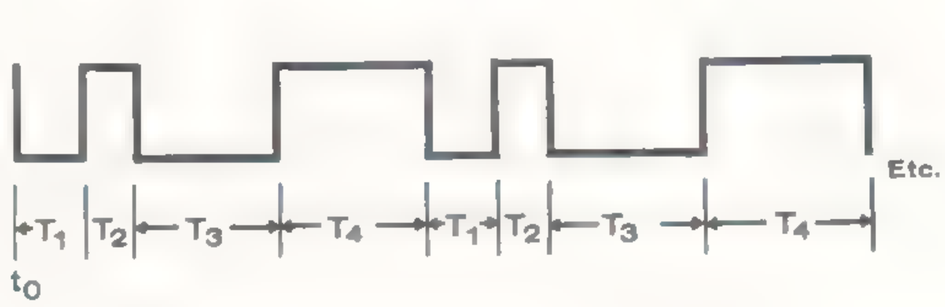


Figure 3 — OUTPUT WAVE FORM

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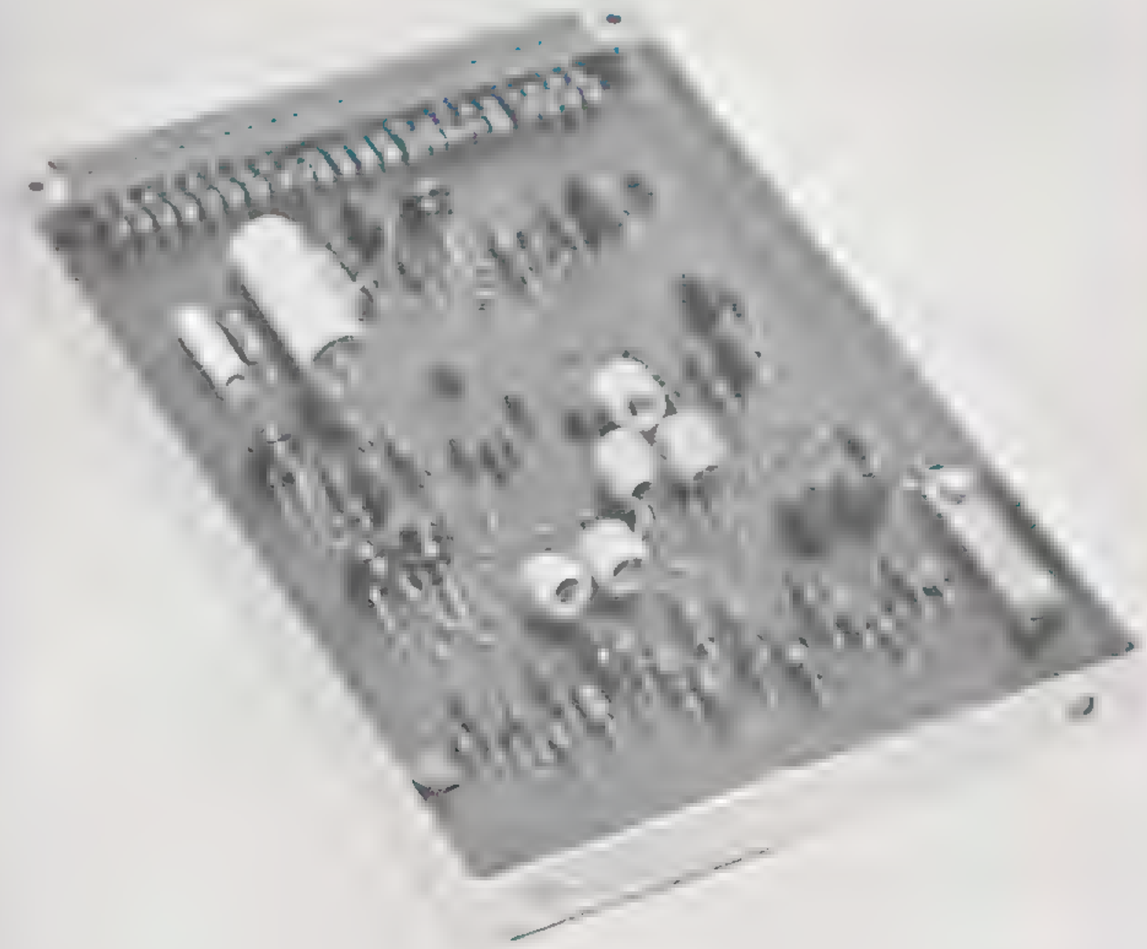
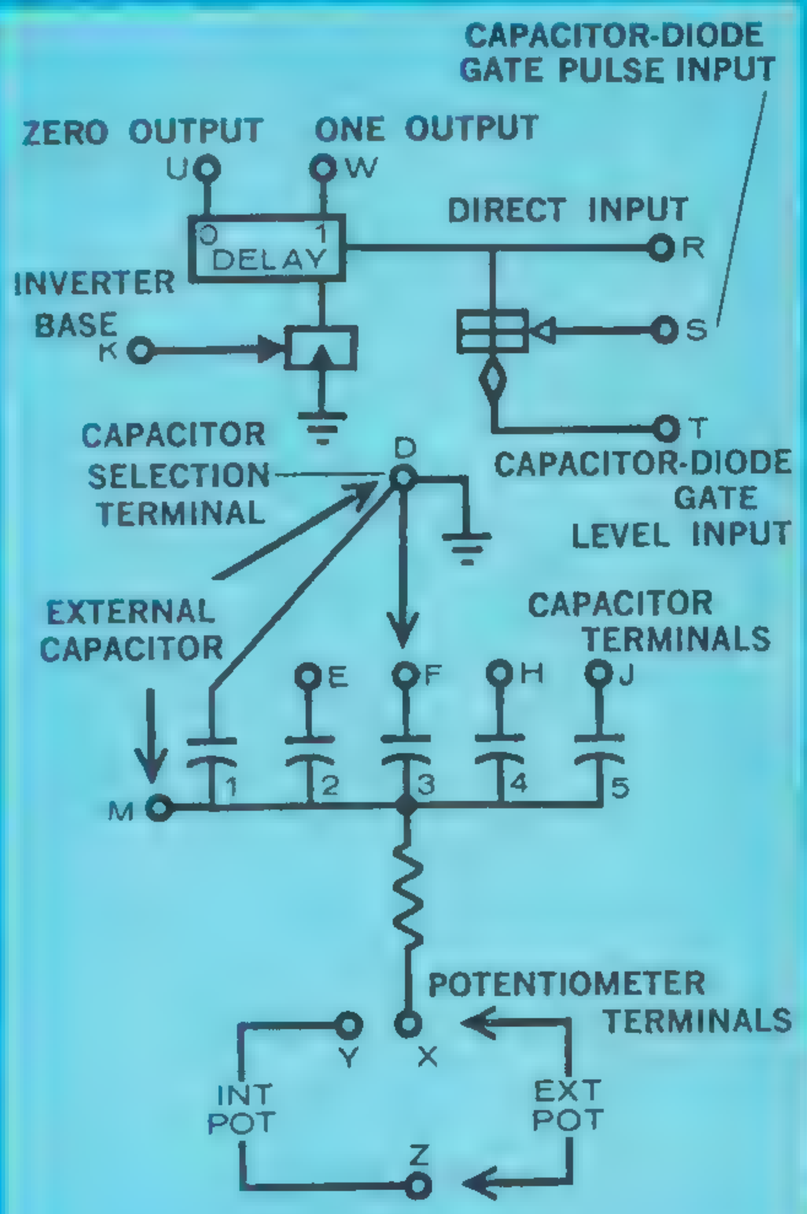
4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4303
INTEGRATING
SINGLE SHOT





The Type 4303 Integrating Single Shot contains a stable single shot multivibrator which generates a flip-flop type output during the delay. The delay intervals are variable in four overlapping ranges from 3.4 microseconds to 0.9 second. (Longer delays may be obtained with an external capacitor.) The unit has an internal potentiometer for fine control and provisions for an external potentiometer, if desired. The unit may be repeatedly triggered, and the delay will continue for the specified duration after the final triggering. If a negative level is applied to the base of the input inverter, the delay will begin when the level is applied and remain for the specified duration after the level has been removed. The unit has no recovery time. The delay time will change less than ±2% for a 20% change in supply voltage, and the peak-to-peak jitter is less than 1.4%. Controls: Capacitor 1 is internally connected to the capacitor selection terminal to give the shortest delay range. Delay ranges may be increased by approximate factors of 10 by connecting capacitors 2, 3, 4 or 5 to the capacitor selection terminal. (Capacitor 5 gives the largest delay range, up to 0.9 second.) For longer delays an external capacitor may be connected between the external capacitor terminal and the capacitor selection terminal.

To use the internal potentiometer for fine control, pin X should be jumpered to pin Y. If an external potentiometer is desired, it should be placed between pin X and pin Z.

INPUT: Inverter — The delay may be triggered by a DEC Standard 0.4 microsecond Negative Pulse or a Negative Level applied to the base of the inverter attached to the delay. The DC load at this point is 1 unit Base Load. The transient load presented to a pulse input is 1 unit Pulse Load. **Capacitor-Diode Gate** — The 1500-ohm capacitor-diode gate attached to the delay has pulse and conditioning level inputs. The pulse inputs should be a DEC Standard Positive Pulse or Positive Going Level change. The load presented is 1 unit Pulse Load. The conditioning level input is ground for assertion and should be present at least 3 microseconds before the unit is pulsed. There is no DC load at this point. The transient load approximates 1 unit of Base Load. **Direct Input** — The direct input (pin R) may be connected to the

output of a positive capacitor-diode gate. Load is 1 unit Pulse Load.

OUTPUT: The Type 4303 has flip-flop type outputs available. The ONE output will produce −3 volts during a delay period and ground volts otherwise. The ZERO output will produce ground volts during a delay and −3 volts otherwise. Each output may drive 4 units of Base Load, 0.4 unit of DC Emitter Load; and two capacitor-diode gate level inputs. An output cannot be used to gate emitters directly. When an output is used to drive an inverter base, the emitter of that inverter must be grounded.

POWER: −15 volts/70 ma; +10 volts (A)/2.9 ma; +10 volts (B)/3.2 ma.

TYPICAL APPLICATION

GATABLE PULSE SOURCE

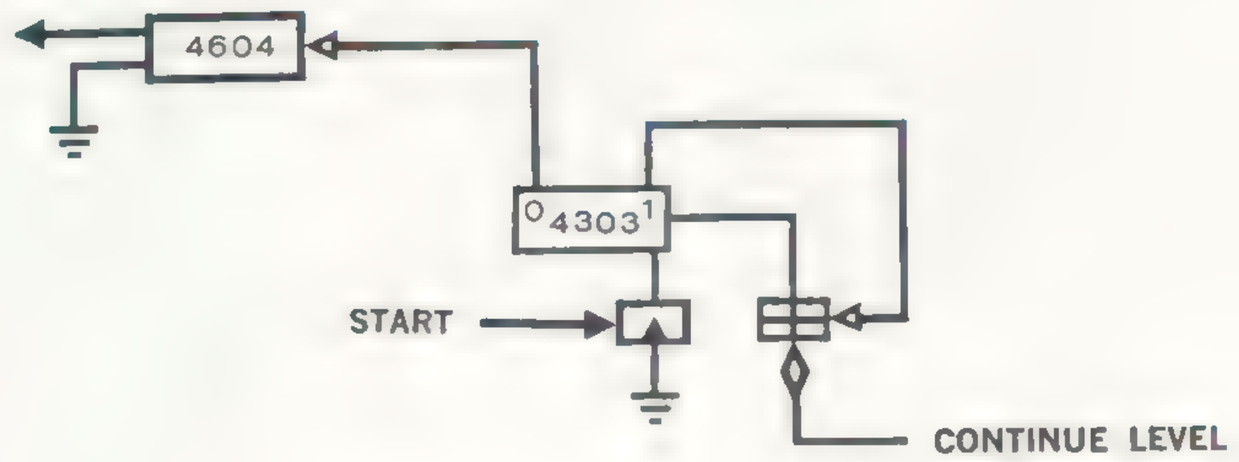


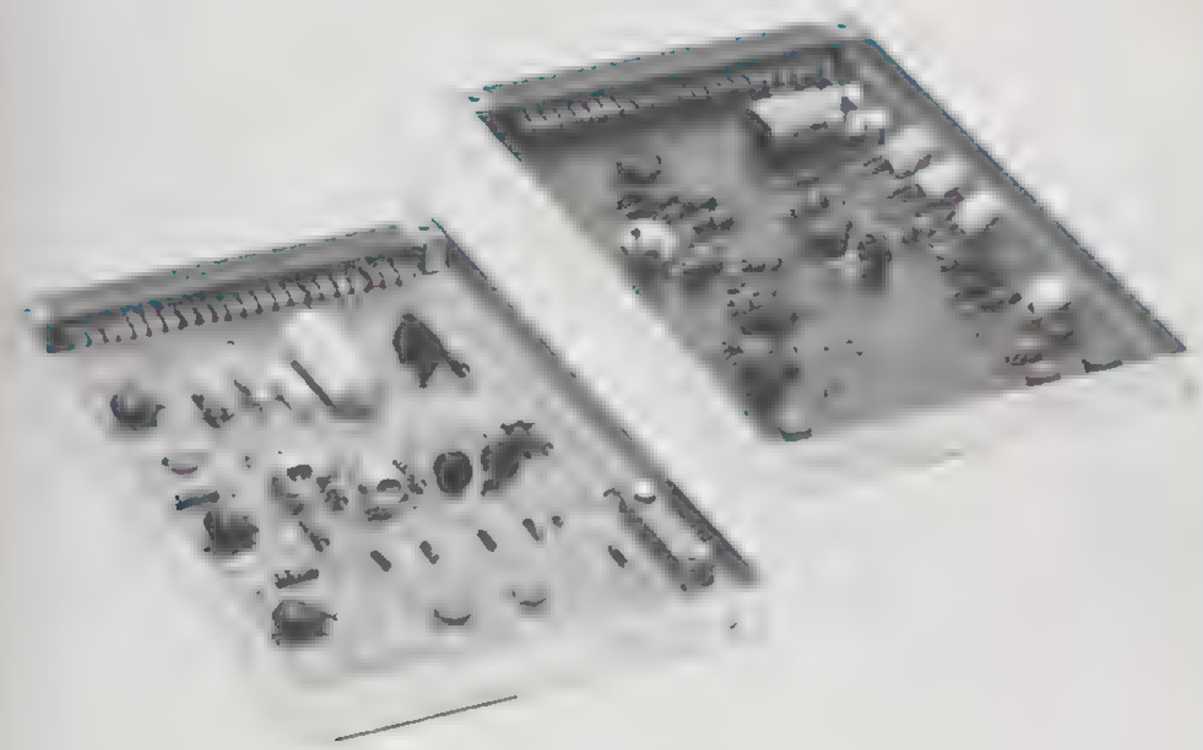
Figure 1 – GATABLE PULSE SOURCE

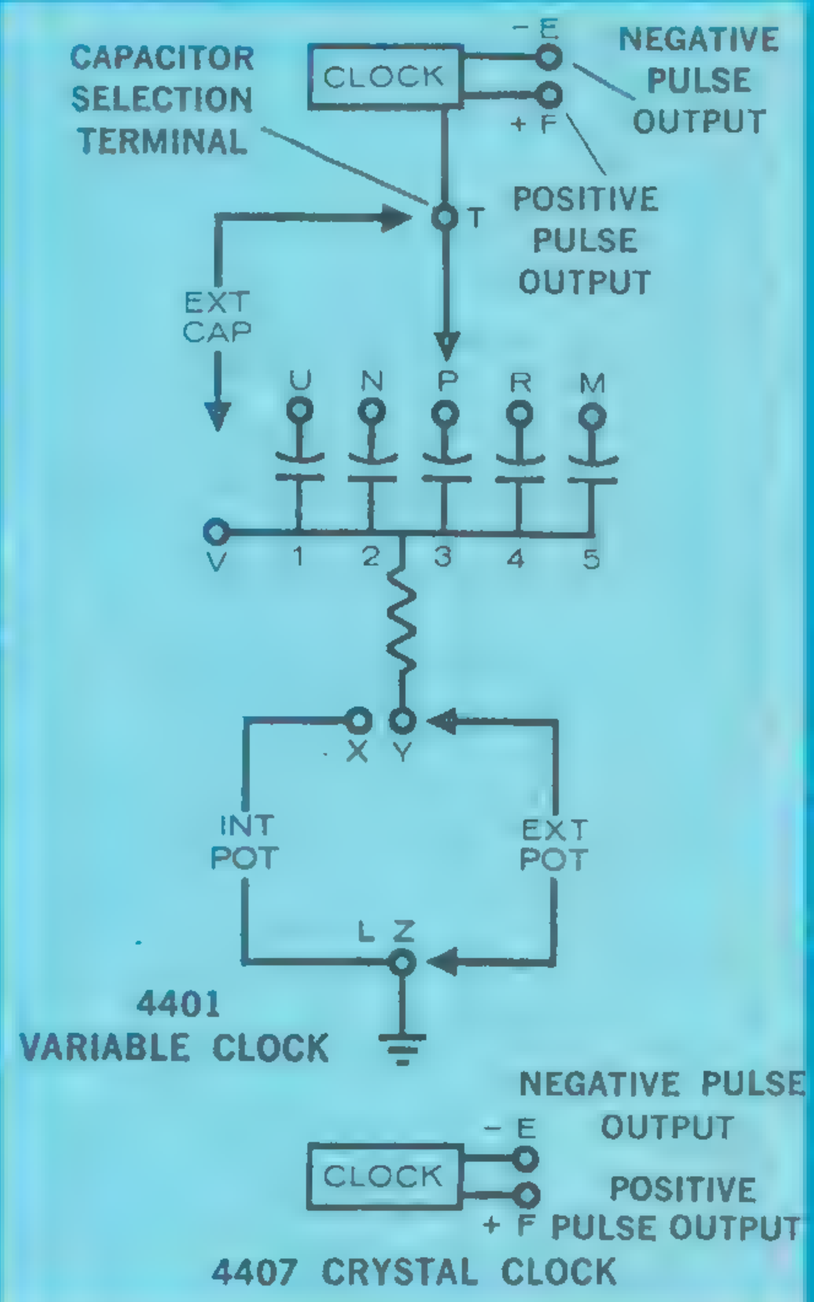
A typical application for the Type 4303 is in making a gatable pulse source such as shown in Figure 1. The delay is turned on by a negative pulse on the inverter base. When the delay is completed, the unit will be retriggered by the feedback loop from the ONE output to the capacitor-diode gate input. This retriggering process will continue as long as the continue level is at ground.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4401-4407
CLOCKS





The DEC Variable Clock Type 4401 produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies available. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the Type 4407 Crystal Clock, which contains a single—frequency crystal oscillator, may be used.

The frequency of the Type 4401 is variable from 5 cycles/second to 500 kilocycles/second. The capacitor connection determines the frequency range and a 20,000 ohm potentiometer provides fine control. Capacitor 1 gives a range of approximately 50 to 500 KC; capacitor 2, 5 to 50 KC; capacitor 3, 500 to 5000 cycles; capacitor 4, 50 to 500 cycles; and capacitor 5, 5 to 50 cycles. An external capacitor may be used for lower frequencies. If terminals X and Y are connected together, the internal potentiometer will provide the fine control. An external potentiometer can be connected between terminals Y and Z.

The Type 4407 contains a series resonant crystal oscillator circuit and two pulse shaping buffer amplifiers which produce DEC Standard 0.4 microsecond Pulses. The frequency, specified by the customer, may be between 5 and 500 kilocycles. The frequency is stamped on the crystal in the plug-in unit.

OUTPUT: The output is a DEC Standard 0.4 microsecond Pulse which occurs at the preselected frequency. The pulse may be made positive by grounding the negative output terminals; it may be made negative by grounding the positive output terminal. The signal can drive 8 units of Pulse Load. **Crystal Clock:** The stability of the crystal clock's output frequency is 0.01% between −20 and +55°C. **Variable Clock:** A 20% change in the power supply voltage on the Type 4401 Clock will change the prf less than 1% and its pulse-to-pulse jitter is less than 0.2%.

POWER: Type 4401: −15 volts/45 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. **Type 4407:** −15 volts/81 ma; +10volts (A)/5 ma; +10 volts (B)/4.5 ma.

SYNCHRONIZATION

It is possible to synchronize the output of a variable clock to the outputs of other clocks, generators or external signals. The frequency of the synchronizing signal may be the same, a harmonic or a subharmonic. (Synchronization to a subharmonic results in an average period standardization only. The time from one pulse to the next may vary since only one clock pulse in several is actually triggered by the incoming signals.) The phase drift of clocks operating on the same frequency is eliminated by synchronizing the clocks.

A typical application is the synchronization of DEC Variable Clocks to a DEC Crystal Clock to obtain the desirable features of both the crystal and variable clocks. Provide the DEC Crystal Clock with a simple resistive attenuator whose output (capacity coupled) can be used as the standardization signal for the variable clock used in the system. Synchronization signal amplitudes of from one-tenth to several tenths of a volt peak-to-peak are most satisfactory. The signal of the crystal clock is applied to the capacitor of the variable clock at pin V. (This Signal must be applied through a blocking capacitor with an impedance on the order of 1000 ohms at the operating frequency.)

As in all synchronizing schemes, the smaller the synchronization signal, the less reliable is the lock and the more tendency there is over a long period of time for small variations in the natural free running frequency of the multivibrator to cause the locking action to become intermittent or fail. There may be cases, however, in which it is desirable to be able to synchronize the variable clock in a special ratio to the synchronizing frequency for a short period of time (e.g. 2/3, 4/3, 5/7) to perform a single experiment, and in these cases the locking reliability for the weak inputs required will be found to be satisfactory.

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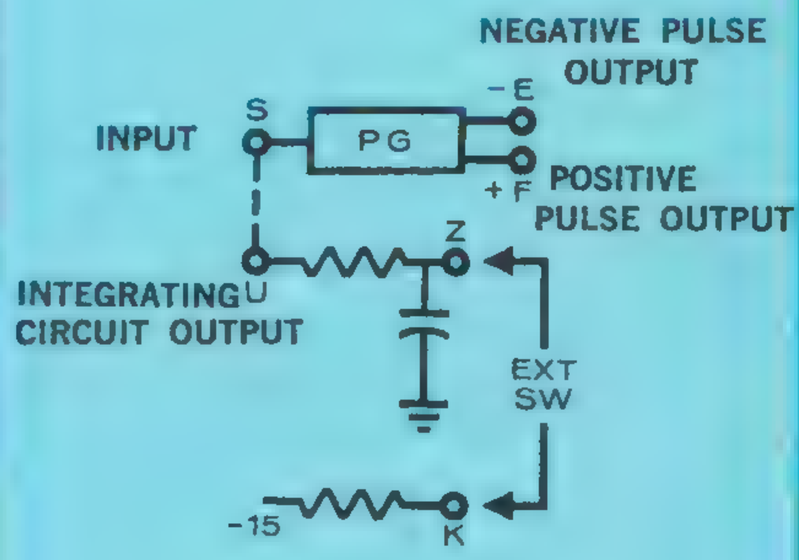
4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4410
PULSE GENERATOR



The Type 4410 converts external signals to DEC Standard Pulses. A Schmitt circuit produces a DEC Standard 0.4 microsecond Pulse at the output every time the input voltage goes more negative than −2.5 volts after having been more positive than −1.0 volts. This unit also contains an integrating circuit to filter contact bounce when a switch or relay is used to generate the pulse. The time constant of the integrating circuit is 12 milliseconds.

INPUT: Pulse Generator — The input is a DC connection, thereby eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. The input signal should stay between +10 volts and −10 volts. The input can come from an external source or from the output of the integrating circuit. **Integrating Circuit** — The two inputs to this circuit come from switch or relay contacts.

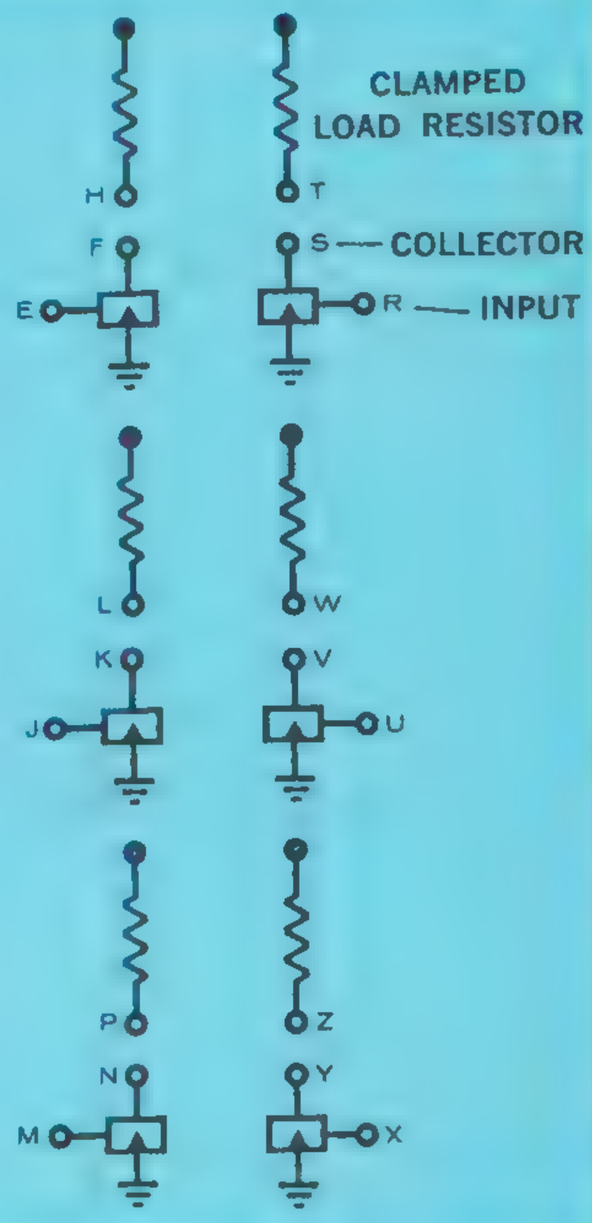
OUTPUT: Pulse Generator — The output is a DEC Standard 0.4 microsecond Pulse. The pulse will be negative if the positive terminal is grounded; it will be positive if the negative terminal is grounded. The maximum prf is 500 KC. This signal can drive 8 units of Pulse Load.

POWER: −15 volts/68 ma; +10 volts (A)/5 ma; +10 volts (B)/5 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4504
7090 TO DEC CONVERTER



The Type 4504 contains 6 circuits that convert voltage mode IBM 7090 signals to DEC signals. Each circuit consists of a grounded emitter inverter with a bias network between its input and the base of the inverter. When the input is more positive than +4 volts the inverter will be cut off, and the output will be at −3 volts if a clamped load is connected to the output. When the input is more negative than +2 volts the inverter will be saturated and the output will be ground. Six clamped loads are included.

INPUT: For input voltages between +4 and +15 the inverter is cut off, and the input load is equivalent to a 6000 ohm resistor returned to −12 volts. For inputs less than +2 volts, the inverter is saturated and the input load is equivalent to 12,000 ohms returned to −12 volts.

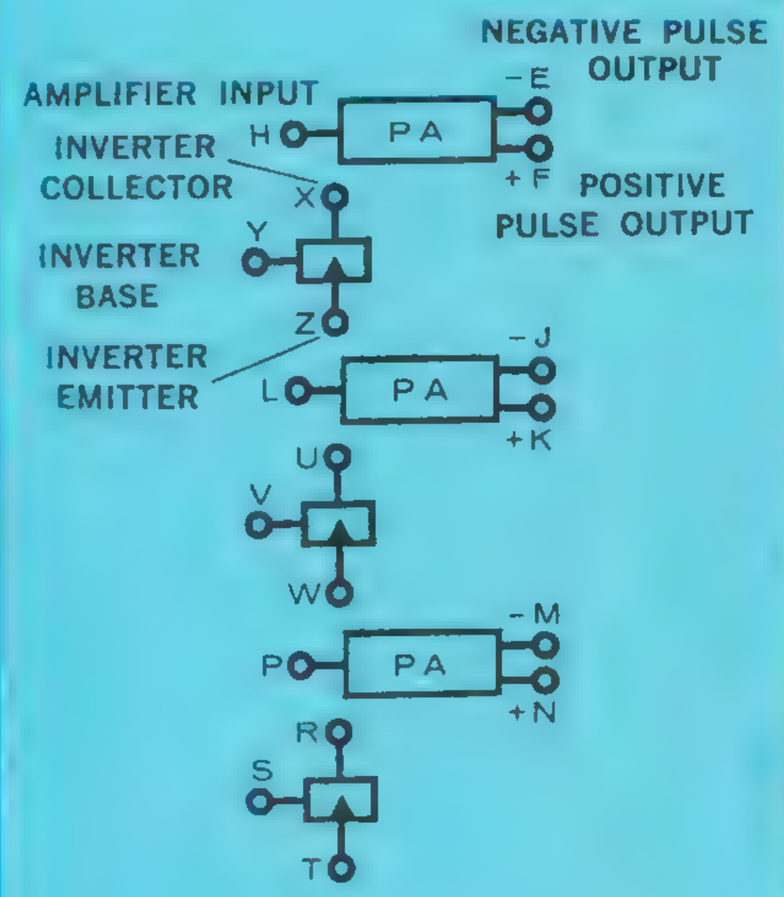
OUTPUT: When driving a clamped load the output rise delay will be less than 0.3 microseconds and the total transition time will be less than 0.5 microseconds. The fall delay will be less than 0.2 microseconds and the total transition time less than 0.3 microseconds. The output is a standard 500 KC inverter similar to the 4105 and 4106, and the same loading rules apply.

POWER: −15 volts/120 ma; +10 volts (A)/1.2 ma; +10 volts (B)/1.2 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4603
PULSE AMPLIFIER



The Type 4603 contains three pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Three standard inverters are included for gating the input. The inverters are similar to those in the DEC Inverter Type 4105. Delay through the pulse amplifier is approximately 0.05 microsecond. Input pulses may occur at any frequency up to 500 kilocycles. The DEC Diode Type 4110 may be used in conjunction with the pulse amplifier for conveniently mixing pulses from several sources.

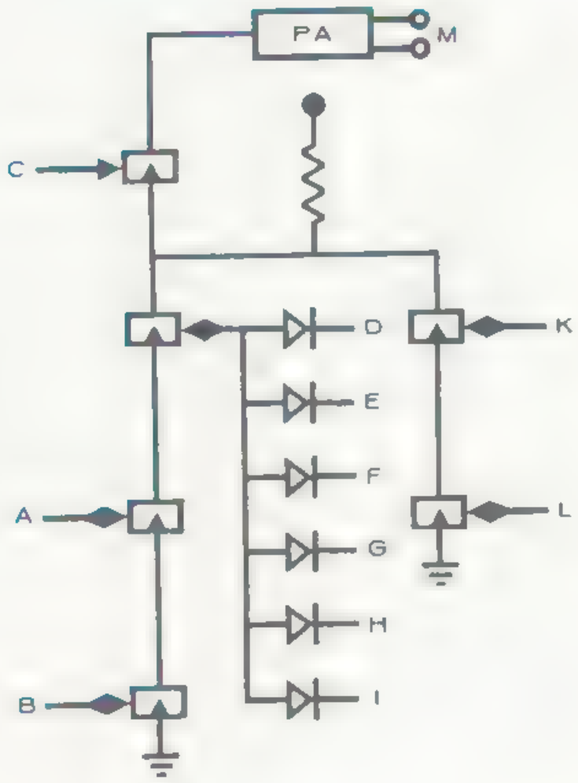
INPUT: The input must come from the collector of one or more pulse gates. The signal on the base of the pulse gate is normally a DEC Standard 0.4 microsecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 0.2 microsecond and width greater than 0.3 microsecond may be used. Input pulses of less than −0.5 volts will not generate an output pulse. Several remote pulse gate collectors may be connected together to mix pulse sources. A DEC 70 nanosecond Negative Pulse may be used as an input, providing a feedback loop is used (as shown in Figure 2 of the applications section) and high speed pulse gates such as those in Type 1105 are used as the input and feedback pulse gates.

OUTPUT: The output is a DEC Standard 2.5 volt, 0.4 microsecond Pulse which occurs at the output every time the input signal meets the input requirement. The pulse will be negative if the positive output is grounded; it will be positive if the negative output is grounded. Each output is capable of driving 16 units of Pulse Load.

POWER: +10 volts (A)/0.3 ma; +10 volts (B)/0.2 ma; −15 volts/110 ma.

TYPICAL APPLICATION

LOGICAL GATING



$$M = C[A \cdot B(D + E + F + G + H + I) + K \cdot L]$$

Figure 1 — PULSE AMPLIFIER GATING

When a large amount of gating must be performed in several places, it is often economical to perform this gating at the input of a pulse amplifier. The output pulse may then go directly to flip-flops and other pulsed units with the same results as if the gating had been performed at each unit being pulsed. Figure 1 illustrates a typical gated pulse amplifier.

For more information on mixed systems, see "Integrating Different Series of DEC Modules."

PULSE STANDARDIZATION

DEC Pulse Amplifiers are also useful in providing compatibility between the different series of DEC Modules. Since the modules are designed with compatibility in mind, the only differences between frequency lines are in the timing characteristics. In particular, pulses in the 10 megacycle line have a duration of 40 nanoseconds; in the 5 megacycle line, 70 nanoseconds; and in the 500 kilocycle line, 400 nanoseconds (0.4 microseconds).

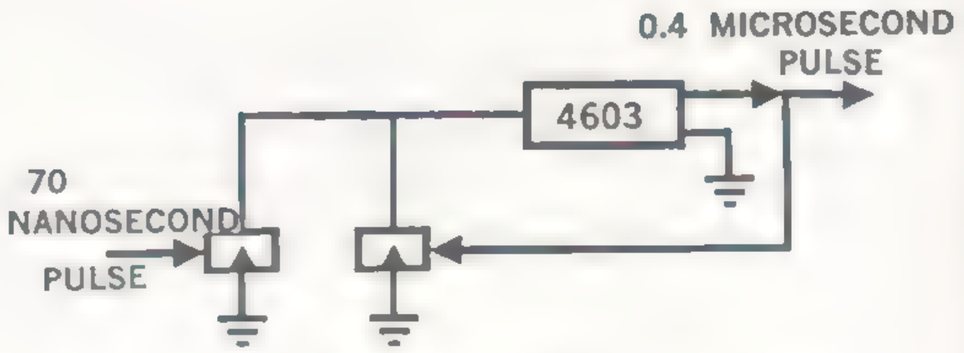


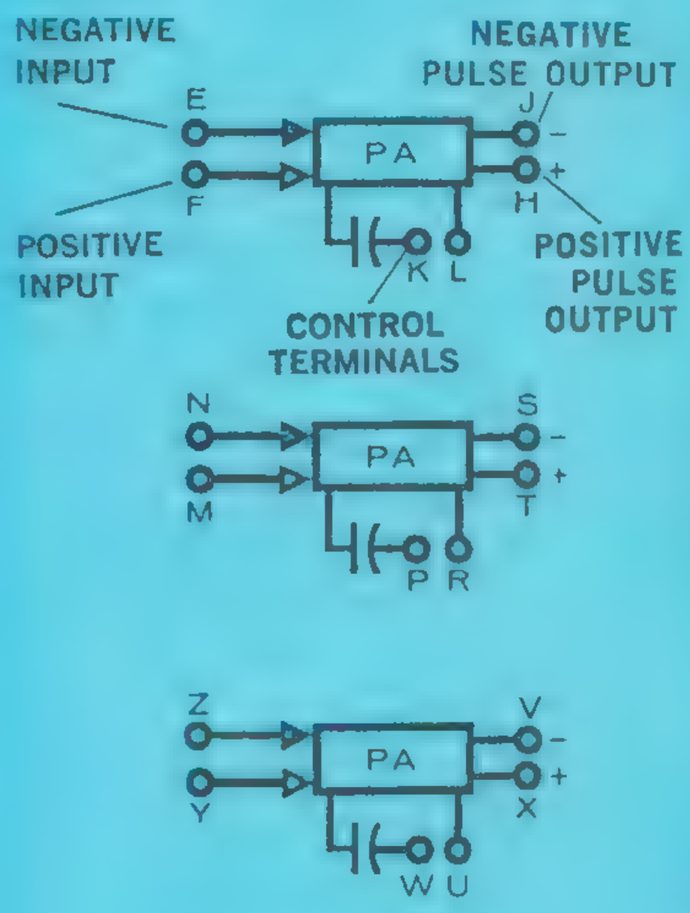
Figure 2 — PULSE STRETCHING

To produce an 0.4 microsecond pulse from a 70 nanosecond pulse, either a Type 4603 or a Type 4604 pulse amplifier may be used. The Type 4604 requires no additional gating to perform this function; however, the Type 4603 requires a feedback loop which reduces the output driving ability somewhat.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4604
PULSE AMPLIFIER
1 MEGACYCLE



Three pulse amplifiers perform power amplification and standardize pulses to any width between 0.4 and 1 microsecond. Each pulse amplifier has two control pins for determining the output pulse width. When these control terminals are left open circuited, the unit will amplify all input signals to DEC Standard 0.4 microsecond Pulses at pulse repetition frequencies up to 1 megacycle. When the control terminals are shorted together, the unit will standardize inputs to produce 1 microsecond pulses at any rate up to 330 kilocycles. Any pulse width between 0.4 and 1 microsecond is obtainable by connection of an appropriate external capacitor between the two control terminals. The maximum pulse repetition frequency varies with the pulse width from 330 kilocycles to 1 megacycle.

INPUT Negative: The negative input terminal will accept negative going signals with a swing of 2.5 to 4 volts, a fall time less than 0.5 microsecond and a width greater than 60 nanoseconds. The load presented by the input is 1 unit of Pulse Load.

INPUT Positive: The positive input terminal will accept positive going signals with a swing of 2.5 to 4 volts, a rise time less than 0.5 microsecond and a width greater than 60 nanoseconds. The load presented by the input is 1 unit of Pulse Load.

OUTPUT: The output is a 2.5 volt pulse which occurs every time the input signal meets the input requirement. For a negative output pulse, ground the positive terminal. For a positive output pulse, ground the negative terminal. Each output is capable of driving 16 units of Pulse Load.

POWER: −15 volts/180 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

TYPICAL APPLICATION

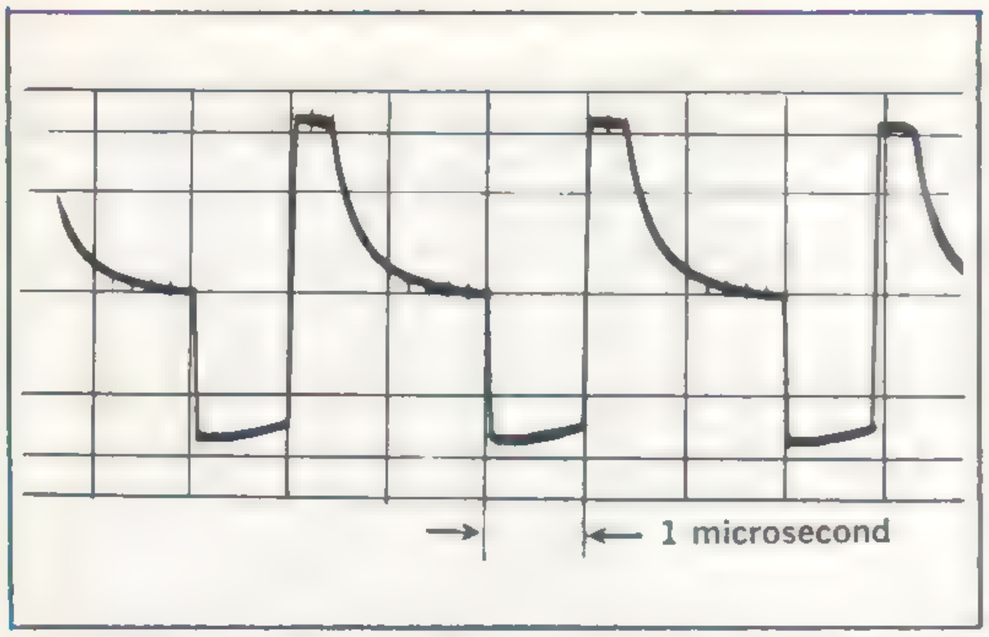


Figure 1 — DEC 1 MICROSECOND NEGATIVE PULSES

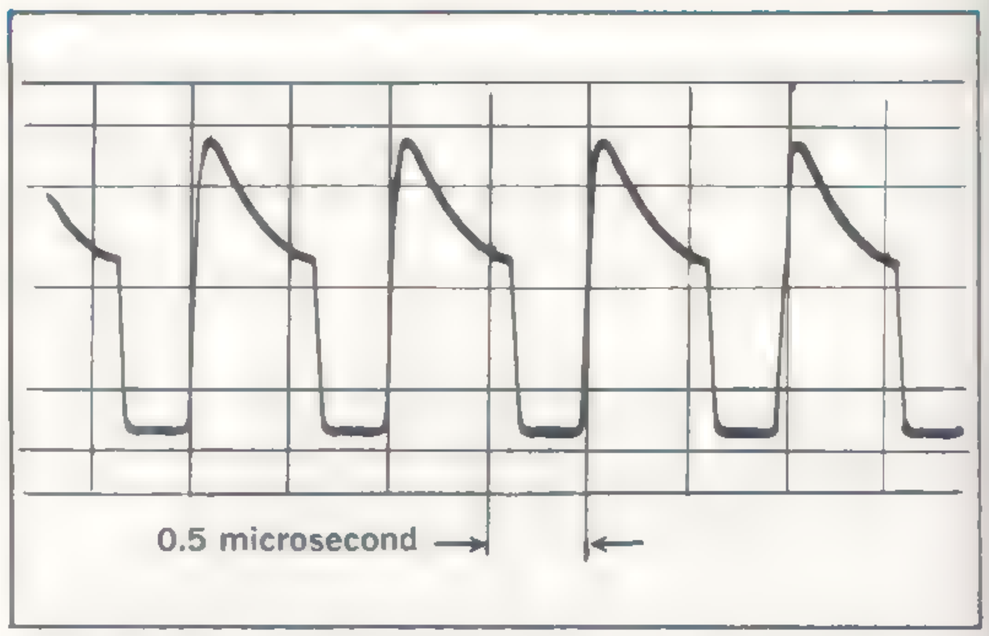


Figure 2 — DEC STANDARD 0.4 MICROSECOND NEGATIVE PULSES

The Type 4604 is particularly useful in converting level changes or DEC Standard 70 nanosecond Pulses into DEC Standard 0.4 microsecond Pulses. Changing levels from the outputs of any DEC Flip-flop or Delay unit may be applied directly to the pulse amplifier inputs. DEC Standard 70 nanosecond Pulses (as used in the 100 and 1000 series of 5 megacycle modules) may also be applied directly to the pulse amplifier input. No special connections are required for converting these signals to DEC Standard 0.4 microsecond Pulses.

By shorting together the two control pins, the pulse amplifier may be used to produce 1 microsecond pulses. These are particularly useful in clearing DEC Type 4215 Flip-flops.

Since the Type 4604 can produce pulses with any width between 0.4 and 1 microsecond, this unit is particularly useful in driving external circuitry. The pulse amplitude, normally 2.5 volts, may be increased by connecting pulse amplifier outputs in series.

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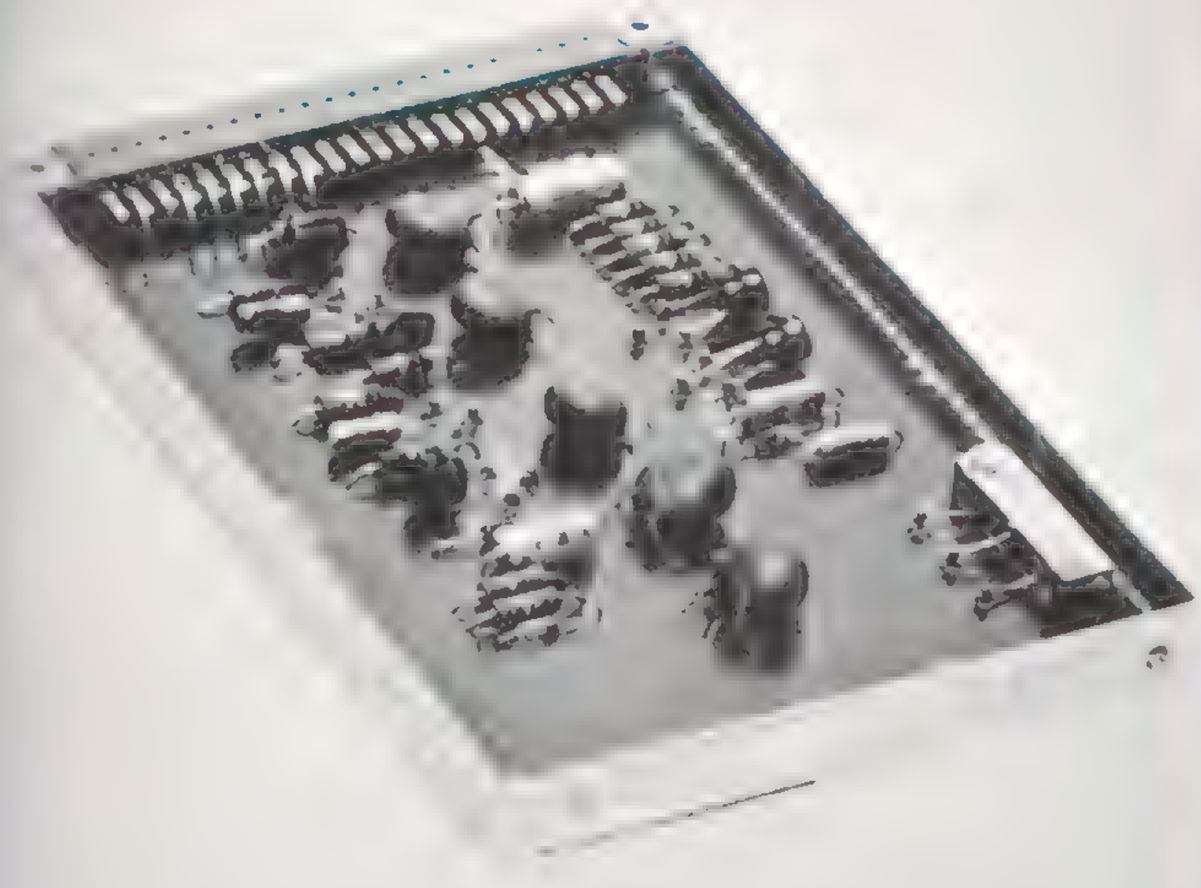
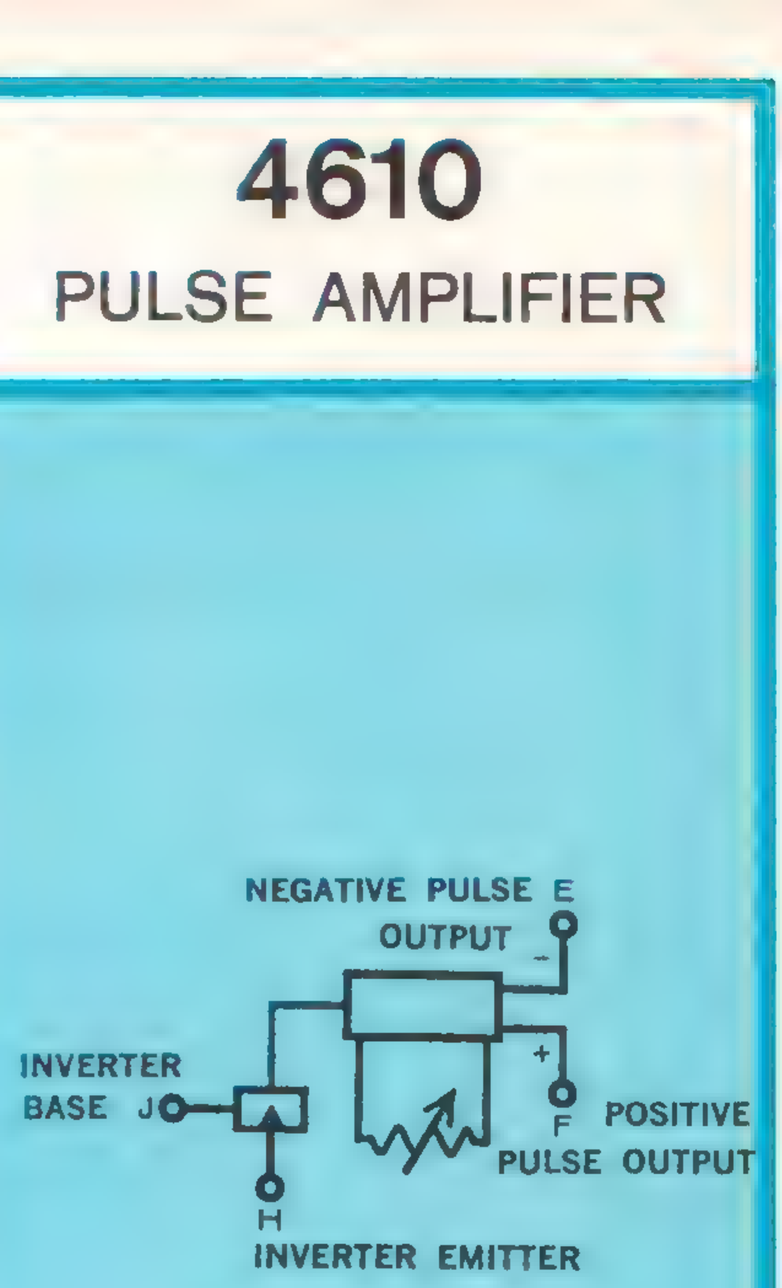
4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4610
PULSE AMPLIFIER





This pulse amplifier delivers 2 to 3 microsecond pulses with amplitudes variable from 2 to 34 volts into 100 ohms. The input is through an inverter gate. A 0.4 microsecond input produces a 2 microsecond pulse, and a 1.0 microsecond input produces a 3 microsecond pulse. The maximum prf is 1 kilocycle. Delay is less than 0.5 microsecond, and the rise and fall times are less than .25 microsecond. Controls: a potentiometer varies the output amplitude.

INPUT: The base input is DEC Standard 0.4 microsecond Negative Pulses or equivalent, which represents 1 unit of Pulse Load. The emitter represents 1 unit of DC Emitter Load.

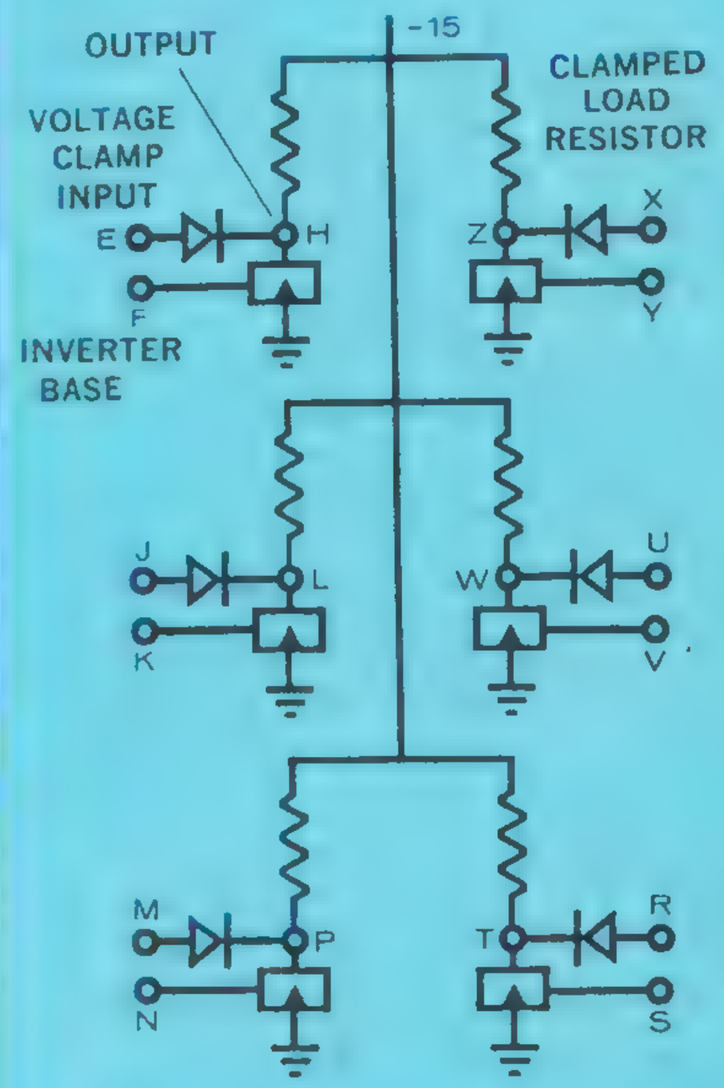
OUTPUT: The output will be negative if the positive output terminal is grounded, and it will be positive if the negative output terminal is grounded.

POWER: −15 volts/30 ma; +10 volts (A)/1 ma; +10 volts (B)/0 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4667
NEGATIVE LEVEL AMPLIFIER



Six grounded emitter inverters amplify DEC Standard Levels. The output signals are ground and a negative voltage that is determined by clamping diodes. These clamping diodes are connected to each inverter collector and brought out to the plug to be returned to an external voltage between ground and −15 volts.

INPUT: The base inputs are driven by DEC Standard Levels or equivalent (1 unit of Base Load).

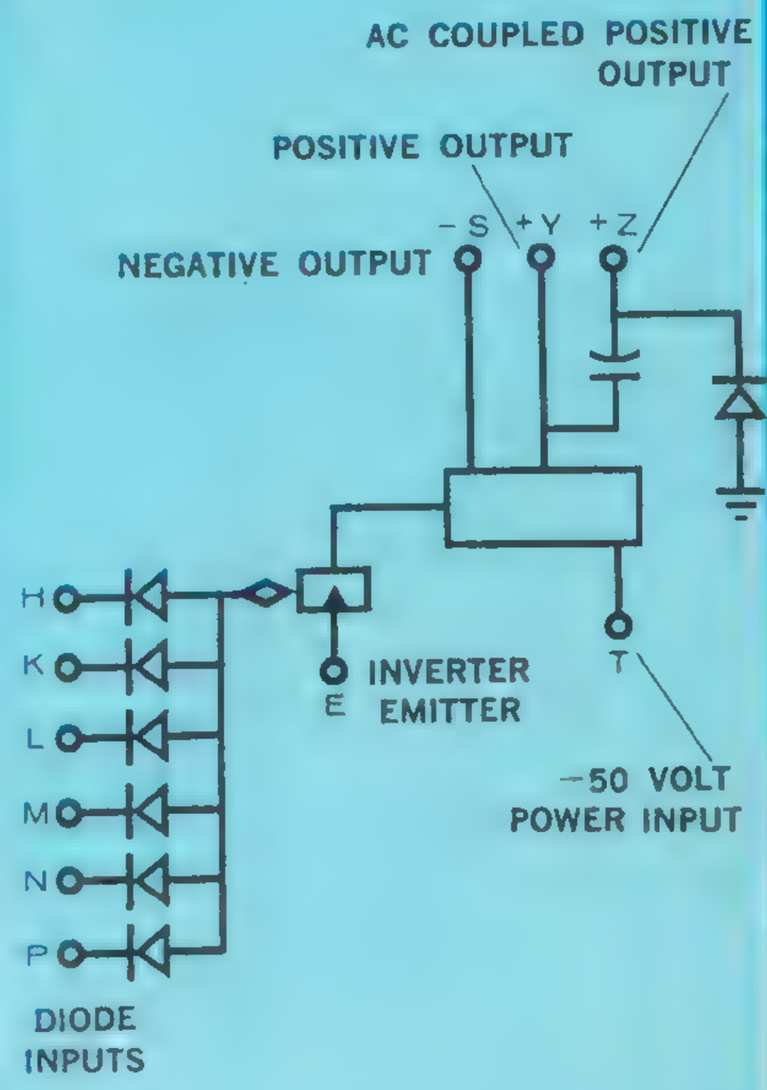
OUTPUT: The upper output level is ground. The lower output level is determined by the external supply attached to the clamp diodes, and must be in the range of ground to −15 volts. When the output signal is at ground, each inverter will supply up to 10 ma to external circuitry. When the output level is negative, the maximum current which can be accepted is determined by the 1500-ohm resistor to −15 volts.

POWER: −15 volts/82 ma; +10 volts (A)/0.45 ma; +10 volts (B)/0.45 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4676
INTENSITY AMPLIFIER



The Type 4676 Amplifier produces a 50 volt gate which will supply the grid or cathode of a cathode ray display tube. Outputs available include a direct coupled negative gate (0 to −50 volts), a direct coupled positive gate (−50 to 0), and an AC coupled positive gate with respect to ground. The total transition time for the amplifier is less than 8 microseconds.

INPUT: The amplifier will be turned on when all diode inputs are at ground or the emitter of the input inverter is at −3 volts. Input signals are DEC Standard Levels or equivalent. The diode inputs represent 2 units of Base Load shared among those inputs which are negative. The emitter input is 1 unit DC Emitter Load.

OUTPUT: Pin S will be at −50 volts when the amplifier is turned on and at −1 volt when the amplifier is off. ±5 ma can be supplied at the upper level. Output current at the lower level is determined by 36,000 ohms to −50 volts. Output pin Y will be at −1 volt when the amplifier is turned on and −50 volts when the amplifier is off. Pin Z is coupled to pin Y by a 0.1 microfarad capacitor. The output at this point will go to +50 volts when the amplifier is turned on and will return to ground when the amplifier is turned off. Pins Y and Z together can supply the same amount of current as pin S.

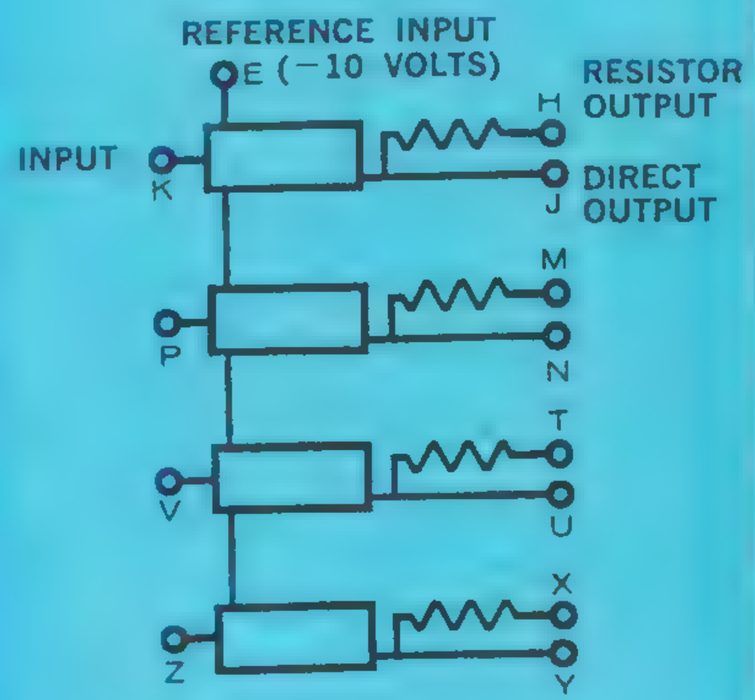
POWER: −50 volts/14 ma*; −15 volts/37 ma; +10 volts (A)/0.8 ma; +10 volts (B)/0.4 ma.

*Must be supplied from an external source.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4677-4677A
SINGLE-ENDED BRIDGES



Each module contains four single-ended bridge amplifiers which are designed principally for driving DEC Digital-to-Analog Converter Networks. The amplifiers may also be used as bus drivers. The output voltages for the amplifiers are ground and a negative voltage (of up to −10 volts). A similar amplifier also useful for these purposes is the Type 1677.

INPUT: The input signals are DEC Standard Levels or equivalent. Each input represents two units of Base Load.

POWER: Reference Voltage — The reference voltage supplies all output current plus a nominal amount for internal use. This voltage may be as great as −10 volts. When the amplifier is used in digital-to-analog conversion, −10 volts is recommended for the greatest accuracy. In this case, a maximum of ±13.2 ma will be required. For other applications, the maximum current required should not exceed 120 ma total towards ground.

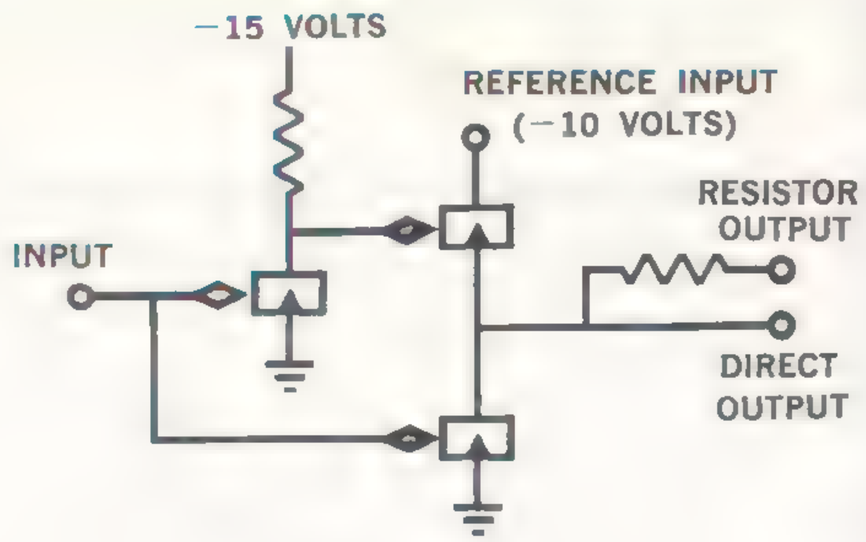
OUTPUT: A ground input gives a negative output. A −3 volt input gives ground output. Each output is available either directly or through a 100-ohm resistor. The direct output should always be used to drive digital-to-analog converter networks. (Either output may be used in driving the Type 1561 Digital-to-Analog Converter). If the amplifier is used for any other purpose, the 100-ohm resistor outputs should be used in order to protect the transistors from accidental shorting to ground. Up to 15 ma can be supplied at the ground level and up to 30 ma at the reference level. The output terminal should never be shorted directly to any external voltage or ground.

Table 1 shows a summary of the different characteristics of the amplifiers: Column I shows the variation in output impedance with the output connected through a resistor (greater than 3000 ohms) to −10 volts. Column II shows the variation in output impedance with the output at −10 volts and connected through a resistor (greater than 3000 ohms) to ground. Column III shows the total transition time, measured from 10% of input to 90% of output.

POWER: −15 volts/40 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0.6 ma.

SINGLE ENDED BRIDGE TABLE

Type	To Reference Voltage (ohms)	To Ground (ohms)	Total Transition Time (microsecond)
1677	0 - 7	5 - 15	0.045
4677	1 - 5	4 - 9	0.2
4677A	0 - 3	1 - 3	1.5



PUT
S)

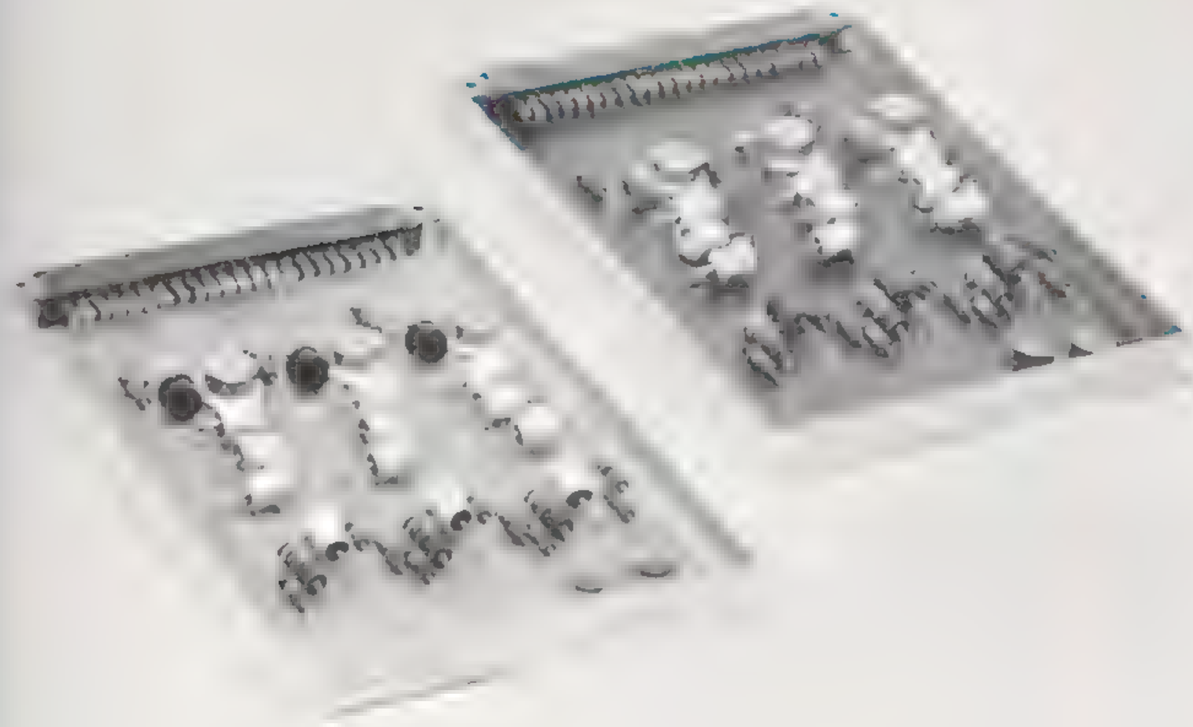
ESISTOR
OUTPUT

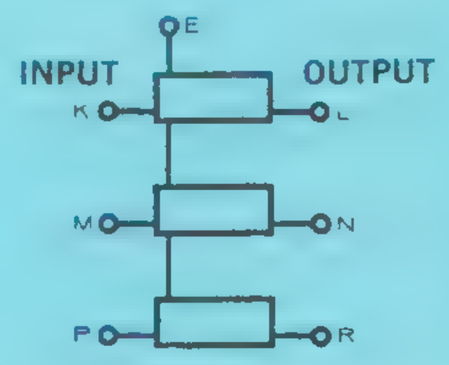
DIRECT
OUTPUT

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4680-4681
SOLENOID DRIVER





Three amplifiers amplify DEC Standard Levels into outputs suitable for driving solenoids. The output signals are −3.5 volts and a more negative voltage that is determined by an external supply. A diode protects the solenoid driver from back EMF generated by the solenoid when the driver is turned off. For the Type 4680, the more negative output may be as great as −35 volts; for the Type 4681, it may be as great as −70 volts.

INPUT: Inputs are DEC Standard Levels or equivalent, which represent 2 units of Base Load (no capacitance).

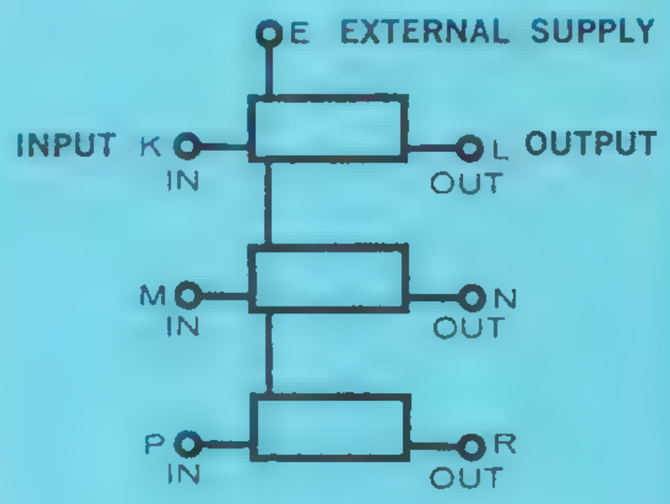
OUTPUT: A ground signal at the input produces a −3.5 volt output. A DEC Negative Level at the input produces the more negative output, as determined by the external supply. This voltage may be as great as −35 volts for the Type 4680 and −70 volts for the Type 4681. Each driver can supply up to 500 ma.

POWER: Type 4680: −15 volts/144 ma; +10 volts (A)/3 ma; +10 volts (B)/0 ma. **Type 4681:** −15 volts/144 ma; +10 volts (A)/3 ma; +10 volts (B)/0 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4682
POSITIVE SOLENOID DRIVER



Three drivers amplify DEC Levels to outputs suitable for driving solenoids. Output signals are ground and a positive voltage (up to +28 volts) from an external power supply. Driving capability is 100 ma.

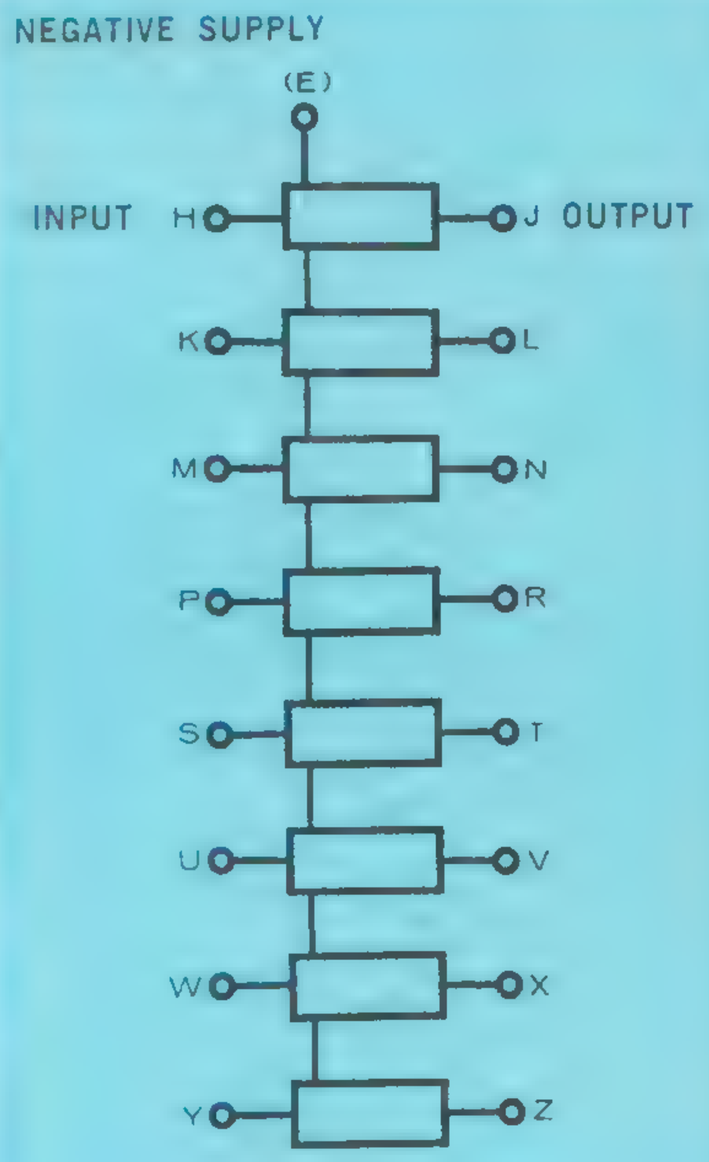
INPUT: The inputs require DEC Standard Levels or equivalent (1⅔ units Base Load).

OUTPUT: A DEC Standard Negative Level input produces a positive voltage, determined by an external power supply. This positive voltage may be as great as +28 volts. A ground input level produces a ground level output. The unit is capable of driving 100 ma.

POWER: −15 volts/0 ma; +10 volts (A)/4.8 ma; +10 volts (B)/33.6 ma.

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4685
LEVEL AMPLIFIER



Eight circuits convert DEC Standard Levels into 0 and —30 volt levels. The maximum operating frequency of this module is 50 kilocycles. Typical total transition times are 20 microseconds for output fall and 2 microseconds for output rise.

INPUT: Inputs are DEC Standard Levels. Each input represents 1 unit of Base Load.

OUTPUT: A —3 volt input produces a ground output which will be no more negative than —0.2 volts while supplying up to 5 ma to an external load. A ground input produces a —30 volt output. The output driving capability in this state is determined by the 3000-ohm internal load resistor to —30 volts.

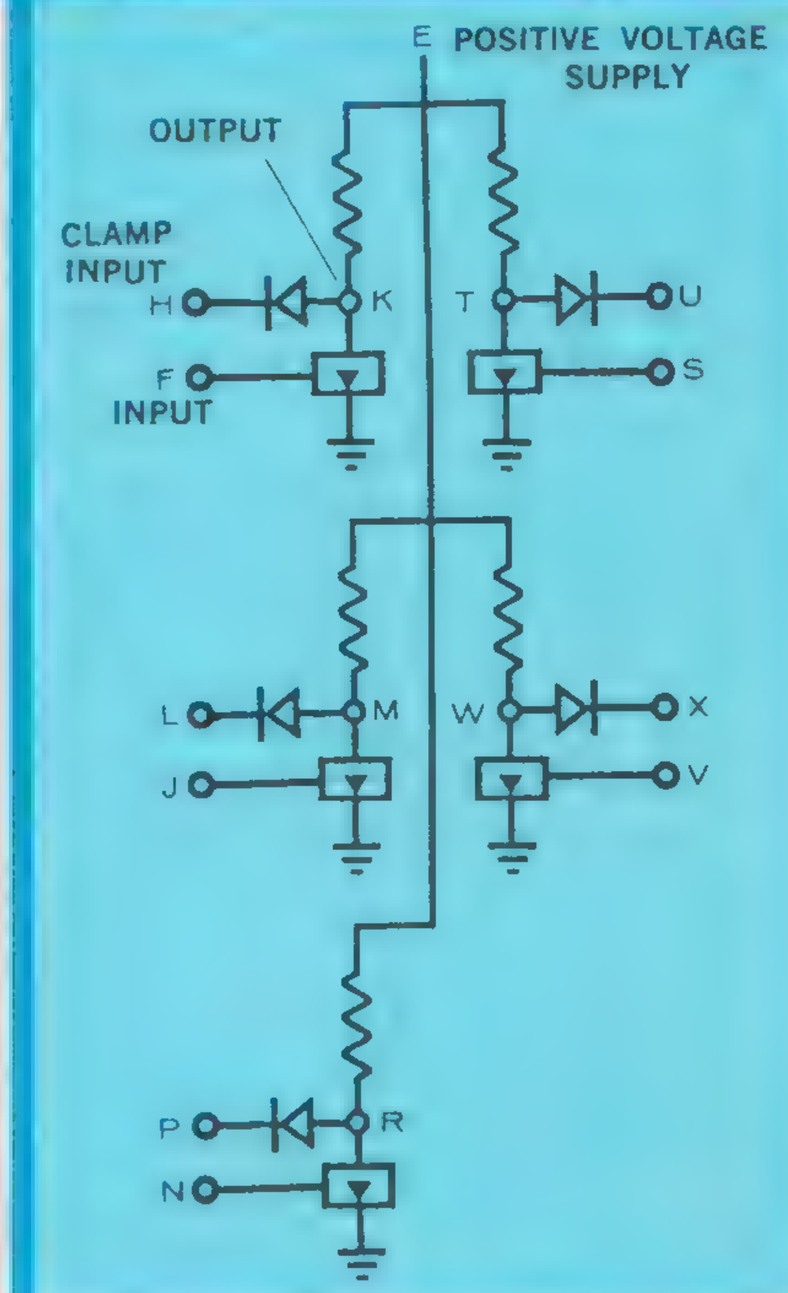
POWER: An external power supply should supply —30 volts to pin E. This source should be capable of supplying 80 ma. If desired, this voltage can be produced from the DEC Type 743 Dual Power Supply by placing the two halves of the floating 15 volt power supply in the series. The supply is then capable of providing 8.5 amperes.

POWER: —15 volts/0 ma; +10 volts (A)/1.3 ma; +10 volts (B)/0 ma; —30 volts (E)/ 80 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4686
POSITIVE LEVEL AMPLIFIER



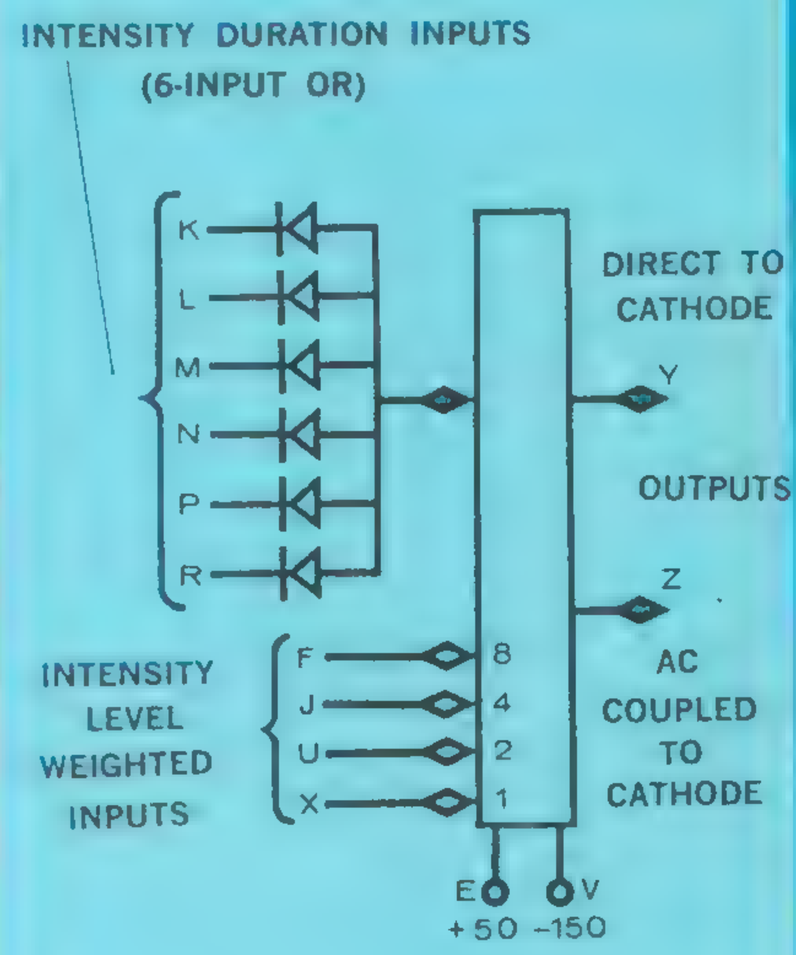
The five amplifier circuits contained in the Type 4686 are similar to DEC Inverters using NPN transistors instead of PNP. This unit is used to convert DEC Standard Levels to levels of ground and some positive voltage between 0 and +20 volts. The positive voltage is determined by the clamp voltage. The load resistors are brought out to pin E, and should be connected to +10 volts or to an external source up to +20 volts.

INPUT: Requirements for the inputs are DEC Standard Levels (1⅓ units Base Load).

OUTPUT: A ground input signal produces a ground output signal capable of supplying up to 20 ma to the 1000-ohm load resistor and external circuitry. A negative input signal produces a positive voltage (determined by the external clamp).

POWER: −15 volts/0 ma; +10 volts (A)/4 ma; +10 volts (B)/0 ma.

4688
VARIABLE AMPLITUDE NEGATIVE INTENSIFIER



Type 4688 is used to generate the intensity gate in an oscilloscope display system when the intensity level is to be under program control. Selection of one of the sixteen-output gate amplitudes between −1 and −20 volts is accomplished by decoding the four-bit intensity level input. The duration of the output gate is determined by the duration of the negative level input to any of the six OR gate inputs. The turn-on time varies between 0.1 and 0.3 microsecond, determined by the intensity level selected. The turn-off time is 0.3 microsecond for all intensity levels.

INPUT: Intensity Duration — The intensity gate will be on as long as there is a −3 volt level into any of the six-input OR gate inputs. The load is 1 unit of Base Load shared among the negative inputs. **Intensity Level** — These inputs are weighted as shown on the logic diagram. If all inputs are ground the maximum gate level of weight 15 will be generated. If, for example, only J and U are ground, a gate level of weight 6 will be generated. The maximum gate of −20 volts is produced with an input weight of 15, and the minimum gate of −1 volt is produced with an input weight of 0. The input load of F is 2 units of Base Load; pin J is 1 unit of Base Load; pin U is ½ unit Base Load; and pin X is ¼ unit Base Load.

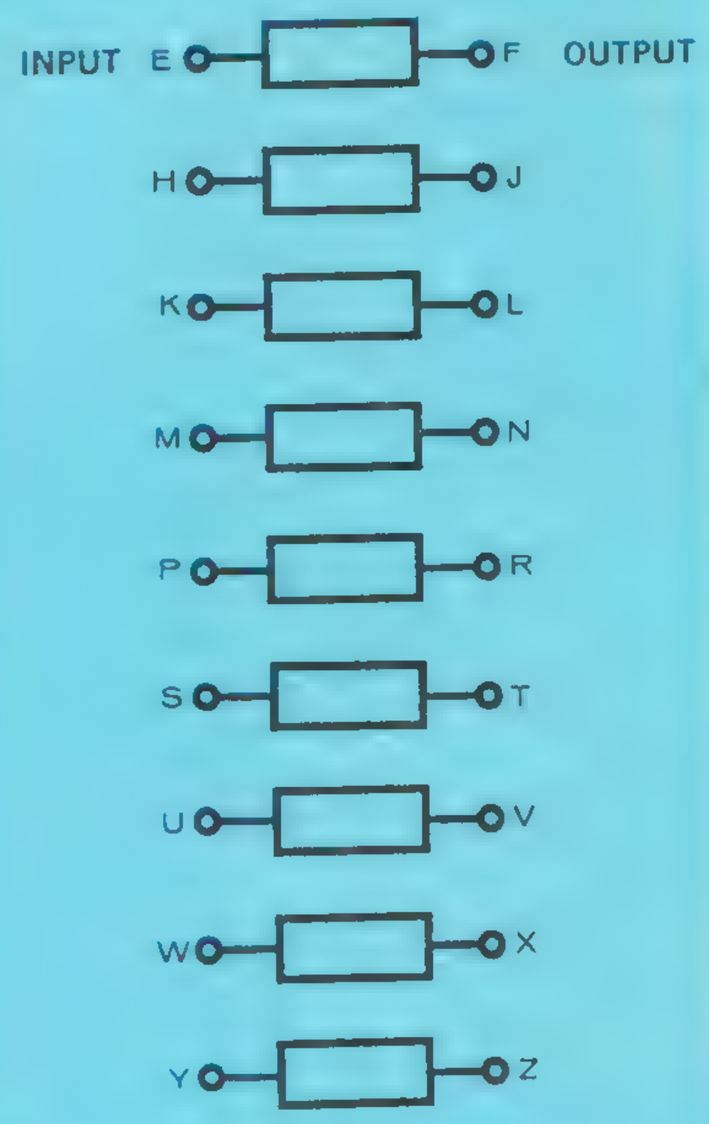
OUTPUT: Direct Output — This output is normally at a DC level of about −1 volt. The output gate will be a −1 to −20 volt change from this quiescent level, so that the output gate will be at a DC level of −2 to −21 volts. The turn-on time varies from 0.1 to 0.3 microsecond depending on the intensity level selected, while the turn-off time is 0.3 microsecond for all levels. **AC Coupled Output** — This output is the direct output through a 0.01 microfarad capacitor with a diode and 100,000-ohm resistor to ground. The quiescent level is ground, and the output gate will be between −1 and −20 volts.

POWER: −15 volts/10 ma; +10 volts (A)/0.6 ma; +10 volts (B)/0 ma; +50 volts/3 ma; −150 volts/14 ma.

digital

4000 SERIES
SYSTEM MODULES
500 KILOCYCLES

4689
INDICATOR DRIVER



The Type 4689 contains nine transistor amplifiers each capable of driving an incandescent bulb that requires 100 ma and 15 volts. It is ideal for providing remote indicators from DEC System Module Flip-Flops. The indicator lights are on whenever the inputs to their respective amplifiers are −3 volts. If the input is from the ONE output of a flip-flop, it indicates a ONE state.

INPUT: The input requires DEC Standard Levels or equivalent and represents 3 units of Base Load.

OUTPUT: Each output is suitable for driving an indicator lamp that is returned to −15 volts. Other loads may be driven, providing the required current is no greater than 100 ma and the voltage is no lower than −20 volts.

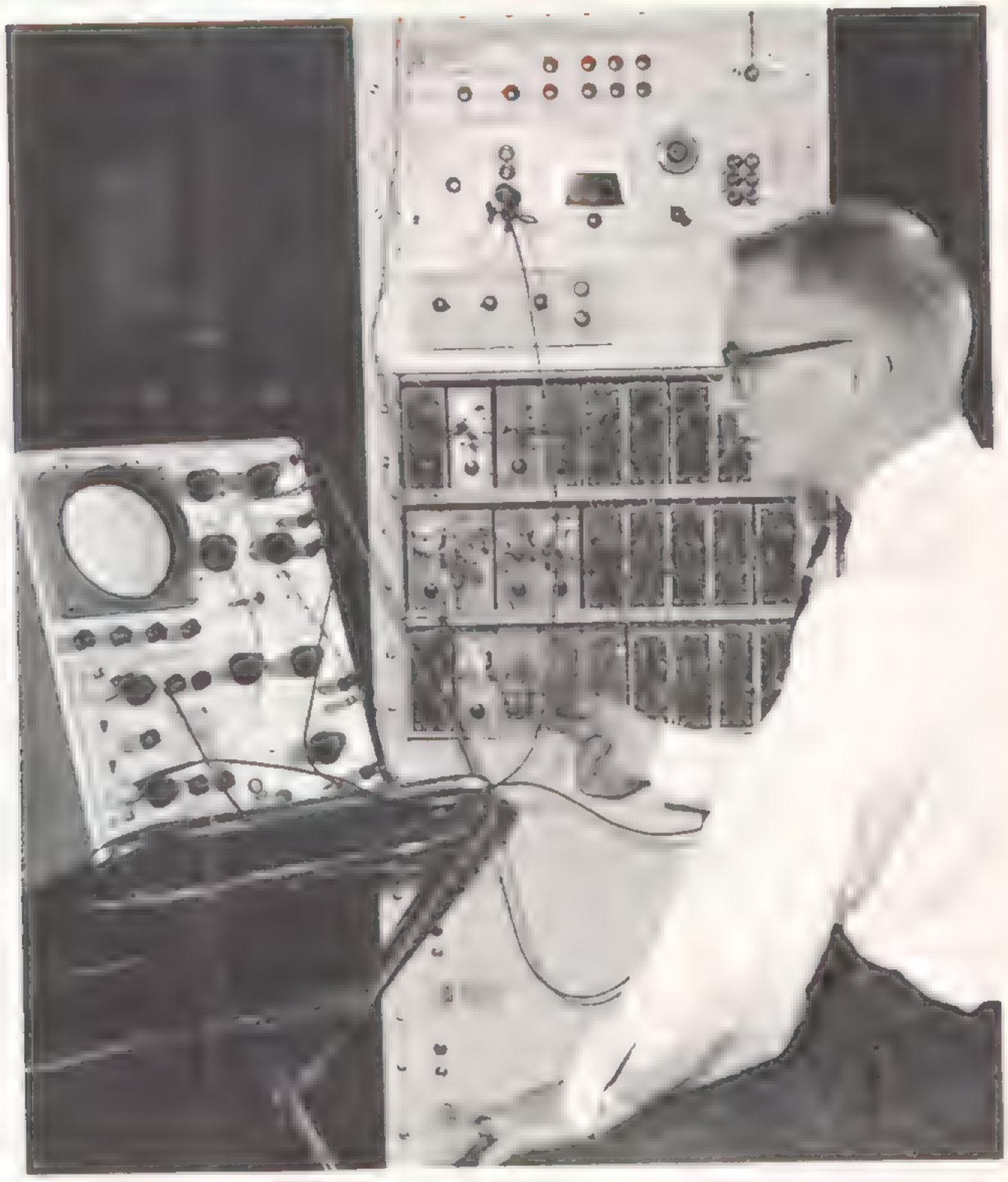
POWER: +10 volts (A)/4 ma; +10 volts (B)/0 ma; −15 volts/900 ma*

*This voltage is not supplied to this unit; this is the maximum current drawn by the remote loads from −15 volts when they are all turned on.

digital

5000 SERIES
LABORATORY MODULES
10 MEGACYCLES

SERIES CHARACTERISTICS



Laboratory Modules of different speeds may be incorporated in a single system as required

DEC 5000 Series Laboratory Modules are a coordinated set of solid state digital circuits operating at frequencies up to 10 megacycles. They are packaged in sturdy aluminum cases, measuring 1¾ x 4½ x 7 inches with graphic front panels which illustrate the logical function of each module. All logical interconnections are made on the front panels with miniature stacking banana jack patch cords. Power connections are made automatically when the modules are inserted in the Type 901 Laboratory Module Mounting Panel.

This unique method of packaging and special built-in safety features make these high quality circuits ideal for test equipment and laboratory use. Logical signals are in the range of 0 to −3 volts, which permits logical experimentation without the risk of damage to the circuitry. By following simple, well-defined loading rules, the user can quickly and easily duplicate existing systems for test or instruction purposes or implement new and unusual systems designs. The modules may be assembled and reassembled in countless combinations to meet any type of test or design requirement.

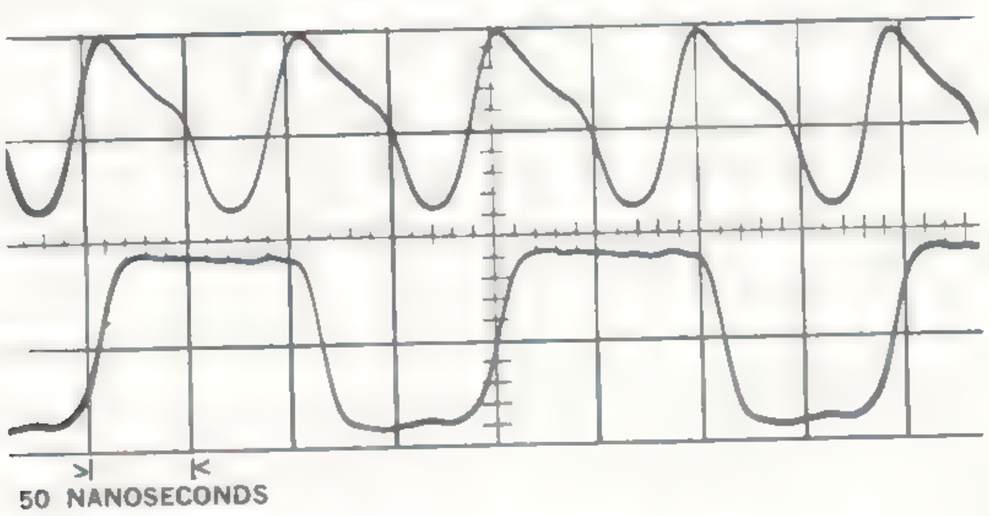
A particular advantage of all Digital Modules is their complete compatibility across speed lines. The 5000 Series units are mechanically and electrically compatible with the 100 and 3000 Series Laboratory Modules, and they are electrically compatible with the 1000, 4000 and 6000 Series System Modules. Thus systems capabilities may be readily extended, if desired, by incorporating suitable units from other lines.

The logic employed in all DEC Laboratory Modules, as described in the Introduction, uses static flip-flops with level logic and pulse sampling. The flip-flop outputs are buffered and include a built-in delay which permits the flip-flops to be pulse-sampled while being changed. Logic gating is performed with series and parallel combinations of DEC saturating transistor inverters. This method of transistor gating and pulse sampling allows the construction of systems with a minimum of concern over wiring techniques and lead lengths.

The basic selection of logic modules in the 5000 Series includes a six inverter package for logical gating, a general purpose flip-flop with buffered level outputs and built-in carry pulse output, a delay line with built-in pulse amplifier, both variable frequency and stable crystal clocks, and a dual pulse amplifier package for logical gating and standardization of input pulses.

DEC Standard Levels, used in all Digital Modules for performing logical gating functions, are 0 and −3 volts. DEC Standard Negative Pulses, used for sampling logic levels, are 2.5 volts in amplitude. The pulse width, which is commensurate with the speed line, is 40 nanoseconds in the 5000 Series. This pulse may be converted to a 70 nanosecond pulse with the 602 pulse amplifier with feedback.

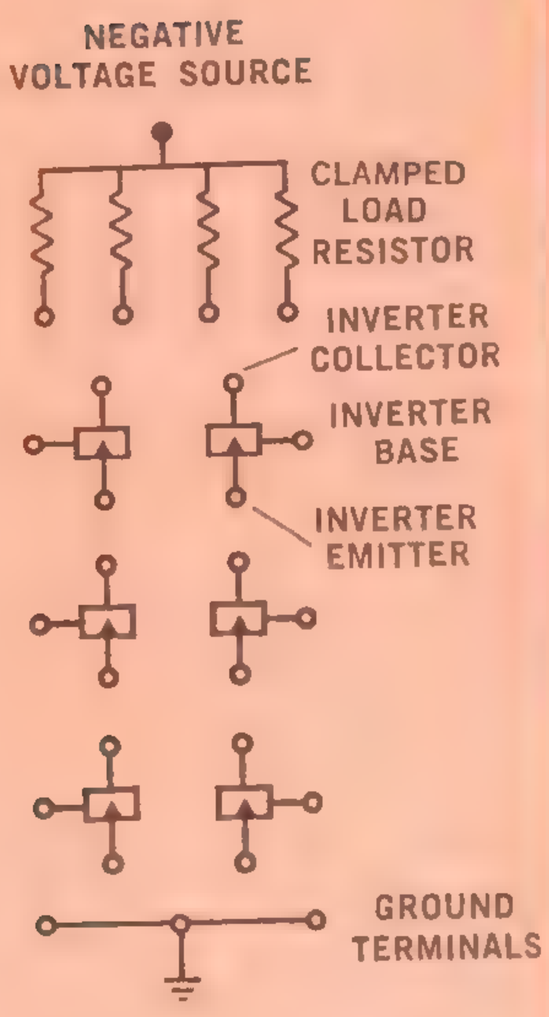
DEC STANDARD 40 NANOSECOND NEGATIVE PULSES



DEC TYPE 5202 FLIP-FLOP OUTPUT

5000 SERIES
LABORATORY MODULES
10 MEGACYCLES

5101
INVERTER



The Type 5101 contains six transistor inverters for use as pulse gates or level gates, and four load resistors clamped to —3 volts. All logical terminals are available at the socket. Delay through an inverter is approximately 12 nanoseconds. Each inverter is analogous to a switch. If —3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base is brought to ground, the emitter-collector path is open.

INPUT: Base — The inputs are DEC 40 nanosecond Negative Pulses when the inverter is used as a pulse gate, at any frequency up to 10 megacycles (1 unit of Pulse Load). The inputs are DEC Standard Levels or equivalent when the inverter is used as a level gate (1 unit of Base Load). **Emitter** — DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If the base input is a pulse, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can drive 2 units of Base Load at 10 megacycles, 7 where speed is not a problem. A collector can be connected to several emitters simultaneously providing not more than one of the inverters is conducting at a time. No more than two level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, three gates may be connected in series. The pulse gate must be placed at the beginning of the string (the end farthest from the load).

POWER: —15 volts/40 ma; —3 volts/37 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

INVERTER USAGE

The high speed transistors used in 10 megacycle inverters have a larger saturation voltage drop than the transistors used in the 5 megacycle and 500 kilocycle inverters. Because of this slightly larger DC drop, a maximum of two inverters may be put in series if the output is to drive another inverter. (See Figure 1). If a flip-flop output is driving an inverter emitter, this flip-flop must be counted as an inverter. (See Figure 2)

When the output of a series of transistor inverters is driving the input of a flip-flop or pulse amplifier, as in Figure 3, an inverter pulse gate may be added in series with the two level gates. This pulsed inverter must be placed at the bottom of the series string; that is, the end farthest from the load. The emitter may be driven by a flip-flop unless the sampling pulse is a P pulse (the carry pulse in counters); in this case the emitter should be grounded.

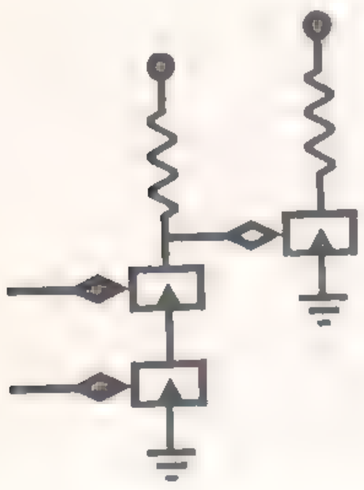


Figure 1

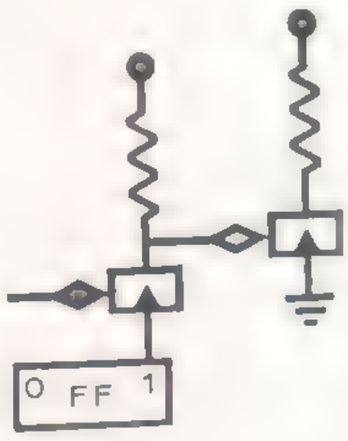


Figure 2

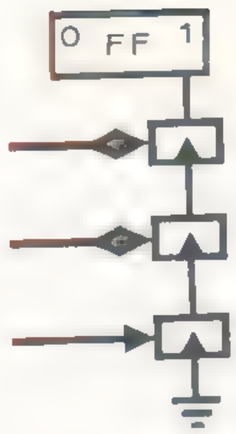


Figure 3

When connecting 10 MC inverters, the user sho... avoid wiring inductance and stray capacitance ... much as possible. Figure 4 illustrates how a wi... which is conducting current for two pulsed inverte... back to the flip-flop output, may serve as a coupli... connection between the two pulsed inverters a... produce ringing. This ringing may produce a positi... pulse of the emitter of the other inverter, thus tu... ing it on at the wrong time. To avoid this, eac... emitter must be driven by a separate wire, unle... the distance is very short.

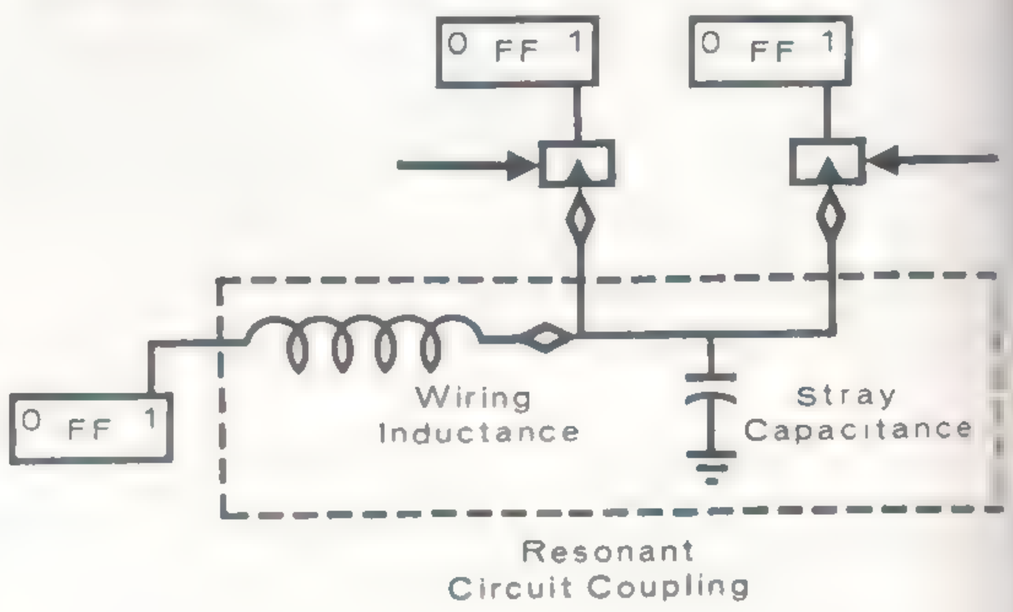
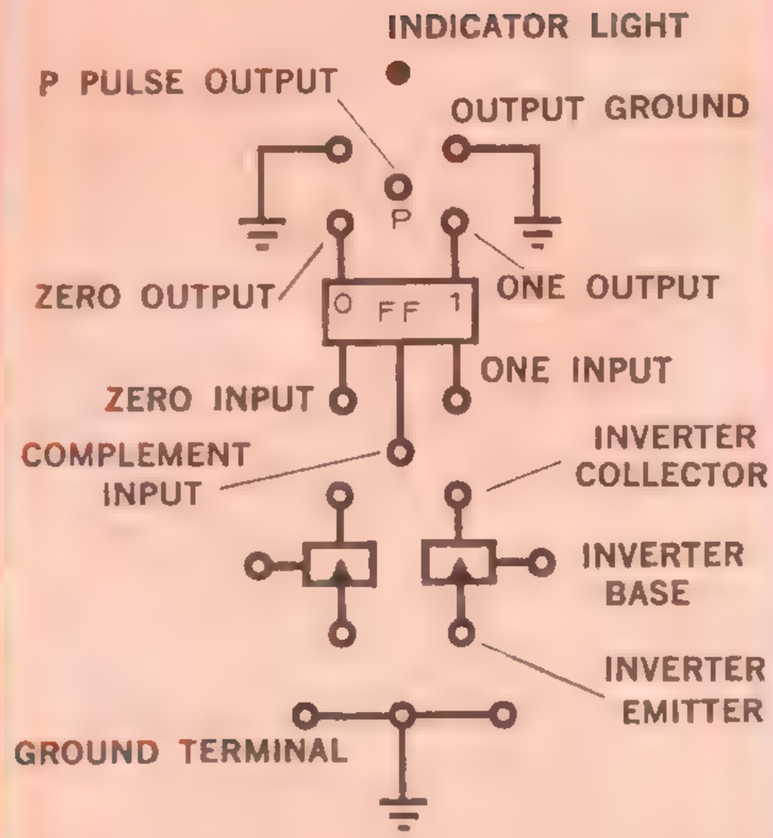


Figure 4

5202
FLIP-FLOP



The Type 5202 contains one flip-flop with built-in output amplifiers, gated inputs to the ZERO and ONE side, a gated Complement input and a Carry output pulse. It also contains an indicator light and two transistor inverters for use as pulse or level gates. The output signals have built-in delays so that they can be sensed reliably at the same time that the input is being pulsed. This general purpose flip-flop is useful in counter, shift register and adder applications.

INPUT: Gated Clear, Set, and Complement signals must come from one or more collectors of pulse gates. Each input terminal represents 1 unit Pulse Load. These signals can occur in any sequence, at any frequency, and at any time intervals which have a minimum of 100 nanoseconds between any two consecutive signals (maximum frequency of 10 megacycles). The two inverters are similar to those included in DEC Inverters Types 5101 and 6105.

OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving up to 6 loads (including both Base and Emitter Loads) at 10 megacycles. However, there can be only 1 unit of DC Emitter Load, and only 1 unit of Pulsed Emitter Load at a time. At frequencies of less than 5 megacycles each output may simultaneously drive: (a) 14 units of Base Load; (b) 1 unit of DC Emitter Load; and (c) any number of Pulsed Emitter Loads, providing not more than one is pulsed at a time.

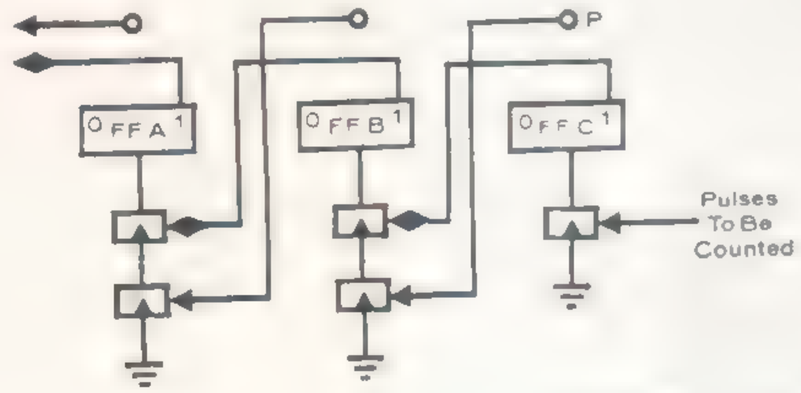
The output grounds are located adjacent to the output terminals and are to be carried along with the output signal via a twisted pair of wires to maintain low output impedance. Each time the Complement terminal is pulsed, a DEC Standard 40 nanosecond Negative Pulse will occur on the P terminal. This pulse is capable of driving one inverter base; however, the inverter emitter must be permanently grounded. The P Pulse will be delayed by approximately 15 nanoseconds with respect to the signal on the base of the input inverter.

POWER: −15 volts/110 ma; −3 volts /10 ma; +10 volts (A)/1.4 ma; +10 volts (B)/1.6 ma.

BINARY COUNTERS

A typical counter arrangement using DEC Complementing Flip-flops is shown above. The pulses being counted enter on the right. They always complement flip-flop C and generate a standard pulse at P. This P Pulse complements flip-flop B when flip-flop C holds a ONE. When this P Pulse gets through the gate and actually complements B, it will generate a P Pulse out of B. The process is continued down the length of the counter.

The series connection of P Pulses and gates forms a high-speed carry chain. The carry propagate time per digit (15 nanoseconds) is much less than the flip-flop's total transition time. To assure that flip-flop C will not be in the process of changing state while flip-flop B is receiving its carry pulse, a delay has been built into each flip-flop package. This insures that the ONE and ZERO output terminals will not change until after the carry pulse has been gated.

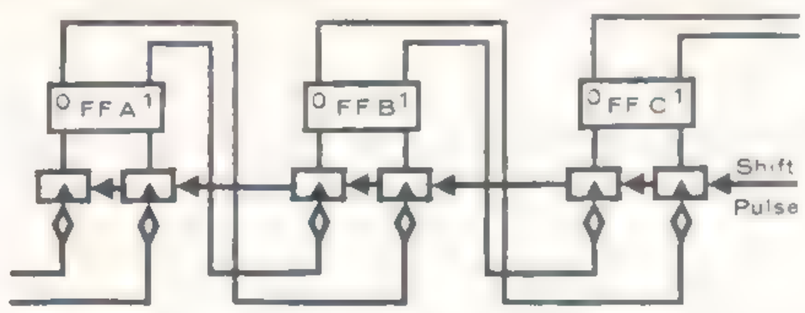


COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure 1 — BINARY COUNTER

SHIFT REGISTERS

Each Type 5202 package will make one stage of a shift register. DEC shift registers employ simultaneous jam transfer. As illustrated in Figure 2, the contents of all flip-flops are simultaneously moved to the right when the shift pulse occurs. Since the flip-flop outputs do not change until after the shift pulse has passed, no logical delays are needed between flip-flops.



COUNTING SEQUENCE	
0	00
1	01
2	10

Figure 2 — SHIFT REGISTER

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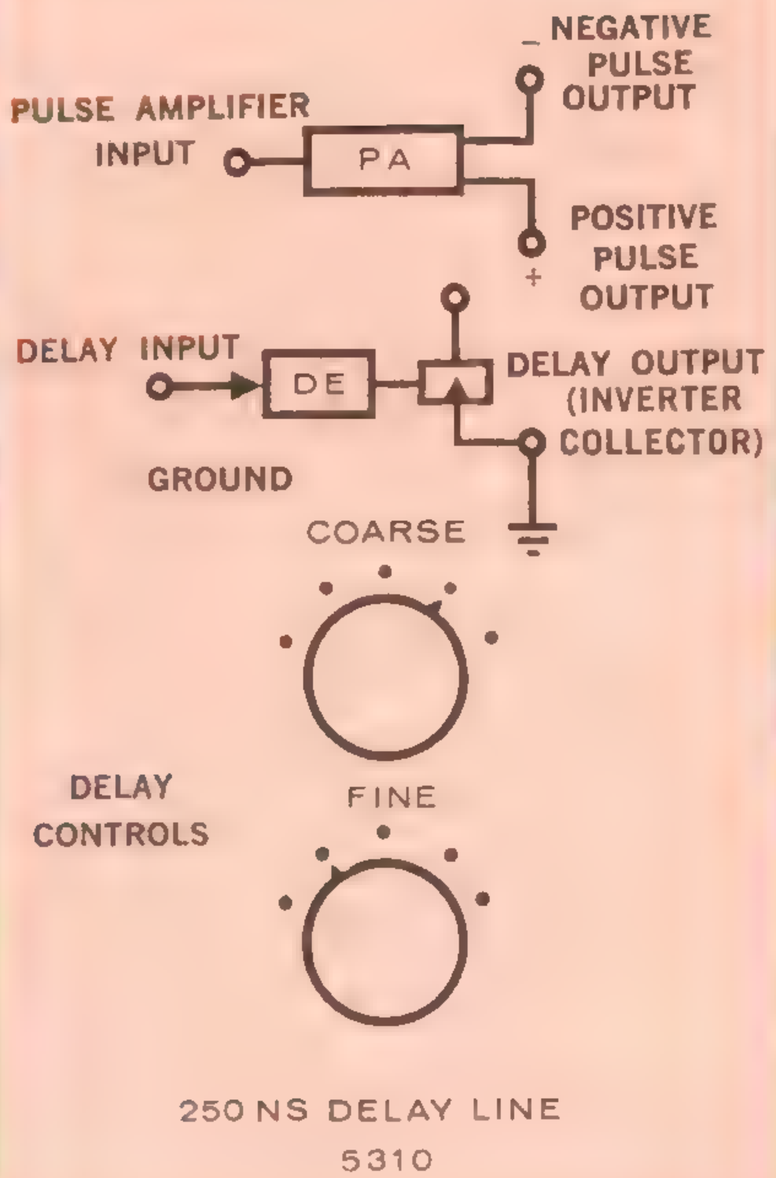
between

5000 SERIES
LABORATORY MODULES
10 MEGACYCLES

5310
DELAY LINE



250 NS DELAY LINE
5310

The Type 5310 contains a 0.25 microsecond delay line which may be connected to obtain delays up to 0.25 microsecond in 12.5 nanosecond steps.

INPUT: The input is a DEC Negative 2.5 volt 40 nanosecond pulse or equivalent (2 units of Pulse Load).

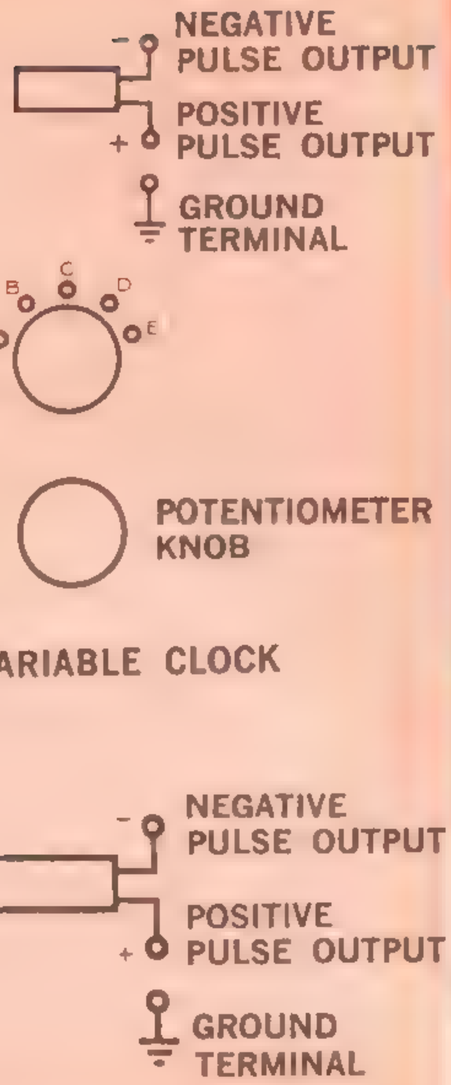
OUTPUT: The output of the inverter collector must be connected to the input of a Pulse Amplifier such as the one contained in the unit, or one section of a 5602 Pulse Amplifier. If additional logical gating is required, it may be done with up to 2 transistor inverters placed in series between the inverter collector and the Pulse Amplifier. The minimum delay including the Pulse Amplifier is 25 nanoseconds.

POWER: −15 volts/64 ma; −3 volts/−53 ma; +10 volts (A)/2.8 ma; +10 volts (B)/0 ma.

digital

5000 SERIES
LABORATORY MODULES
10 MEGACYCLES

5401-5403
CLOCKS



5401 VARIABLE CLOCK

5403 CRYSTAL CLOCK

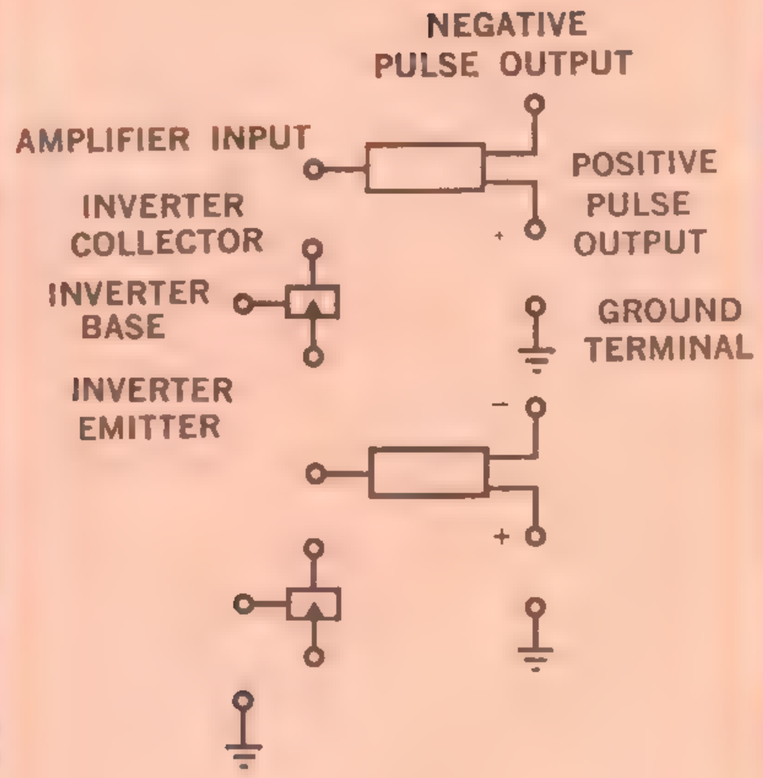
The Type 5401 Variable Clock contains a stable multivibrator type, variable frequency oscillator with a pulse output for use as a source of timing pulses for DEC 10 megacycle System Modules. The frequency is variable from 250 cycles to 10 megacycles. Five overlapping ranges provide coarse frequency control and a built-in potentiometer permits fine adjustment. Lower frequencies may be obtained by adding a capacitor internally in parallel with those that are connected to the coarse range switch.

The Type 5403 employs a series resonant crystal oscillator circuit and pulse shaping buffer amplifiers to provide very precise timing. The amplifiers produce DEC Standard 40 nanosecond Pulses in the 5 to 10 megacycle range. The clock frequency, specified by the customer, is stamped on the module.

OUTPUT: The outputs are DEC Standard 40 nanosecond Pulses, of either polarity, which occur at the preselected frequency. The pulse will be positive if the negative terminal is grounded or negative if the positive terminal is grounded. Crystal Clock: The stability of the crystal clock's output frequency is 0.01% over the temperature range of −20 to +55°C. Variable Clock: A 10% change in the power supply voltage of the Type 5401 Clock will change the prf less than 0.5% and its pulse-to-pulse jitter is less than 0.2%.

POWER: Type 5401: −15 volts/185 ma; −3 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma. Type 5403: −15 volts/60 ma; −3 volts/0 ma; +10 volts (A)/0 ma; +10 volts (B)/0 ma.

5602
PULSE AMPLIFIER



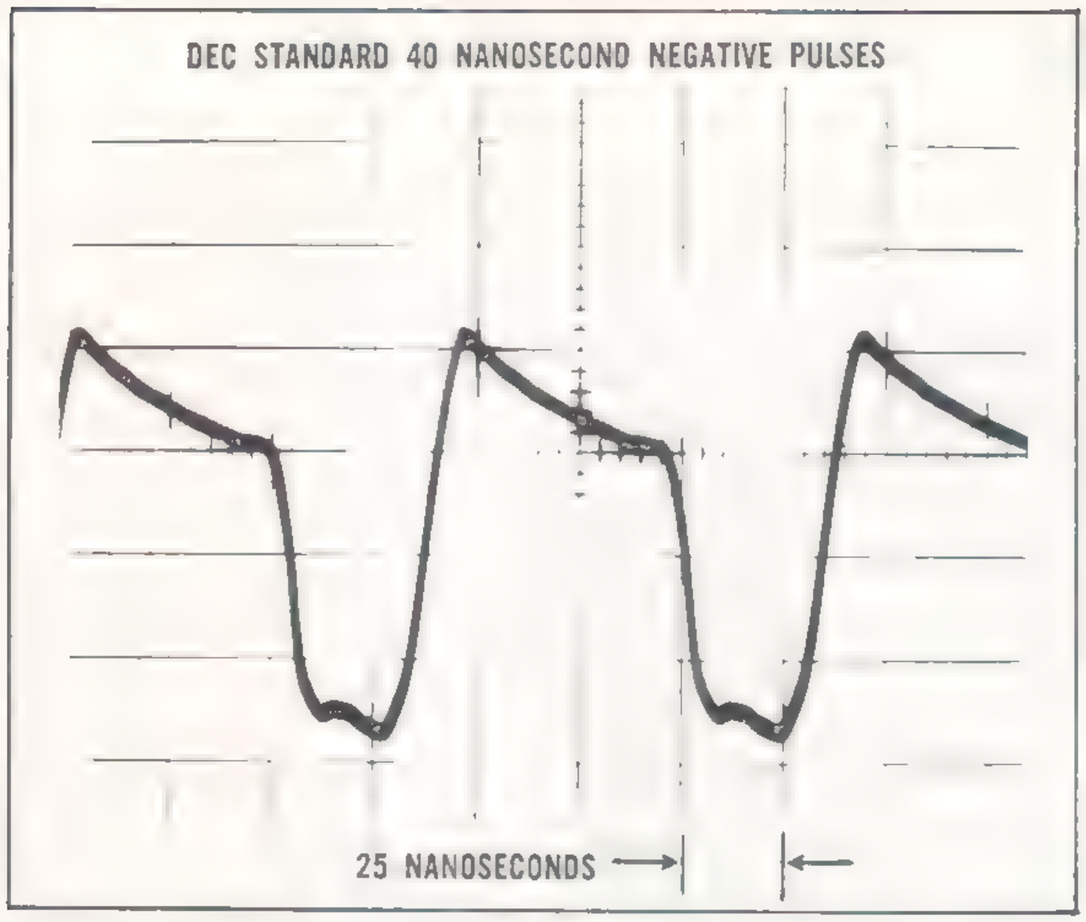
The Type 5602 contains two pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Two inverters are available for gating input levels or for mixing pulses. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 10 megacycles.

INPUT: The input to the base of the inverter whose collector drives the pulse amplifier is normally a DEC Standard 40 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 25 nanoseconds and width (at 2 volts) greater than 25 nanoseconds, can be used. Input pulses of less than −0.5 volts will not generate an output pulse.

Many pulse gate collectors can be connected together to mix pulse sources. The two pulse gates are inverters like those included in the DEC Inverter Types 5101 and 6105.

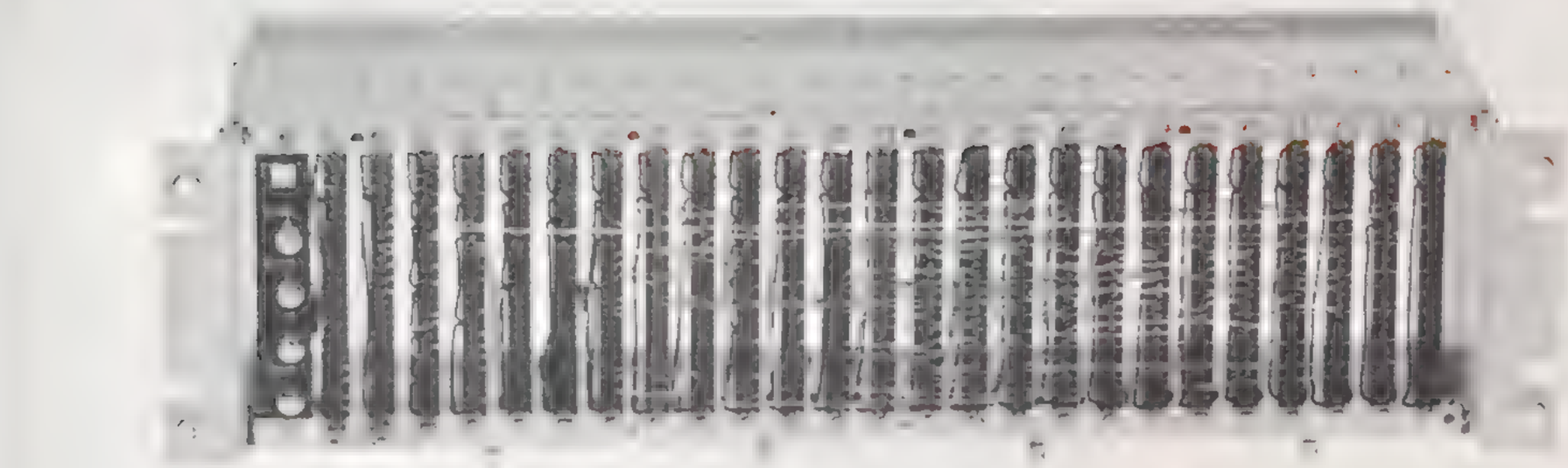
OUTPUT: The output is a DEC Standard 2.5 volt 40 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. The output will be negative if the positive output terminal is grounded; it will be positive if the negative terminal is grounded. Each output is capable of driving 12 units of Pulse Load.

POWER: −15 volts/125 ma; −3 volts/10 ma; +10 volts (A)/0.2 ma; +10 volts (B)/0.2 ma.


DEC STANDARD 40 NANOSECOND NEGATIVE PULSES
25 NANOSECONDS

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

SERIES CHARACTERISTICS



Patchcord Mounting Panels facilitate the use of System Modules in design applications

DEC 6000 Series System Modules are a coordinated set of solid state digital circuits operating at frequencies up to 10 megacycles. They are mounted on protective aluminum frames measuring ½ by 4½ by 7 inches overall. All logic and power connections are through 22-pin Amphenol plugs electrically connected to the circuit boards by flexible wires to minimize strain. Plug-in mounting panels for System Modules are available in various widths, capacities and wiring options.

System Modules offer a unique combination of advantages for the design and construction of all types of digital systems. They are built for long, dependable service, whether used interchangeably in different applications or installed in permanent systems. General purpose circuits permit systems to be implemented with a minimum number of different types of modules. Special purpose units provide economy in the construction of large-scale systems.

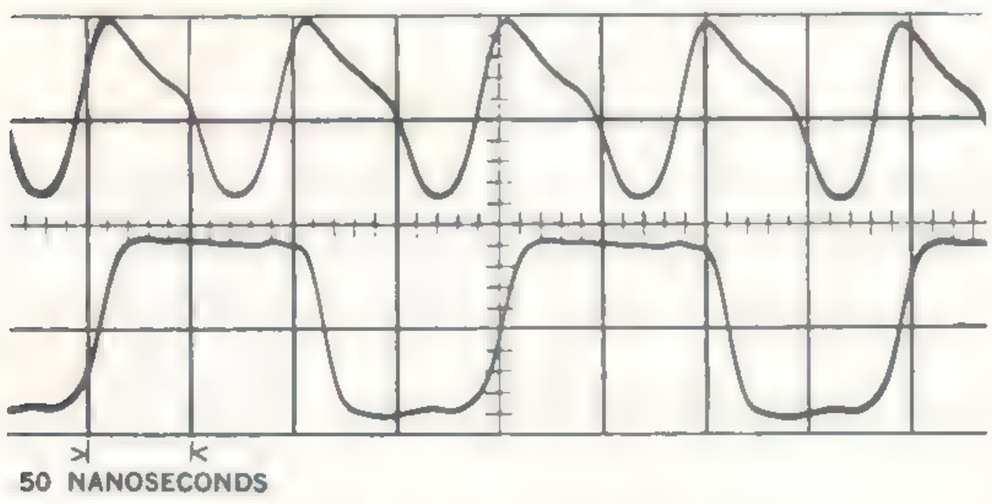
Since all Digital Modules are compatible across speed lines, it is possible to extend system capabilities or to achieve important savings in systems construction by incorporating units from other lines. The 6000 Series units are electrically and mechanically compatible with 1000 and 4000 Series System Modules, and they are electrically compatible with 100, 3000 and 5000 Series Laboratory Modules.

The logic employed in all DEC System Modules, as described in the Introduction, uses static flip-flops with level logic and pulse sampling. Flip-flop outputs are buffered and include a built-in delay which permits the flip-flops to be pulse-sampled while being changed. Logic gating is performed with series and parallel combinations of DEC saturating transistor inverters. This method of transistor gating and pulse sampling allows the construction of systems with a minimum concern over wiring techniques and lead lengths.

The basic selection of general purpose logic modules in the 6000 Series includes two inverter packages for logical gating, a flip-flop with buffered level outputs and built-in carry pulse output, two delay line packages, variable frequency and stable crystal clocks, and a three pulse amplifier package for logical gating and standardization of input pulses.

DEC Standard Levels, used in all Digital Modules for performing logical gating functions, are 0 and −3 volts. DEC Standard Negative Pulses, used for sampling logic levels,.are 2.5 volts in amplitude. The pulse width, which is commensurate with the speed line, is 40 nanoseconds in the 6000 Series. These pulses may be converted to 70 nanosecond pulses with a 70 nanosecond pulse amplifier with feedback as described under the Type 1607.

DEC STANDARD 40 NANOSECOND NEGATIVE PULSES

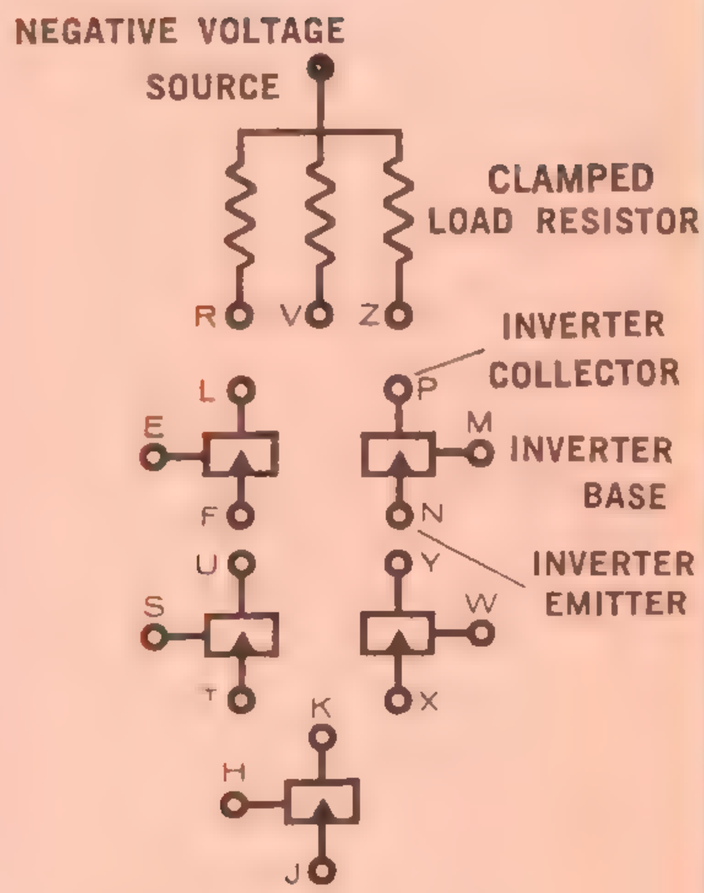


DEC TYPE 6202 FLIP-FLOP OUTPUT

digital

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6105
INVERTERS



The Type 6105 contains five inverters and three clamped load resistors. Each inverter is analogous to a switch. If —3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base is brought to ground, the emitter-collector path is open. Delay through each inverter is approximately 12 nanoseconds.

INPUT: Base — Inputs are DEC Standard 40 nanosecond Negative Pulses when the inverter is used as a pulse gate at any frequency up to 10 megacycles (1 unit of Pulse Load). Inputs are DEC Standard Levels or equivalent when the inverter is used as a level gate (1 unit of Base Load). **Emitter** — The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can drive 2 units of Base Load at 10 megacycles, or 7 units where speed is not a problem. A collector can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than two level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, three gates may be connected in series. The pulse gate must be placed at the beginning of the string (the end farthest from the load).

POWER: —15 volts/52 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.3 ma.

INVERTER USAGE

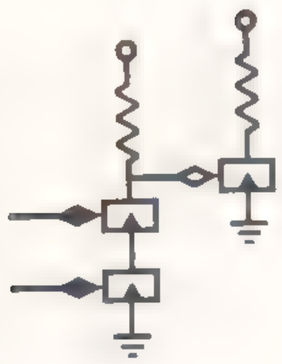


Figure 1

The high speed transistors used in 10 megacycle inverters have a larger saturation voltage drop than the transistors used in the 5 megacycle and 500 kilocycle inverters. Because of this slightly larger DC drop, a maximum of two inverters may be put in series if the output is to drive another inverter. (See Figure 1) If a flip-flop output is driving an inverter emitter, this flip-flop must be counted as an inverter. (See Figure 2)

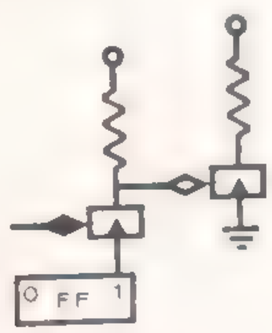


Figure 2

When the output of a series of transistor inverters is driving the input of a flip-flop or pulse amplifier, as in Figure 3, an inverter pulse gate may be added in series with the two level gates. This pulsed inverter must be placed at the bottom of the series string; that is, the end farthest from the load. The emitter may be driven by a flip-flop unless the sampling pulse is a P Pulse (the carry pulse in counters); in this case the emitter should be grounded.

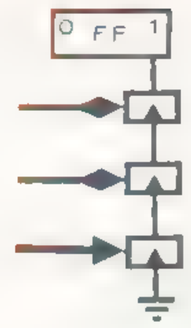


Figure 3

When connecting 10 MC inverters, the user should avoid wiring inductance and stray capacitance as much as possible. Figure 4 illustrates how a wire, which is conducting current for two pulsed inverters back to the flip-flop output, may serve as a coupling connection between the two pulsed inverters and produce ringing. This ringing may produce a positive pulse of the emitter of the other inverter, thus turning it on at the wrong time. To avoid this, each emitter must be driven by a separate wire, unless the distance is very short.

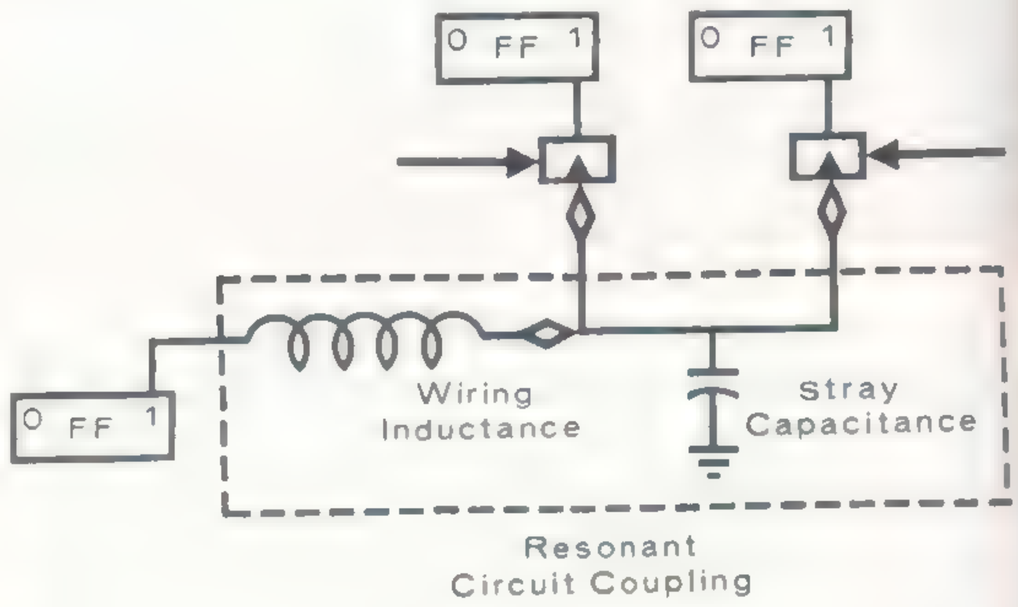
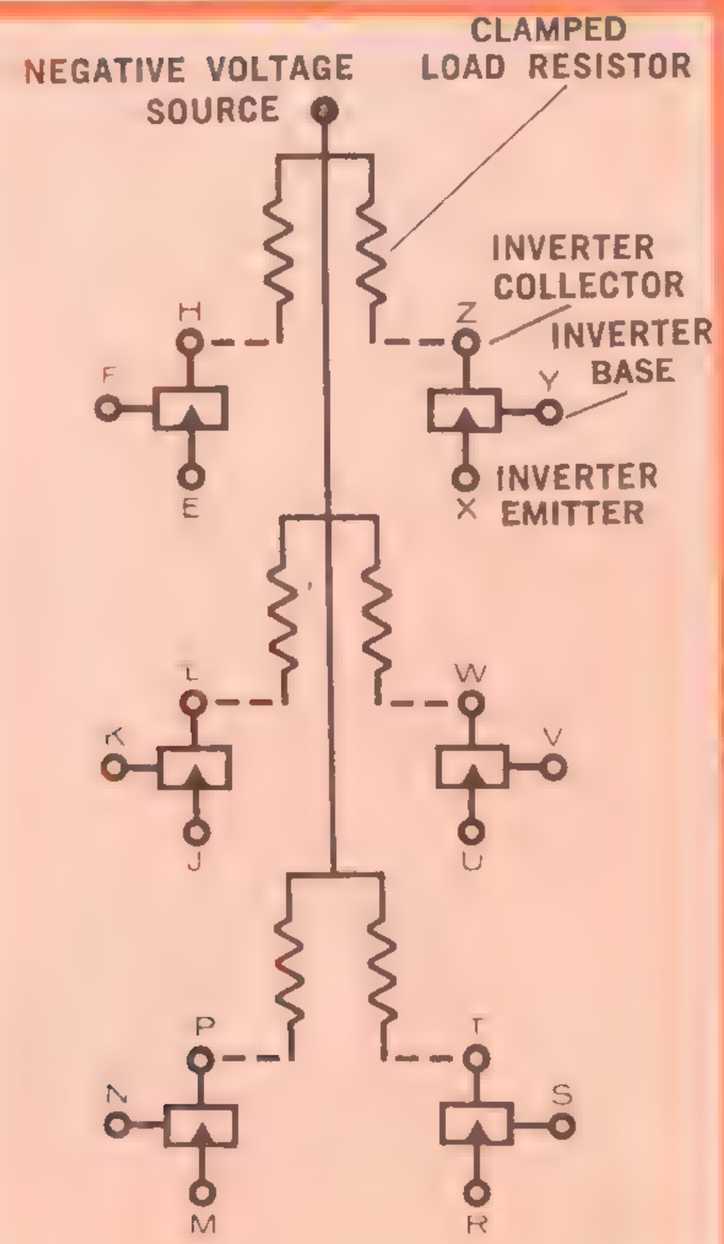


Figure 4

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6106
INVERTERS



The Type 6106 contains six inverters, each with a clamped load resistor which may be internally jumpered to the inverter collector, if desired. Each inverter is analogous to a switch. If —3 volts is applied to a base input, a conducting path is established between the emitter and the collector. If the base is brought to ground, the emitter-collector path is open. Delay through each inverter is approximately 12 nanoseconds.

INPUT: Base — Inputs are DEC Standard 40 nanosecond Negative Pulses when the Inverter is used as a pulse gate at any frequency up to 10 megacycles (1 unit of Pulse Load). Inputs are DEC Standard Levels or equivalent when the inverter is used as a level gate (1 unit of Base Load). Emitter — The inputs are DEC Standard Levels or equivalent, including grounding if emitter gating is not desired. If the collector is connected directly or through another inverter to a clamped load resistor, this input represents 1 unit of DC Emitter Load. If an emitter-collector path to a pulse gate exists, this input represents 1 unit of Pulsed Emitter Load.

OUTPUT: The collector may be connected directly to a clamped load resistor, to the emitter of another inverter, or to the gated input terminal of the flip-flop or other unit being pulsed. When used as a level gate, a collector connected to a load resistor can drive 2 units of Base Load at 10 megacycles, or 7 units where speed is not a problem. A collector can be connected to several emitters simultaneously, providing not more than one of the inverters is conducting at a time. No more than two level gates can be connected in series. When a flip-flop drives the emitter of the first gate in the series string, the flip-flop must be counted as one of the inverters. When one of the series-connected gates is used as a pulse gate, three gates may be connected in series. The pulse gate must be placed at the beginning of the string (the end farthest from the load).

POWER: —15 volts/82 ma; +10 volts (A)/0.5 ma; +10 volts (B)/0.5 ma.

INVERTER USAGE

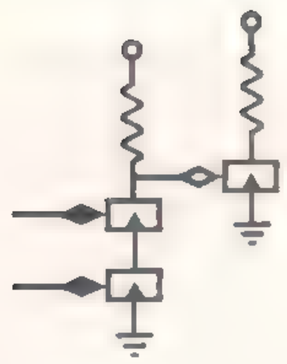


Figure 1

The high speed transistors used in 10 megacycle inverters have a larger saturation voltage drop than the transistors used in the 5 megacycle and 500 kilocycle inverters. Because of this slightly larger DC drop, a maximum of two inverters may be put in series if the output is to drive another inverter. (See Figure 1) If a flip-flop output is driving an inverter emitter, this flip-flop must be counted as an inverter. (See Figure 2)

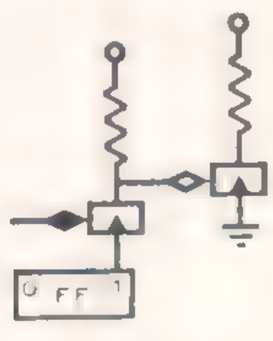


Figure 2

When the output of a series of transistor inverters is driving the input of a flip-flop or pulse amplifier, as in Figure 3, an inverter pulse gate may be added in series with the two level gates. This pulsed inverter must be placed at the bottom of the series string; that is, the end farthest from the load. The emitter may be driven by a flip-flop unless the sampling pulse is a P Pulse (the carry pulse in counters); in this case the emitter should be grounded.

Figure 3

When connecting 10 MC inverters, the user should avoid wiring inductance and stray capacitance as much as possible. Figure 4 illustrates how a wire, which is conducting current for two pulsed inverters back to the flip-flop output, may serve as a coupling connection between the two pulsed inverters and produce ringing. This ringing may produce a positive pulse of the emitter of the other inverter, thus turning it on at the wrong time. To avoid this, each emitter must be driven by a separate wire, unless the distance is very short.

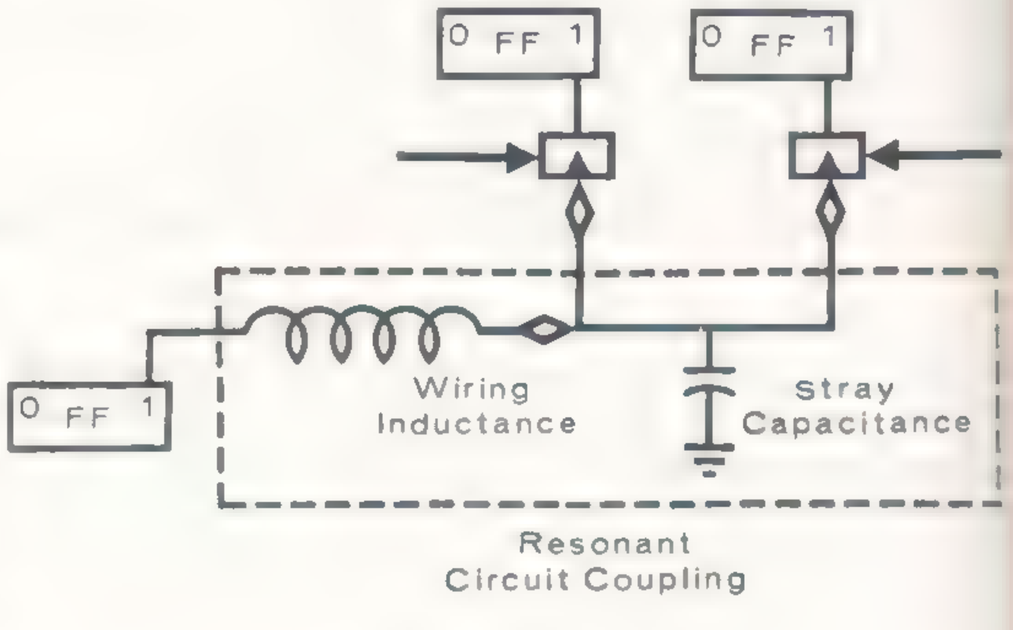
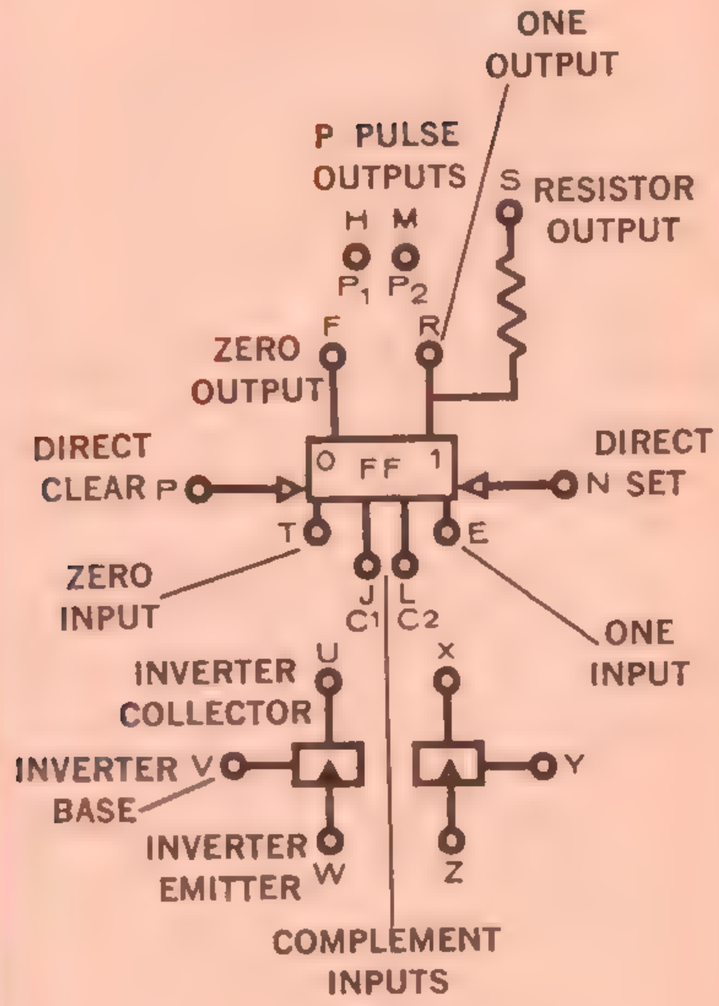


Figure 4

digital

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6202
FLIP-FLOP



The Type 6202 contains one flip-flop with built-in output amplifiers, direct and gated inputs to the ZERO and ONE sides and two independent gated Complement inputs with Carry pulse outputs. The package also contains two transistor inverters for use as pulse or level gates. The output signals have built-in delays so that they can be sensed reliably at the same time that the input is being pulsed. This general purpose flip-flop is useful in counter, shift register and adder applications.

INPUT: Direct Clear and Direct Set require DEC 40 nanosecond 2.5 volt Positive Pulses (1 unit of Pulse Load). Gated Clear and Gated Set signals must come from one or more collectors of Pulse Gates. Gated Complement (C_1 and C_2) signals must come from one or more collectors of pulse gates. The above signals can occur in any sequence, at any frequency and at any time intervals which have a minimum of 100 nanoseconds between any two signals (maximum frequency of 10 megacycles).The two inverters are similar to those included in DEC=Inverters 5101 and 6105.

OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving at 10 megacycles, up to 6 loads each of which may be a Base or Emitter Load. There can be only one unit of DC Emitter Load, and only one unit of pulsed emitter load may be pulsed at a time. At lower frequencies each output may simultaneously drive: (a) 14 units of Base Load; (b) 1 unit of DC Emitter Load; (c) any number of Pulsed Emitter Loads providing not more than one is pulsed at a time. A resistor-coupled output suitable for driving a transistor indicator amplifier is available.

PULSE OUTPUT: Each time the Complement terminal is pulsed, a DEC Standard 40 nanosecond Negative Pulse will occur on the P terminal. This pulse is capable of driving one inverter base; however, the inverter emitter must be permanently grounded. The P Pulse will be delayed by approximately 15 nanoseconds with respect to the signal on the base of the input inverter.

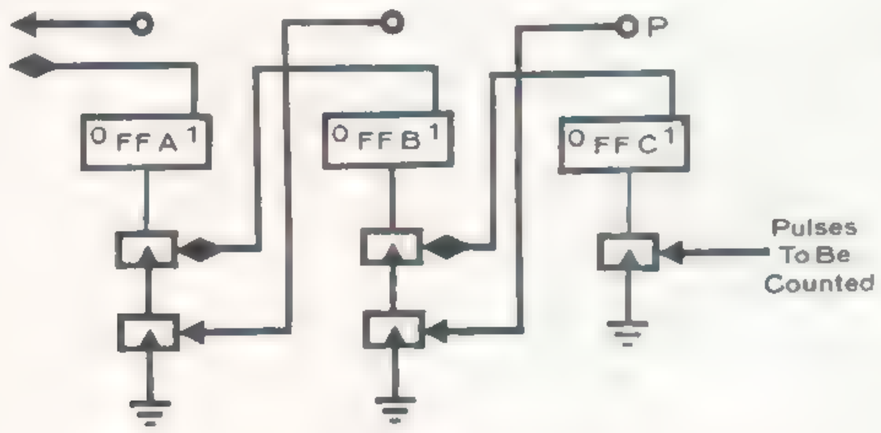
POWER: −15 volts/85 ma; +10 volts (A)/1.4 ma; +10 volts (B)/1.4 ma.

BINARY COUNTER

A typical counter arrangement using DEC Complementing Flip-flops is shown above. The pulses being counted enter on the right. They always complement flip-flop C and generate a standard pulse at P. This P Pulse complements flip-flop B when flip-flop C holds a ONE. When this P Pulse gets through the gate and actually complements B, it will generate a P Pulse out of B. The process is continued down the length of the counter.

The series connection of P Pulses and gates forms a high-speed carry chain. The carry propagate time per digit (15 nanoseconds) is much less than the flip-flop's total transition time.

To assure that flip-flop C will not be in the process of changing state while flip-flop B is receiving its carry pulse, a delay has been built into each flip-flop package. This insures that the ONE and ZERO output terminals will not change until after the carry pulse has been gated.



COUNTING SEQUENCE

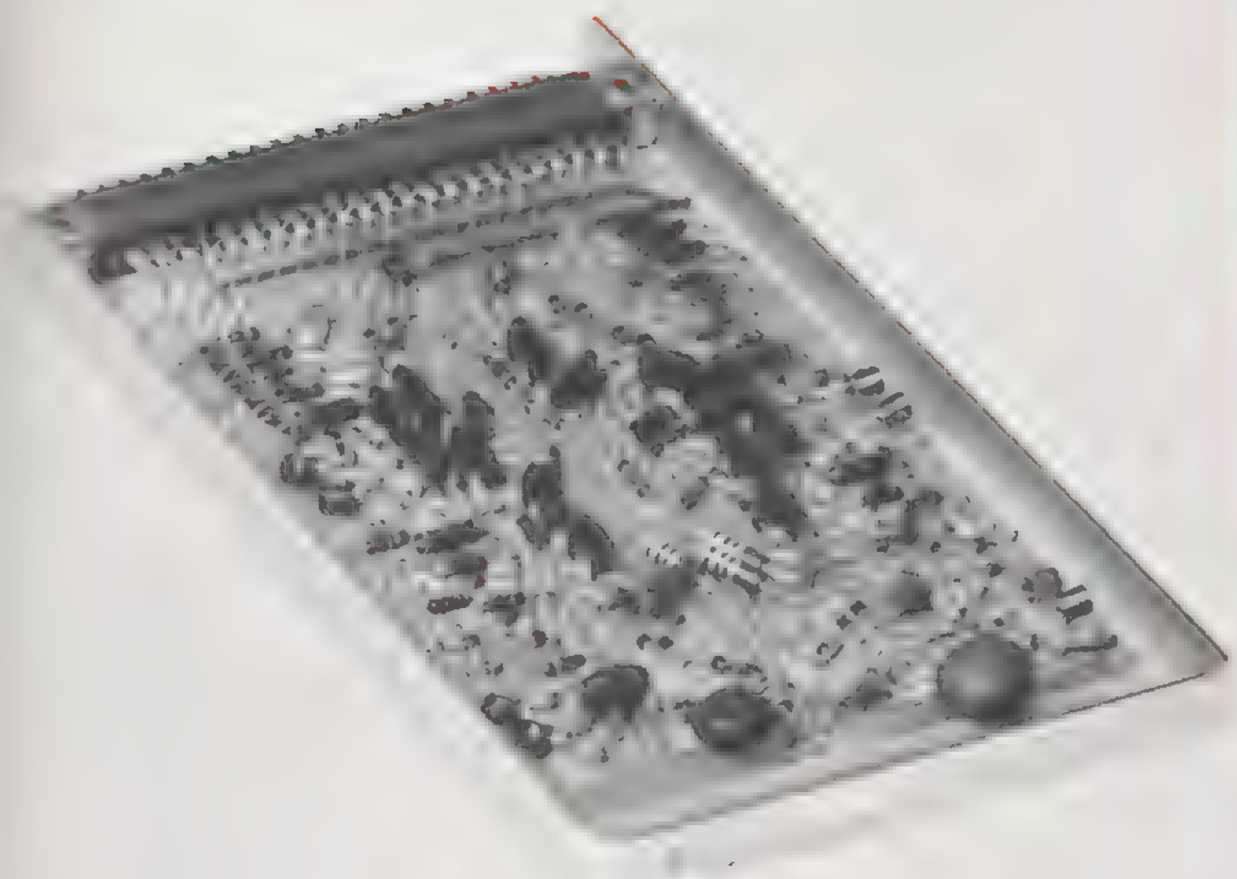
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

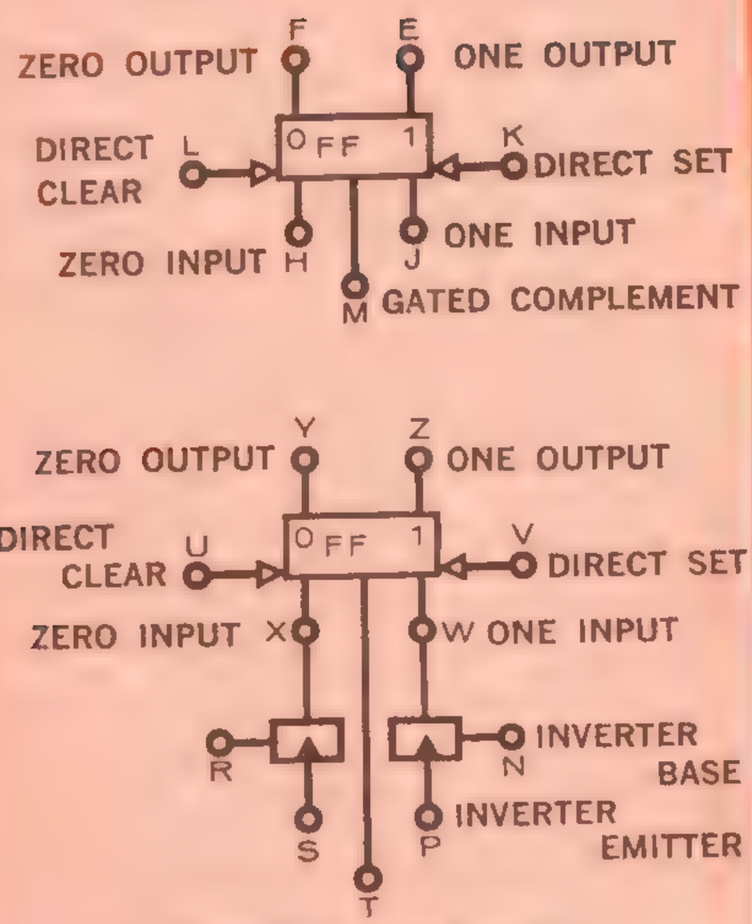
Figure 1 — BINARY COUNTER

digital

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6208
DUAL FLIP-FLOP





The Type 6208 contains two flip-flops with built-in output amplifiers. Both flip-flops have direct and gated inputs to the ZERO and ONE sides. Flip-flop A has a gated complement input. Flip-flop B has a direct complement input and also has pulse gates, internally connected to the gated ZERO and ONE inputs. The output signals have built-in delays so that they can be sensed reliably at the same time that the input is being pulsed.

INPUT: Direct inputs (Pins K, L, T, U, and V) require DEC 40 nanosecond 2.5 volt Positive Pulses (1 unit of Pulse Load, except T, which is 3 units Pulse Load). Gated inputs (Pins H, J, M, X, and W) must come from one or more collectors of pulse gates. The above signals can occur in any sequence at any frequency and at any time intervals which have a minimum of 100 nanoseconds between any two signals. (Maximum frequency of 10 megacycles.) The two inverters are similar to those included in DEC Inverters 5101 and 6105.

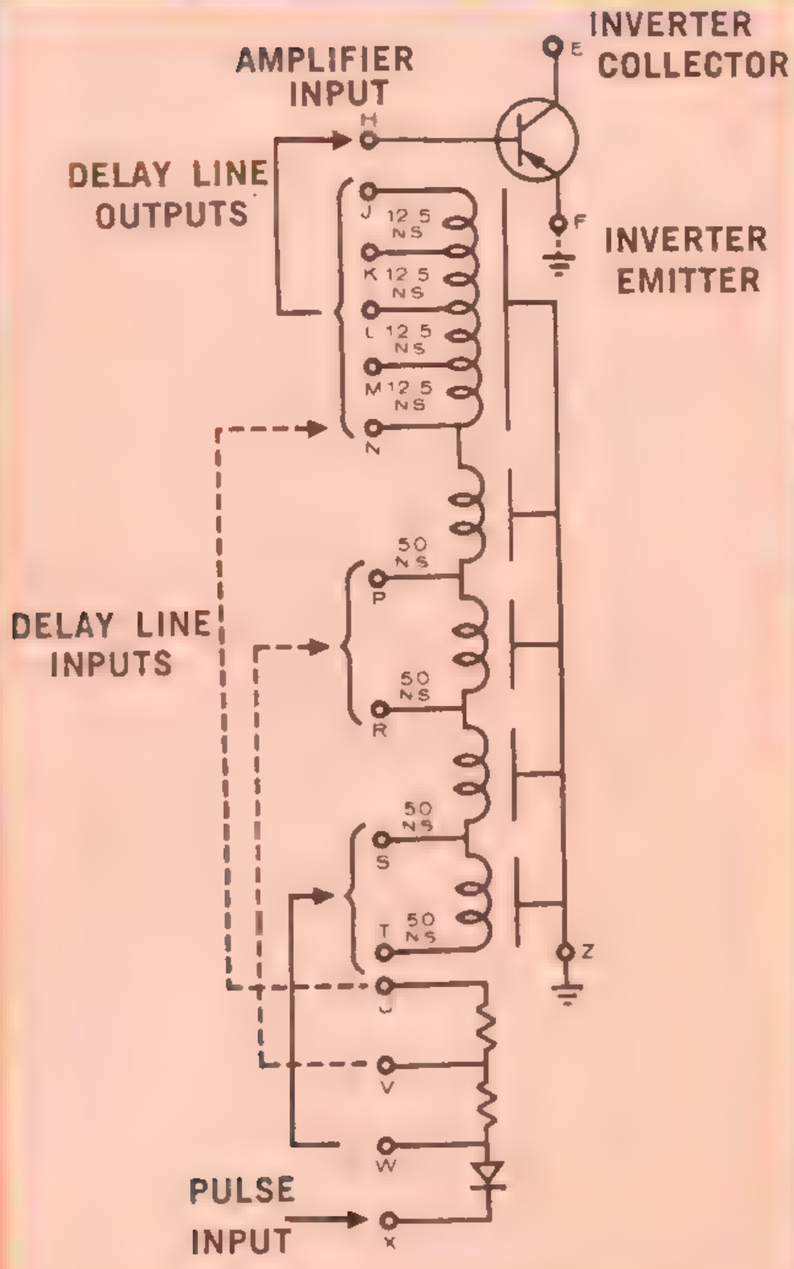
OUTPUT: ZERO output and ONE output provide DEC Standard Levels each capable of simultaneously driving, at 10 megacycles, up to 6 loads each of which may be a Base or Emitter Load. There can be only one unit of DC Emitter Load, and only one of the emitters may be pulsed at a time. At lower frequencies each output may simultaneously drive: a) 14 units of base load; b) 1 unit of DC Emitter Load; and c) any number of Pulsed Emitter Loads providing not more than one is pulsed at a time.

POWER: −15 volts/170 ma; +10 volts (A)/2.8 ma; +10 volts (B)/2.8 ma.

digital

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6310
DELAY LINE



The Type 6310 produces delays up to 0.25 microsecond in steps of 12.5 nanoseconds. A transistor amplifier is built into the package. Its input, not being a standard inverter, must be driven by the delay line. The 15 nanosecond delay of the inverter must be added to the total delay time. Controls: the input pulse is applied to pin X, and the input of the delay line (pins N through T) is connected to pin V, as shown. The output of the delay line (pin J through N) is connected to the base of the output inverter, pin H.

INPUT: The input should be a DEC Standard 40 nanosecond Negative Pulse or its equivalent (2 units of Pulse Load).

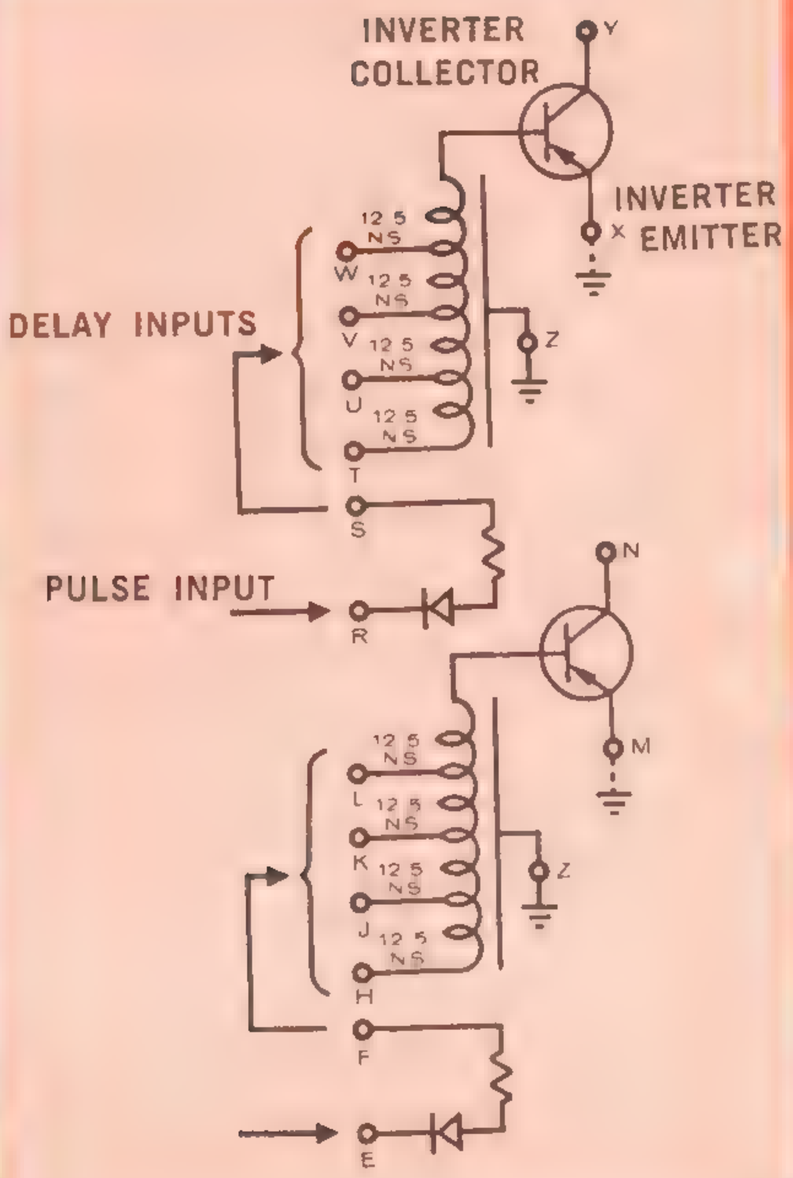
OUTPUT: The emitter of the output inverter must be grounded; the transistor's collector should be connected to the input of a DEC Pulse Amplifier Type 6603 or other unit being pulsed. However, if additional logic gating is required, it may be done with up to two transistor inverters placed in series between the collector and the pulse amplifier.

POWER: −15 volts/0 ma; +10 volts (A)/2.1 ma; +10 volts (B)/0 ma.

digital

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6311
DELAY LINE



The Type 6311 contains two delay lines. Each line produces a maximum of 50 nanoseconds delay in 12.5 nanosecond steps. The output of each of the delay lines is connected to a transistor inverter. The collector terminal is available for logical gating. The 15 nanosecond delay through the inverter must be added to the delay of the line. Controls: the inputs are applied at pin R (or E) and the desired delay is obtained by connecting S (or F) to one of the delay line taps.

INPUT: The input should be a DEC Standard 40 nanosecond Negative Pulse or its equivalent (1 unit of Pulse Load).

OUTPUT: The emitter of the output inverter must be grounded; the transistor's collector should be connected to the input of a DEC Pulse Amplifier Type 6603 or other unit being pulsed. However, if additional logic gating is required, it may be done with up to two transistor inverters placed in series between the collector and the pulse amplifier.

POWER: −15 volts/0 ma; +10 volts (A)/1.0 ma; +10 volts (B)/1.0 ma.

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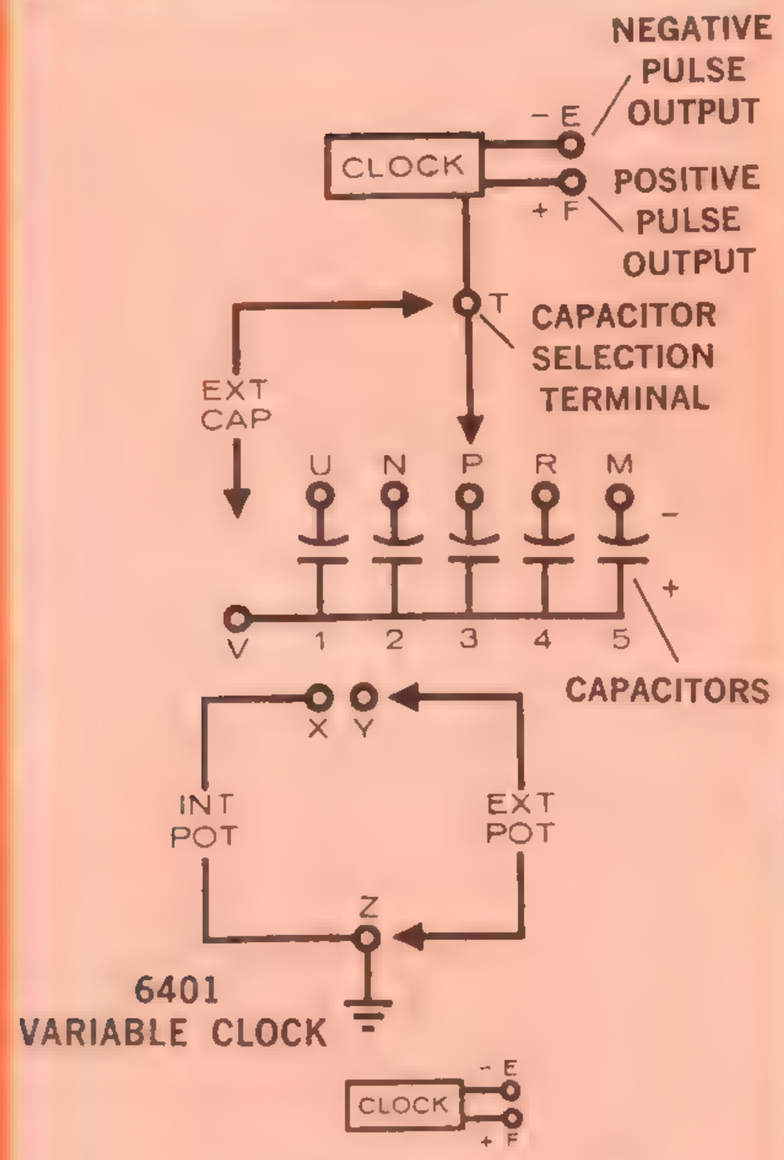
6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6401-6403
CLOCKS



The DEC Variable Clock Type 6401 produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies available. The variable clock is often used as a primary source of timing for large systems. Where very precise timing is needed, the Type 6403 Crystal Clock, which contains a single-frequency crystal oscillator may be used.

The frequency of the Type 6401 is variable from 250 cycles/second to 10 megacycles. Five capacitors determine the frequency range and a potentiometer provides fine control. For lower frequencies, an external capacitor may be used. If terminals X and Y are connected together, the internal 20,000 ohm potentiometer will provide the fine control. If desired, an external potentiometer can be connected between terminals Y and Z.

The Type 6403 contains a series resonant crystal oscillator circuit and two pulse shaping buffer amplifiers which produce DEC Standard 40 nanosecond Pulses. The frequency, specified by the customer, may be between 5 and 10 megacycles. The frequency is stamped on the crystal in the plug-in unit. Stability is 0.01% over the temperature range of −20 to +55° C.

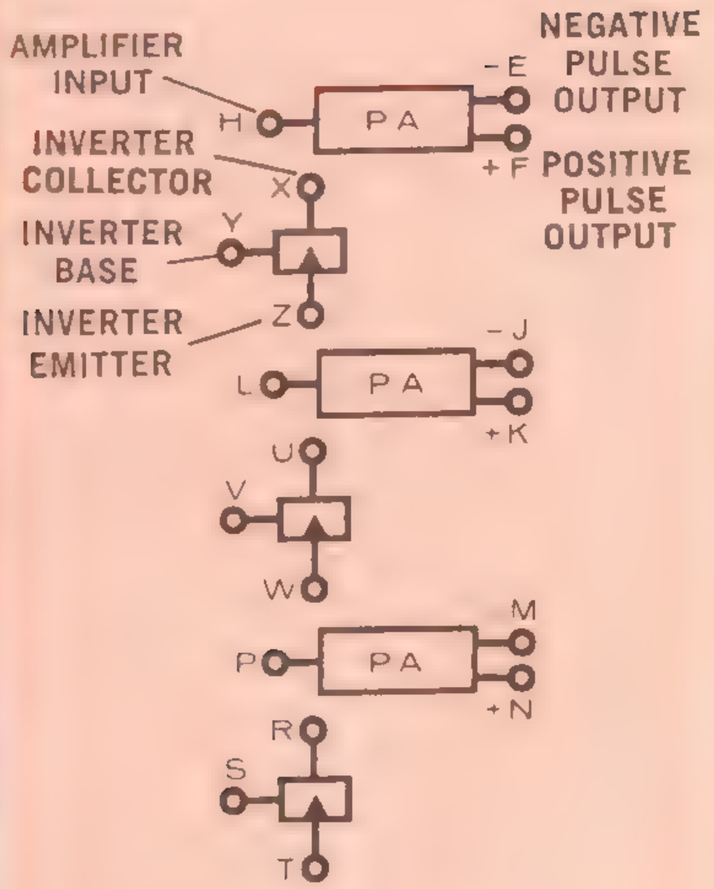
OUTPUT: DEC Standard 40 nanosecond Pulses will appear at the output at the preselected frequency. The output pulse will be negative if the positive output terminal is grounded; it will be positive if the negative output terminal is grounded. Each output is capable of driving 8 units of Pulse Load.

POWER: Type 6401: −15 volts/185 ma; +10 volts/0 ma; +10 volts/0 ma. Type 6403: −15 volts/60 ma; +10 volts/0 ma; +10 volts/0 ma.

digital

6000 SERIES
SYSTEM MODULES
10 MEGACYCLES

6603
PULSE AMPLIFIER



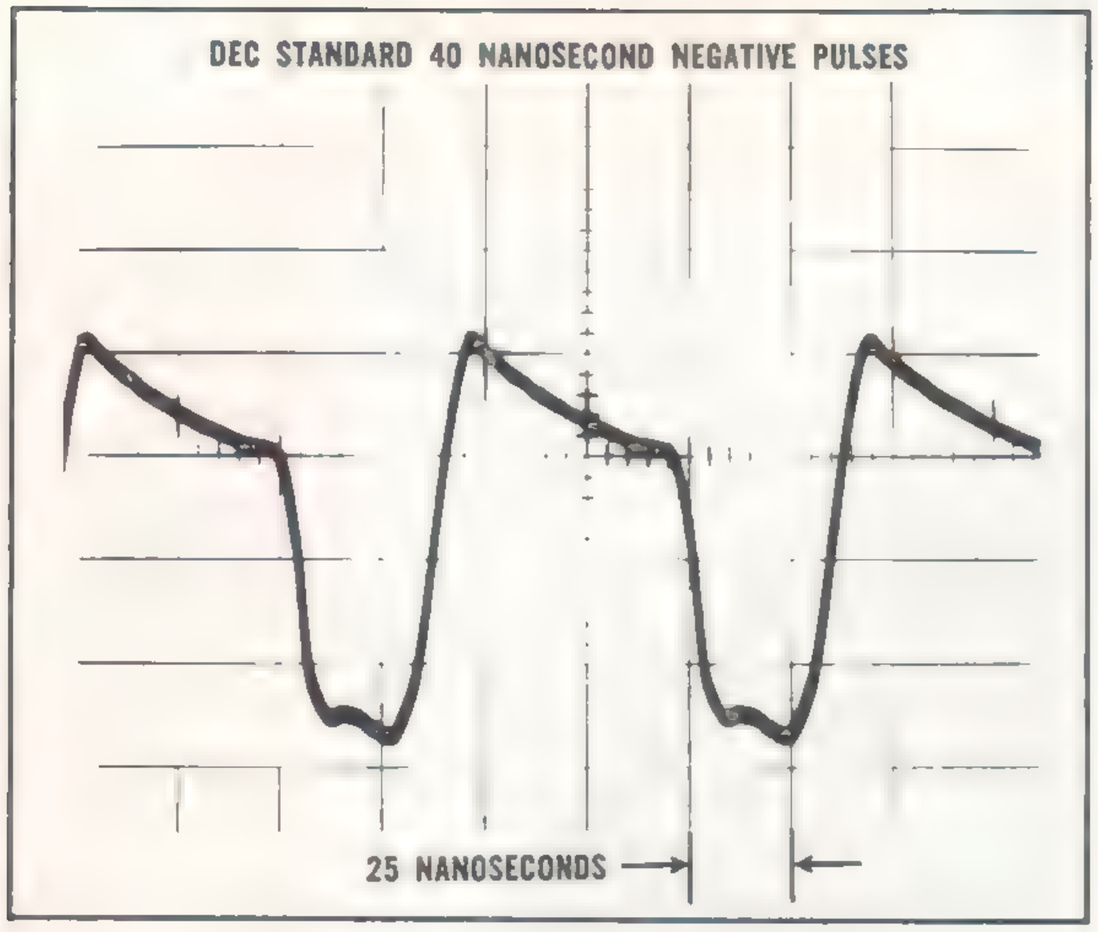
The Type 6603 contains three pulse amplifiers which are used for power amplification and for standardizing pulses in amplitude and width. Three inverters are available for gating input levels or for mixing pulses. Delay through the pulse amplifier is approximately 25 nanoseconds. Input pulses may occur at any frequency up to 10 megacycles.

INPUT: The input to the base of the inverter whose collector drives the pulse amplifier is normally a DEC Standard 40 nanosecond Negative Pulse. However, any negative pulse having an amplitude between 2.0 and 5.0 volts, leading edge less than 25 nanoseconds and width (at 2 volts) greater than 25 nanoseconds, can be used. Input pulses of less than —0.5 volts will not generate an output pulse.

Many pulse gate collectors can be connected together to mix pulse sources. The two pulse gates are inverters like those included in the DEC Inverter Types 5101 and 6105.

OUTPUT: The output is a DEC Standard 2.5 volt 40 nanosecond Pulse which occurs at the output every time the input signal meets the input requirement. The output will be negative if the positive output terminal is grounded; it will be positive if the negative terminal is grounded. Each output is capable of driving 12 units of Pulse Load.

POWER: —15 volts/91 ma; +10 volts (A)/0.3 ma; +10 volts (B)/0.2 ma.


DEC STANDARD 40 NANOSECOND NEGATIVE PULSES
25 NANOSECONDS

Digital offers a wide selection of Module Accessories to meet varied requirements

DEC Module Accessories are designed to provide maximum flexibility in the use of Laboratory and System Modules in various digital applications. Like the modules themselves, many of the accessory items may be repeatedly incorporated in entirely different set-ups without modifications of any kind.

Ten types of power supplies are standard Digital catalog items. The most universal of these units is the Type 722, which provides all DEC Standard Voltages and drives approximately 45 modules. Also available is a selection of single and dual supplies for use with System Modules. Most of these units have floating outputs, and they can be connected in series to provide higher output voltages for driving special circuits.

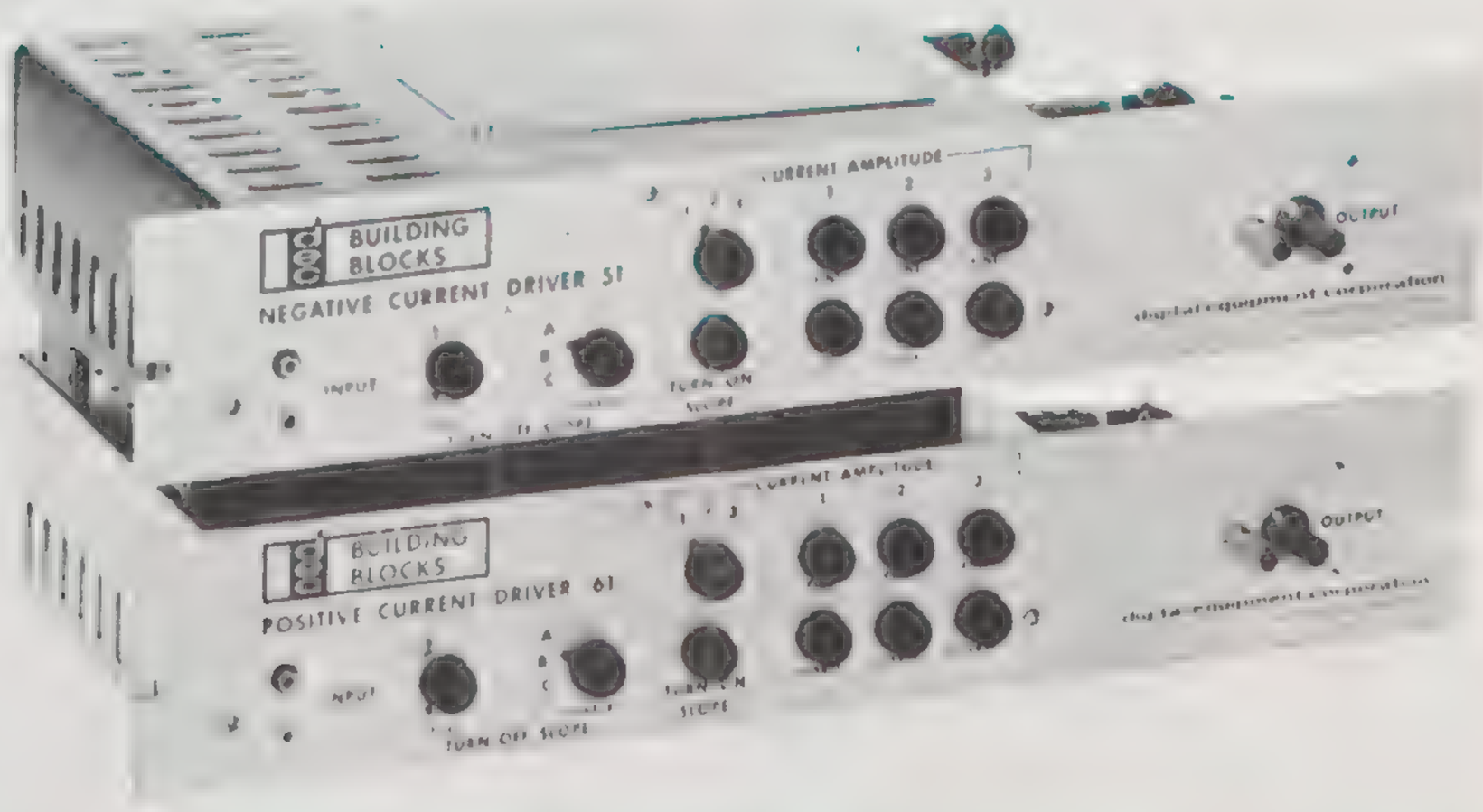
Types 730 and 734 are metered, variable-voltage supplies for marginal checking of Digital Modules. The Type 765 is a bench power supply with four variable voltages for testing modules. Types 749 and 766 are used with current drivers Types 51-61 and 52-62 respectively.

There are two basic kinds of mounting panels. The Type 901 is the standard Laboratory Module panel. It accommodates up to nine modules, and it has back-panel plugs which make the power connections automatically when modules are inserted.

Mounting panels for System Modules come in a variety of sizes, packing densities and connector options. Standard lengths are 19, 24 and 30 inches, accommodating from 20 to 43 modules. Special 17-inch panels may also be ordered for mounting on plenum doors. The standard connector is a coded, solder-type pin connector. Other connector options are taper pin, patch cord and wire wrap. Modules may be removed from any of these mounting panels without disturbing the logical wiring.

Digital also offers a number of useful "convenience items" in the accessory lines. Test power cables and module extenders allow ready access to the module circuitry. Assembled and unassembled blank modules permit the development of special circuits. Cover plates are used to cover front panel wiring, and blank panels are available for mounting accessories such as switches and to fill unused space.

Special purpose accessories include high current pulse equipment items — vacuum tube and solid state negative and positive current drivers, current calibrators, and associated power supplies and panels. This equipment is used in testing ferrite magnetic cores, films and memories.



The DEC Types 51 and 61 Negative and Positive Current Drivers provide convenient sources of current pulses for testing digital equipment which requires significant drive currents. The width and pattern of current pulses is determined by external logic carried out with DEC Digital Modules or equivalent. DEC Current Drivers can be used in parallel to provide both polarities of pulses.

Type 51 Negative Current Driver

OUTPUT CURRENT: 15-1000 ma, 250 ma maximum average.

TURN-ON TIME: 0.1-1.6 μsec, at 1000 ma, 0.07-0.7 μsec, at 50 ma.

TURN-OFF TIME: 0.1-0.5 μsec, at 1000 ma, 0.07-0.5 μsec, at 50 ma.

OUTPUT IMPEDANCE: Typical values are 1000 ohms at 1000 ma, and 2500 ohms at 100 ma.

BACK VOLTAGE: Plus or minus 50 volts.

SCREEN GRID PROTECTION: When output terminals are open, screen grids of output tubes are automatically protected from over dissipation.

AMPLITUDE CONTROLS: (1) 3 pairs of Slice and Fine amplitude controls, each of which may be preset to any current level. The Slice control clips the grid swing of the output amplifier, while the Fine control is a variable cathode resistor in the output amplifier. (2) A 3-position switch for the selection of one of the above pairs of amplitude controls.

POWER: +130 volts/44 ma; −135 volts/5-230 ma; −285 volts/20-65 ma; 6.3 volts AC/6.2 amps. One DEC Type 749 Power Supply is required for each Current Driver, and provides regulation for the filaments as well as the d-c voltages.

Type 61 Positive Current Driver

OUTPUT CURRENT: 60-1000 ma, 250 ma maximum average.

TURN-ON TIME: 0.1-1.0 μsec.

TURN-OFF TIME: 0.07-0.5 μsec, at 1000 ma 0.3-0.5 μsec, at 100 ma.

OUTPUT IMPEDANCE: Typical values are 80 ohms at 1000 ma, 200 ohms at 500 ma, 500 ohms at 250 ma, 1100 ohms at 100 ma.

BACK VOLTAGE: Plus or minus 20 volts.

SCREEN GRID PROTECTION: None needed; output tubes are cathode-follower connected.

AMPLITUDE CONTROLS: (1) 3 pair of Coarse and Fine amplitude controls, each of which may be preset to any current level. (2) A 3-position switch for the selection of one of the above pairs of amplitude controls.

POWER: +135 volts/5-300 ma; −130 volts/17 ma; −150 volts/14-60 ma; 6.3 volts AC/6.2 amps. One DEC Type 749 Power Supply is required for each Current Driver, and provides regulation for the filaments as well as the d-c voltages.

Types 51 and 61 Current Drivers

DUTY FACTOR: 50% maximum for pulse currents of 500 ma or less. Limited by maximum average current of 250 ma at higher pulse amplitudes.

PULSE REPETITION FREQUENCY: Up to 1 megacycle.

INPUT SIGNAL: Requires a 3-volt negative gate for the duration of the pulse, such as is provided by the output of a DEC Type 302 Delay or the output of any DEC Flip-flop. The load is 1 unit of Base Load.

RISE AND FALL TIME CONTROLS: Turn On Slope to control turn-on time. Turn Off Slope to provide a Fine control and a 3-position Coarse control over turn-off time.

OUTPUT TERMINALS: One pair of terminals, one side of which is ground. Output may be paralleled with other Type 51 or Type 61 Current Drivers.

TUBE COMPLEMENT: (2) dual, pentode-triodes 6BA8A; (2) output amplifiers 6DQ5.

PHYSICAL SIZE: DEC Current Drivers measure 3½ x 19 x 8 inches. The Power Supply Type 749 measures 5¼ x 19 x 10 inches.

digital

MODULE ACCESSORIES

52-62
CURRENT DRIVERS

The DEC Types 52 Negative and 62 Positive solid-state Current Drivers provide shape-controlled, constant current pulses of up to 1 amp to variable loads. DEC Logic Modules, used in conjunction with these current drivers, generate complex current pulse sequences for thorough evaluation of magnetic memory core characteristics under all operating conditions. The high impedance output of the driver ensures a fixed driving current even during changing back voltage.

The circuit, similar for negative and positive drivers, can be considered in two parts. The first part generates a trapezoidal control voltage, and the second converts the control voltage to an output current. The duration of the current corresponds to the duration of the input signal. Linear rise and fall slopes are generated by a Milier integrator. The current for charging the integrating capacitor is fixed, but the discharge current may be varied to establish a symmetrical control voltage. High speed transistors with high power and voltage ratings convert the trapezoidal control voltage to a trapezoidal output current pulse.

Controls: coarse and fine amplitude controls, on concentric shafts, permit the pulse current to be set between 50 ma and 1 ampere (with a maximum average output current of ¼ ampere). Coarse and fine slope controls establish the duration of the linear current rise, variable from 50 nanoseconds to 1 microsecond over the full range of output currents. The fall trim control adjusts the duration of the linear current fall ±10% so that it can be made equal to the rise time.

INPUT: Ground produces no output; a −3 volt level input produces an output pulse of the same duration as the input. The load is 1 unit of 5 megacycle Base Load. The maximum repetition rate is 2 megacycles. Input connections may be made on the front or rear panel of current drivers with DEC Type 911 Patch Cords.

OUTPUT: 50 ma to 1 ampere current pulses with linear rise and fall are generated for back voltages up to 50 volts (20 volts if no extra supplies boost the output of the DEC Type 766 Power Supply). The mini-

mum output impedance is 5000 ohms at 1 ampere current; it is considerably higher at lower currents. Droop and overshot are less than 1%. Amplitude jitter is less than 0.1%. The nominal temperature coefficient of the output current is 0.02%/°C. The duty factor is limited to 50% for pulse currents up to 500 ma; at higher pulse amplitudes it is limited by the maximum average output current rating of 250 ma.

Output terminals are binding posts on ¾" centers which accept double banana plugs. Positive and negative drivers may be paralleled in any combination for pulse mixing or to obtain higher currents.

DIMENSIONS: Up to six current drivers (2½" wide x 10½" high x 10½" deep) or four drivers and one current/voltage calibrator fit into one DEC Type 1913 19" mounting panel. The power cord is 8 ft. long.

POWER:* Type 52: +35 volts DC/0.2 ma; −35 volts DC/253 ma + average output current; −45 volts DC/96 ma. **Type 62:** +45 volts DC/75 ma; +35 volts DC/275 ma + average output current; −35 volts DC/9.5 ma.

*These data apply for drivers operating from a DEC Type 766 Power Supply. Supplies used to provide additional back voltage supply only the average output pulse current.

71
CURRENT/VOLTAGE CALIBRATOR

The Type 71 Calibrator provides high accuracy measurement of current and voltage pulses, which makes it an ideal companion for the Types 52 and 62 solid-state or the Types 51 and 61 vacuum-tube current drivers. The calibrator generates a precise reference voltage using a two-stage Zener regulated voltage supply and a resistive divider with very low temperature coefficients and high setting resolution. A ten-turn potentiometer with ±0.05% non-linearity controls the amplitude. A linearity tape supplied by the manufacturer, along with measurements of end resistance, is used in calibration to insure rated accuracy.

To superimpose the reference and input wave forms for output to a display oscilloscope, two mercury-wetted contact relay choppers provide commutation between the reference voltage, the input signal, and ground. Four metal film, 2 ohm, ±0.2% resistors with temperature coefficient of less than ±25 parts per million/°C, with four General Radio Type 274 MB banana plugs, are supplied with each Type 71. Two such resistors in parallel provide a scale factor of one for direct readings up to 1 ampere. One resistor allows increased sensitivity in the 0-500 ma range.

Controls: The on-off switch controls the internal power supply to the reference voltage and the time-sharing chopper circuit. The output shows the input when this switch is off. The reference control sets the magnitude, and the polarity switch determines the polarity of the reference level. The reference control dial is calibrated in increments of 1 mv (from zero) to 1 volt. The dwell control apportions the display time between the input signal, ground, and reference voltage traces, which permits control of their relative brightness.

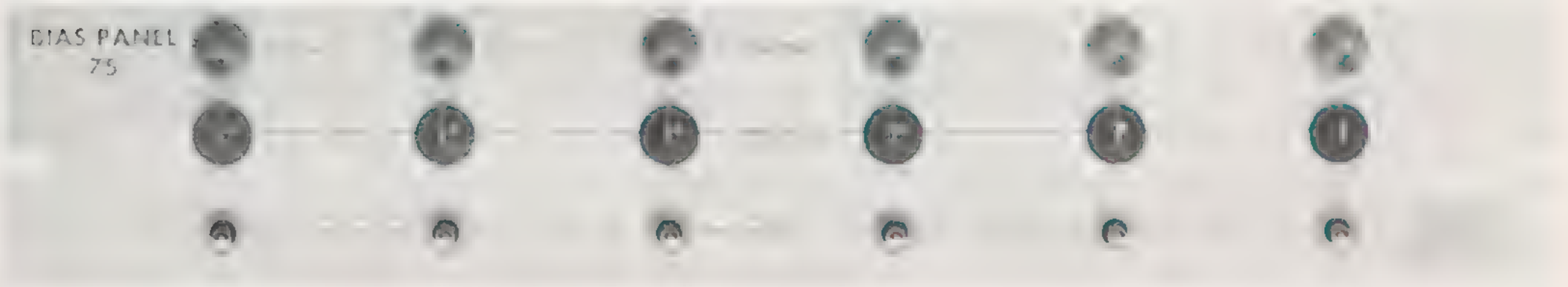
The input selector switch connects one of the four input terminals to the time-sharing commutator. The match control provides compensation for stray reactances by adjusting the series resistance of the signal path to the scope. (Consult the Applications note on transmission of High Current Pulses.)

INPUT: Four pair of input binding posts are provided with standard ¾" spacing. The input voltage range is between −1 volt and +1 volt.

OUTPUT: A standard UHF female connector and a grounded binding post are the output terminals. The output impedance of the reference voltage source is 1000 ohms/volt. Error is limited to within ±0.07%, ±0.8 mv for all amplitudes of the reference voltage at 25°C. The temperature coefficient of the reference voltage at 1 volt is within ±50 parts per million/°C within the operating range, 0°C to 50°C.

POWER: The input power is less than 15 watts at 115 volts AC. The plug on the back panel is a standard three-prong grounded plug.

75
BIAS PANEL



The Type 75 is a 19″ x 3½″ panel, with six switches and six rheostats for supplying a small, adjustable amount of DC bias current to systems using Current Drivers Types 52 and 62. The principal use of the Type 75 Bias Panel is to balance out small leakage currents from current drivers in the exceptional cases where such leakages materially affect measurements.

Six identical circuits are housed in the bias panel. Each circuit has a resistance that can be adjusted to from 15,000 ohms to 265,000 ohms nominal. A switch allows a voltage of ±45 volts from a Type 766, 769, or 776 Power Supplies to be applied to the variable resistance. Thus each output terminal can deliver a small current of either polarity to ground, adjustable from 3 ma down to 0.2 ma. (If booster voltage supplies are used with the Type 766, 769, or 776 Power Supply, the increased voltage is applied to the Type 75 Bias Panel, increasing the bias current accordingly.)

An Amphenol plug of the type used on solid-state current drivers and the Type 766, 769, and 776 Power Supplies is provided for power connection at the rear.

710
POWER SUPPLY

The Type 710 unit is a 10 volt, 0.5 ampere floating power supply to be mounted on a standard 19-inch rack. Output voltage is regulated by a zener diode.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts

OUTPUT CURRENT: 0.5 amperes

TOTAL UNIT REGULATION: Output voltage stays within 9.5 to 10.5 volts when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC.

P-P RIPPLE $\leq$0.2 volts

LINE FREQUENCY REGULATION: 50-65 cycles

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 3½″

CHASSIS WIDTH BEHIND PANEL: 17⅛″

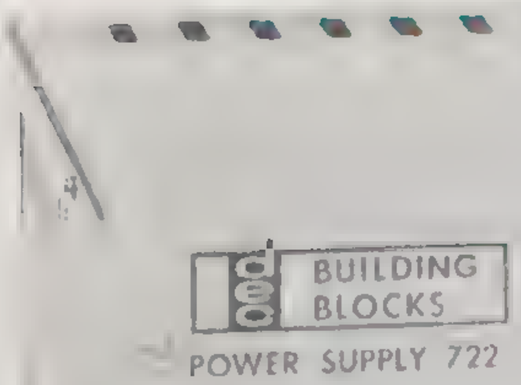
CHASSIS DEPTH BEHIND PANEL: 6″

CHASSIS HEIGHT BEHIND PANEL: 3 6/16″

FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket

POWER OUTPUT CONNECTION: DC: 10-32 screw terminals. AC: Amphenol 160-4 Socket. A power cable with a two-prong adapter is also furnished.



The Type 722 is a +10, −3, and −15 volt power supply designed for mounting in a standard 19-inch rack. A single resonant transformer, two full wave silicon rectifiers, filter capacitors, and a shunt diode regulator, give a simple rugged supply able to adequately withstand wide line and load variation for general system use. (Figure 1 is a simplified schematic of the supply.) The −3 volt output is obtained from a string of forward-biased silicon rectifiers which are fed from a 1.5 ampere bleeder that is connected to −15 volts. Any load on the −3 volt output up to the maximum of ±1.2 amperes will not affect the rest of the supply. The +10 volt and −15 volt load current ratings are interdependent, as shown in Figure 2.

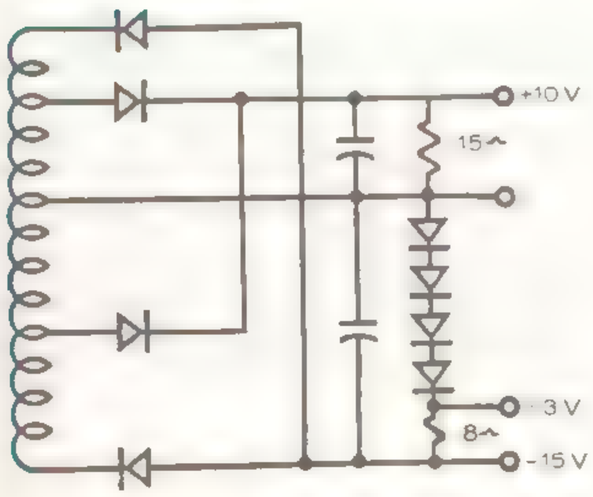


Figure 1

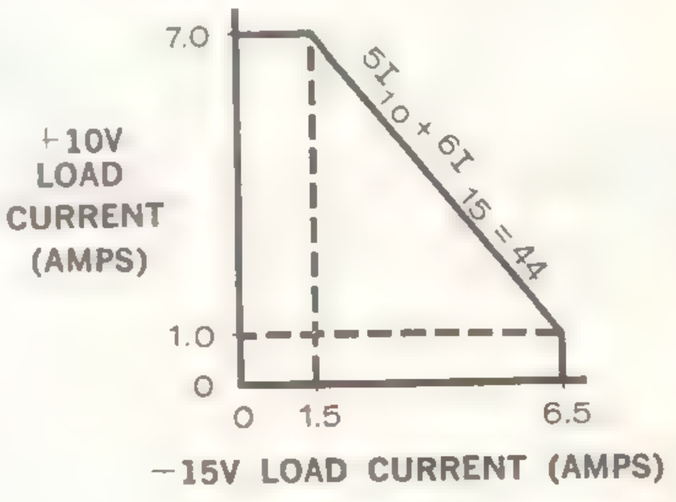


Figure 2

While the −15 volt output is delivering 6.5 amperes, the +10 output can deliver up to 1 ampere; and while the −15 volt output is delivering 0 to 1.5 amperes, the +10 output can deliver up to 7 amperes. When the −15 volt output current is between 1.5 and 6.5 amperes, the maximum +10 volt DC load current can be determined by the equation: $5I_{10} + 6I_{15} = 44$.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts; −3 volts; −15 volts DC

OUTPUT CURRENT: +10 volts: 0 to 7.0 amperes*
−3 volts: 0 to ±1.2 amperes
−15 volts: 0 to 6.5 amperes*

COMBINED LINE AND LOAD REGULATION: For all combinations of above loads and line between 105 and 125 volts AC.
−15 volts: −14.5 volts to −16 volts
−3 volts: −2.8 volts to −3.4 volts
+10 volts: 9.0 volts to 11 volts

P-P RIPPLE: 0.8 volts for +10 and −15 outputs and less than 15 mv for the −3 outputs

LINE FREQUENCY REGULATION: 60 ±0.5 cycles

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) \leq 44$

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19"

PANEL HEIGHT: 5¼"

CHASSIS WIDTH BEHIND PANEL: 17⅛"

CHASSIS DEPTH BEHIND PANEL: 9 15/16"

CHASSIS HEIGHT BEHIND PANEL: 5"

FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket

POWER OUTPUT CONNECTION: DC: Cinch Jones S-308F.D. socket that fits to DEC 750 Power Cable 110 AC: Amphenol 160-4 Socket. A power cable with two-prong adapter is also furnished.

TYPE 750 POWER CABLE

The Type 750 is a power cable for connecting the Type 722 Power Supply to the Laboratory Module Mounting Panel Type 901.

TYPE 1919 POWER CABLE

The Type 1919 Power Cable is used to connect the Type 722 Power Supply to a System Module mounting panel. The Type 1919 has a Jones plug on one end for connection to the power supply and spade lugs on the other end for connection to the System Module mounting panels.

728
POWER SUPPLY

The Type 728 (+10, −15 volt) Power Supply is a simple rugged supply capable of withstanding wide line and load variation for general system use. When used singly the 10-volt channel can supply 0 to 7.5 amperes, or the 15-volt channel can supply 1.0 to 8.5 amperes.

Figure 1 shows the permissible operating region when both outputs are used. While the −15 volt output is delivering 8 amperes, the +10 volt output can deliver up to 1 ampere; and while the −15 volt output is delivering 1 to 3 amperes, the +10 volt output can deliver up to 7 amperes. When the −15 volt output is delivering between 3 and 8 amperes, the maximum +10 volt

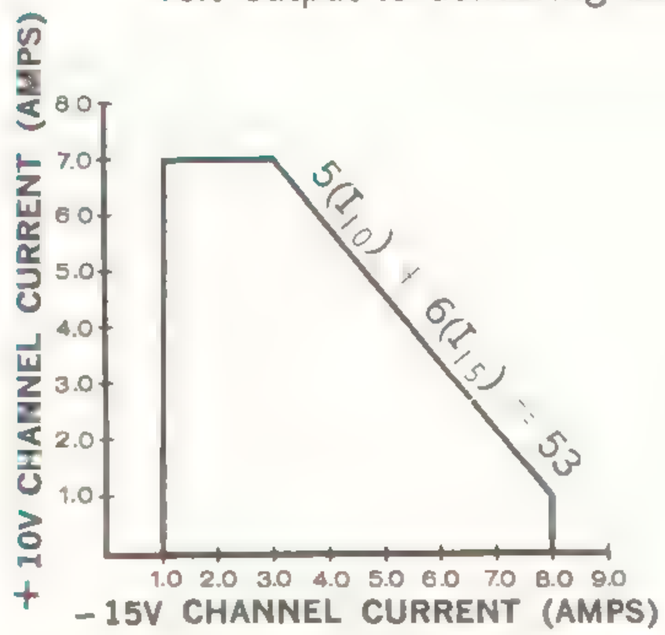


Figure 1 COMBINED LOAD OPERATING REGION

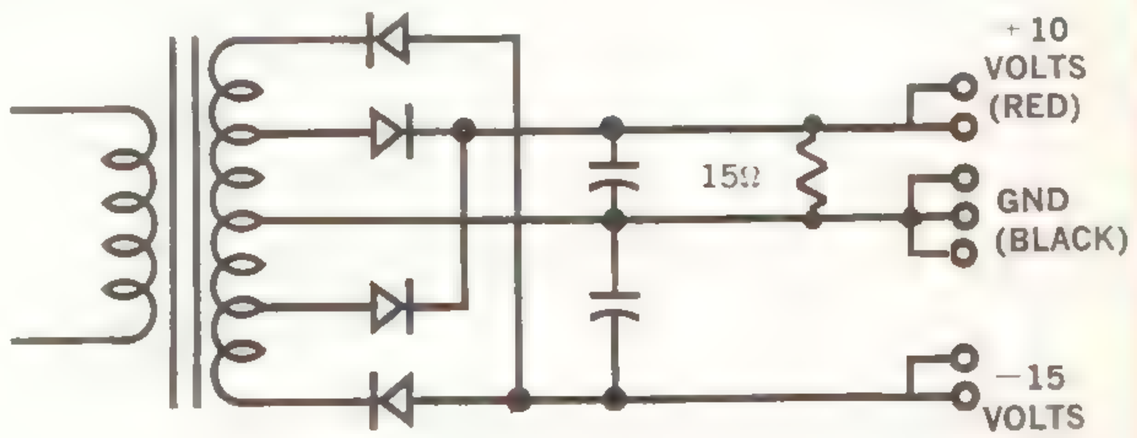


Figure 2 SCHEMATIC

current can be determined by the equation: $5(I_{10})+6(I_{15})=53$. Removing the 15-ohm shunt increases the 10 volt output by ⅔ ampere. (See Figure 2.)

The supply unit is designed for mounting on the plenum door of a DEC Computer Cabinet, but can also be mounted on a standard 19-inch rack with suitable adapter plates.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: +10 volts, −15 volts DC, floating

OUTPUT CURRENT: 1. When only one output is loaded: +10 volts: 0 to 7.5 amperes −15 volts: 1.0 to 8.5 amperes. 2. When both outputs are loaded: +10 volts: 0 to 7.0 amperes* −15 volts: 1.0 to 8.0 amperes*

LINE AND LOAD REGULATION: The output voltage remains between −14.5 to −16 volts for the −15 volt channel and within +9.5 to +11 volts for the +10 volt channel, when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC

P-P RIPPLE: less than 0.8 mv for +10v output
less than 0.6 mv for −15v output

LINE FREQUENCY REGULATION: 60 cycles ±0.5 cycle

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) = 53$. (See Figure 1.)

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16 ⅝"

PANEL HEIGHT: 8"

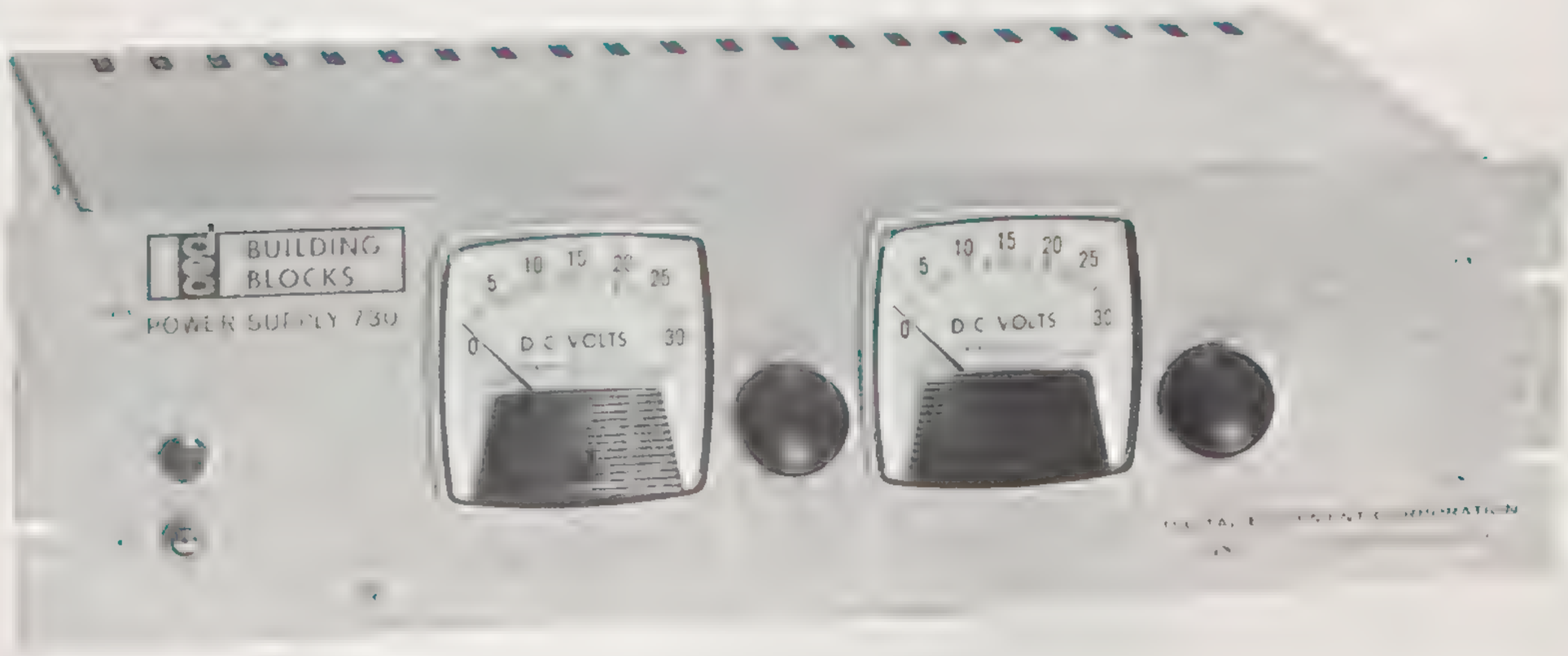
DEPTH: 5¼"

FINISH: Chromicoat

POWER INPUT CONNECTION: Cinch Jones No. 141 terminal strip

POWER OUTPUT CONNECTION: Heyman tab terminals to fit with Amphenol "Faston" Receptacles Series 250, part no. 41774.

730
DUAL VARIABLE POWER SUPPLY



The Dual Variable Power Supply Type 730 is a two-channel, floating output unit for general purpose laboratory use. It is designed to offer the maximum in flexible, maintenance-free operation. Some of its features are: resonant transformers to protect against line variations, variable transformers to give continuous control of output voltage, and silicon rectifiers to insure long life. Placement of meters and all controls on the front panel provides complete ease of operation. Incorporation of two channels in the same package results in a more economical, more compact unit. This is the supply normally used for marginal checking of systems made from DEC Modules.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 0 to ±20 volts DC continuously variable (no load)

OUTPUT CURRENT: 2.5 amperes per channel

LOAD REGULATION: Maximum 3.0 volts drop at 20 volts when load varies from minimum to maximum

LINE REGULATION: 2.0% for input variation from 105 to 125 volts AC

P-P RIPPLE: 1.0 volt at maximum load

LINE FREQUENCY REGULATION: 60 ±0.5 cycles

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 5¼″

CHASSIS WIDTH BEHIND PANEL: 17⅛″

CHASSIS DEPTH BEHIND PANEL: 10¼″

CHASSIS HEIGHT BEHIND PANEL: 5″

FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket

POWER OUTPUT CONNECTION: DC: 10-32 screw terminals. AC: Amphenol 160-4 Socket. A power cable with a two-prong adapter is also furnished.

734
VARIABLE POWER SUPPLY

The Type 734 is a floating power supply that is variable from 0 to 20 volts. It is often used for marginal checking of DEC Systems. A variable transformer gives continuous control of output voltage; a resonant transformer protects against line variations; and silicon rectifiers insure long life. The placement of meter and controls on the front panel facilitates operation. Although designed for mounting on the plenum door of a DEC Computer, this 17 x 8 inch unit may be mounted on a standard 19-inch rack using suitable adapter plates.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGES: 0 to 20 volts DC, continuously variable

MAXIMUM OUTPUT CURRENT: 2.5 amperes

LOAD REGULATION: Maximum 3.0 volts drop at 20 volts when load varies from minimum to maximum

LINE REGULATION: 2% for input variation from 105 to 125 volts AC

P-P RIPPLE: $\leq$ 1.0 volts

LINE FREQUENCY REGULATION: 60 $\pm$0.5 cycles

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16 5/8"

PANEL HEIGHT: 8"

DEPTH: 5 3/8"

FINISH: Chromicoat

POWER INPUT CONNECTIONS: Cinch Jones No. 141 Terminal Strip

POWER OUTPUT CONNECTIONS: Heyman Tab Terminals to fit with Amphenol "Faston" Receptacles Series 250, part no. 41774

743
DUAL POWER SUPPLY

The Type 743 is a dual channel floating (15 volt, 8.5 amperes each) power supply designed to adequately withstand wide line and load variations for general systems use. The package consists of two identical supplies, each one made up of resonant transformer, full wave silicon rectifier and filter capacitor.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 15 volts DC

OUTPUT CURRENT: 1.0 to 8.5 amperes per channel

LINE AND LOAD REGULATION: Output voltage remains between −14.5 to −16 volts when load varies from minimum to maximum and line voltage varies from 105 to 125 volts

P-P RIPPLE: $\leq$ 1.0 volt

LINE FREQUENCY REGULATION: 60 $\pm$0.5 cycles

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″

PANEL HEIGHT: 5¼″

CHASSIS WIDTH BEHIND PANEL: 17⅛″

CHASSIS DEPTH BEHIND PANEL: 10¼″

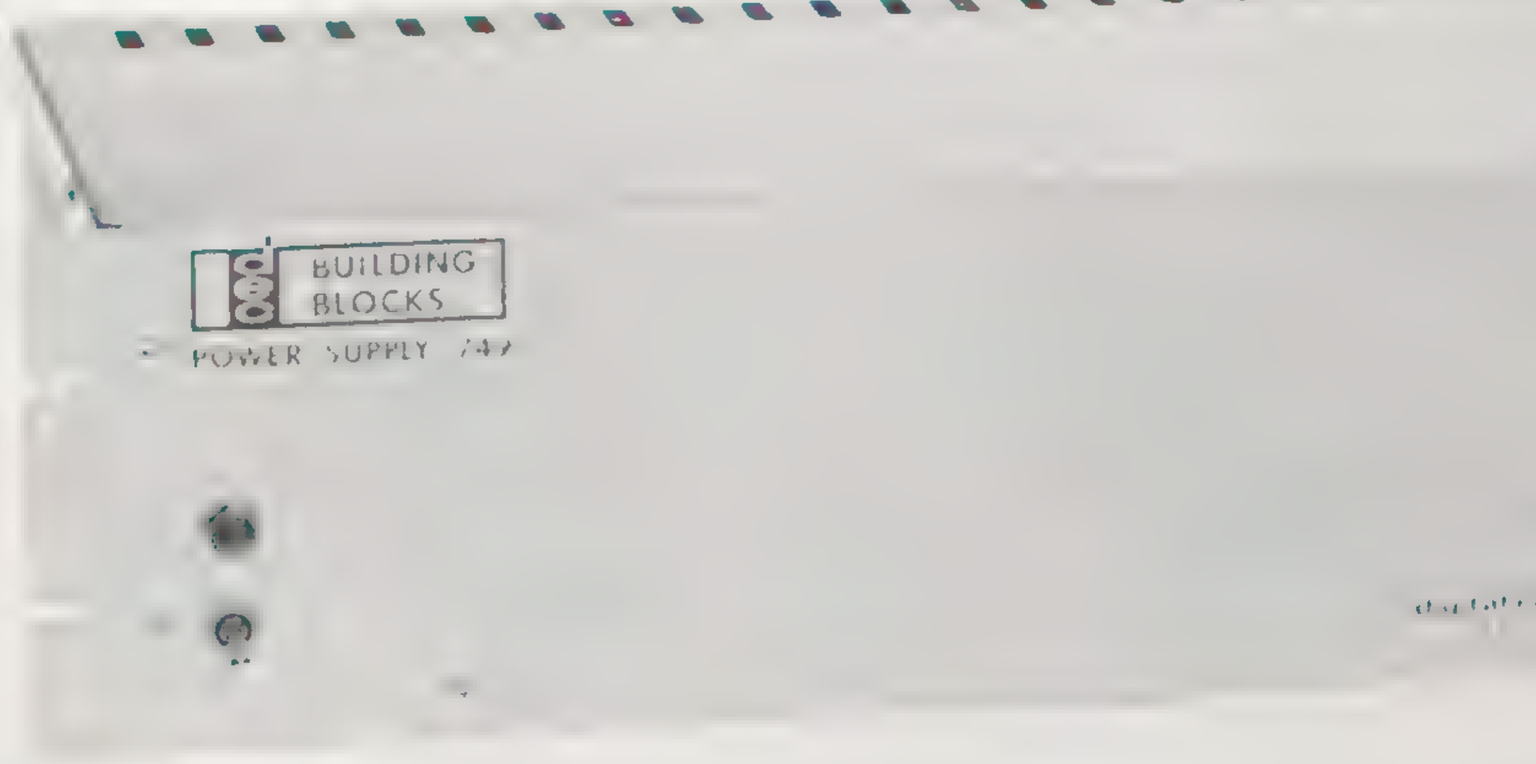
CHASSIS HEIGHT BEHIND PANEL: 5″

FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket

POWER OUTPUT CONNECTION: DC: 10-32 screw terminals. AC: Amphenol 160-4 Socket. A power cable with two-prong adapter is also furnished.

749
POWER SUPPLY



Type 749 is a power supply to be used with DEC Type 51 Negative Current Driver and DEC Type 61 Positive Current Driver. The circuit contains a resonant transformer which minimizes output changes during line and load variations.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 130 volts DC; 150 volts DC; 135 volts DC; 6.3 volts AC, rms.

OUTPUT CURRENT RATING: 130 volts/17-44 ma; 150 volts/14-65 ma; 135 volts/5-300 ma; 6.3 volts AC/6.2 amps.

LINE REGULATION: Approximately 2% on all channels when line changes from 105 to 125 volts AC.

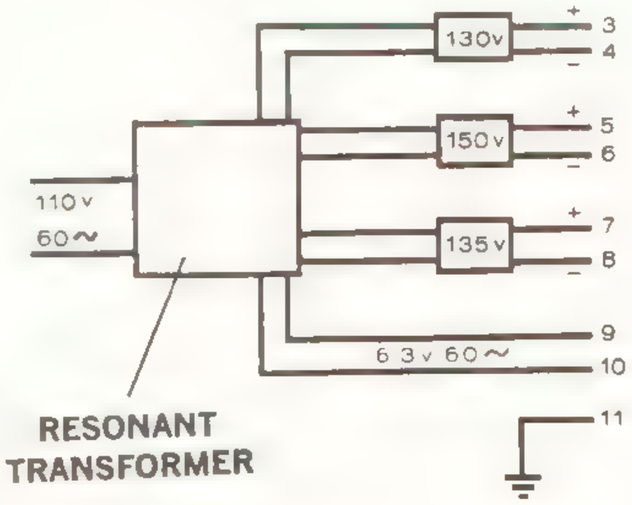
MAXIMUM LOAD REGULATION: 130 volts/3 volts; 150 volts/3 volts; 135 volts/7 volts.

MAXIMUM RIPPLE: 130 volts/0.5 volts p-p; 150 volts/0.9 volts p-p; 135 volts/0.3 volts p-p.

LINE FREQUENCY REGULATION: 60 ±0.5 cycles

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″
PANEL HEIGHT: 5¼″
CHASSIS WIDTH BEHIND PANEL: 17⅛″
CHASSIS DEPTH BEHIND PANEL: 10⅛″
CHASSIS HEIGHT BEHIND PANEL: 5″
FINISH: CHASSIS — Chromicoat; PANEL — Brown "tweed"

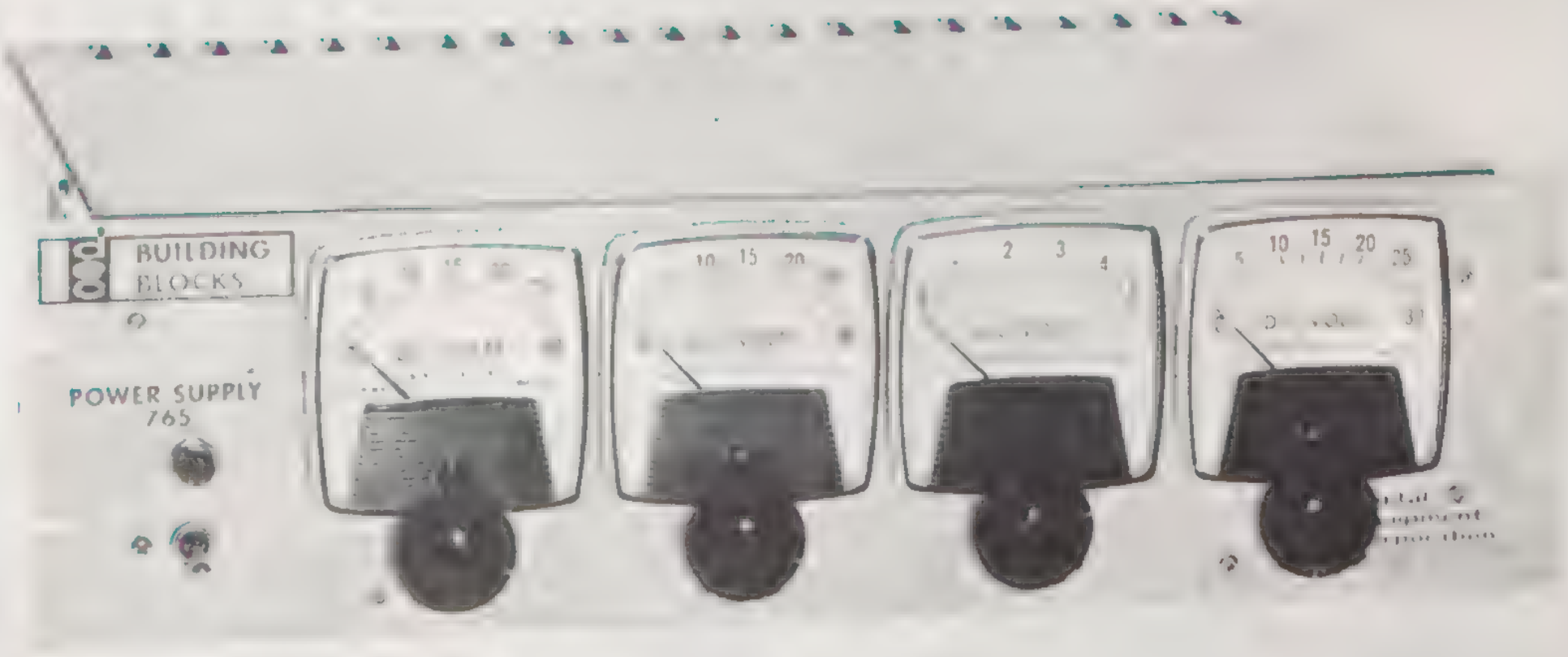


POWER INPUT CONNECTION: Amphenol 160-5 socket
POWER OUTPUT CONNECTION: DC — Cinch Jones S-2410-DB socket. AC — Amphenol 160-4 socket. A power cable with a two-prong adapter is also furnished.

digital

MODULE ACCESSORIES

765
BENCH POWER SUPPLY



The Type 765 is a bench power supply for use in development, testing and marginal checking of DEC Modules. The unit contains four separate variable supplies. A control knob and voltmeter for each channel are on the front panel. The output voltage ranges are:

OUTPUT 1: 0 to +24 volts
OUTPUT 2: 0 to +24 volts
OUTPUT 3: 0 to −4 volts
OUTPUT 4: 0 to −18 volts

Since it is desirable to test modules under adverse conditions, a considerable amount of ripple exists in the Type 765. The Type 765 will drive one module. Connections from the power supply to the module are made with a test power cable, Type 921 for Laboratory Modules or Type 922 for System Modules.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGES: 0 to +24 volts; 0 to +24 volts; 0 to − 4 volts; 0 to −18 volts.

MAXIMUM OUTPUT CURRENT: 24 volts/50 ma; 24 volts/50 ma; −4 volts/100 ma; −18 volts/200 ma.

P-P RIPPLE: 25 volts/500 mv; 25 volts/500 mv; −5 volts/400 mv; −18 volts/800 mv.

OUTPUT IMPEDANCE: Variable with voltage; up to 50 ohms at midscale for 24 volt supplies; −4 volts/4 ohms; −18 volts/7.5 ohms.

LINE VOLTAGE REGULATION: About 20% for line variation of 105 to 125 volts AC

LINE FREQUENCY: 50 to 65 cycles

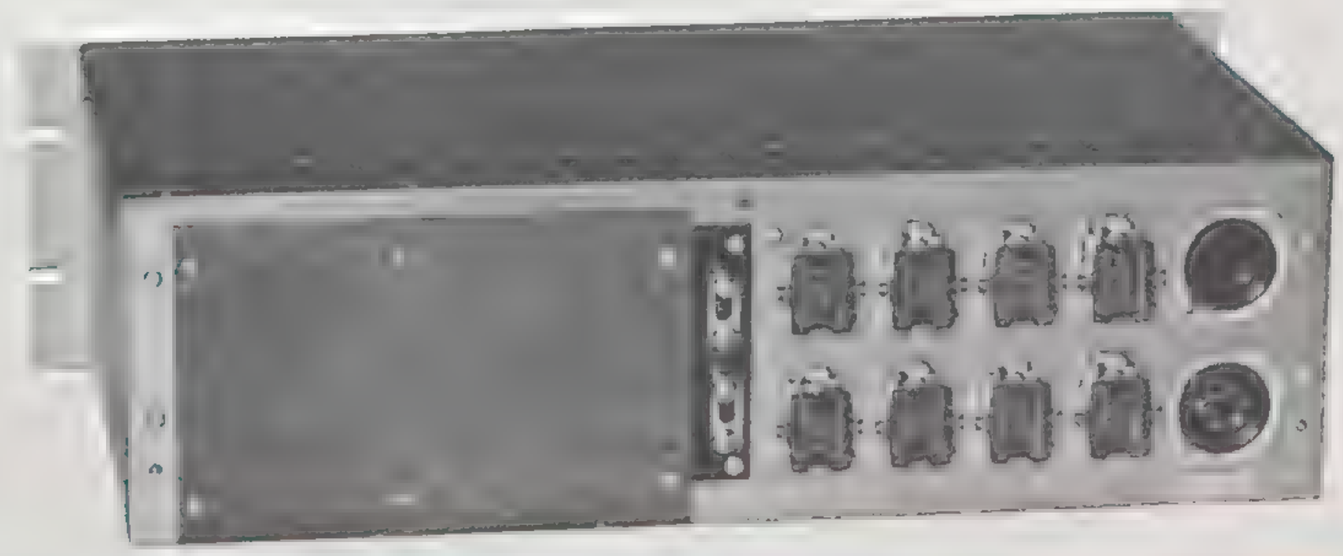
MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″
PANEL HEIGHT: 5¼″

CHASSIS WIDTH BEHIND PANEL: 17⅛"
CHASSIS DEPTH BEHIND PANEL: 10 1/16"
CHASSIS HEIGHT BEHIND PANEL: 5"
FINISH: Chassis — Chromicoat; Panel: Brown "tweed"

POWER INPUT CONNECTION: Amphenol 160-5 socket
POWER OUTPUT CONNECTION: DC: Cinch Jones S-300-FP socket. AC: Amphenol 160-4 socket

769
POWER SUPPLY



The Type 769 is intended for use with DEC Current Drivers Types 52 and 62. The supply can drive up to four Type 52 Negative Current Drivers and four Type 62 Positive Current Drivers. Four output voltages are available. These are: +35 volts, −35 volts, +45 volts, and −45 volts. Figure 1 shows how these voltages are obtained from 35 volt and 10 volt resonant transformer supplies.

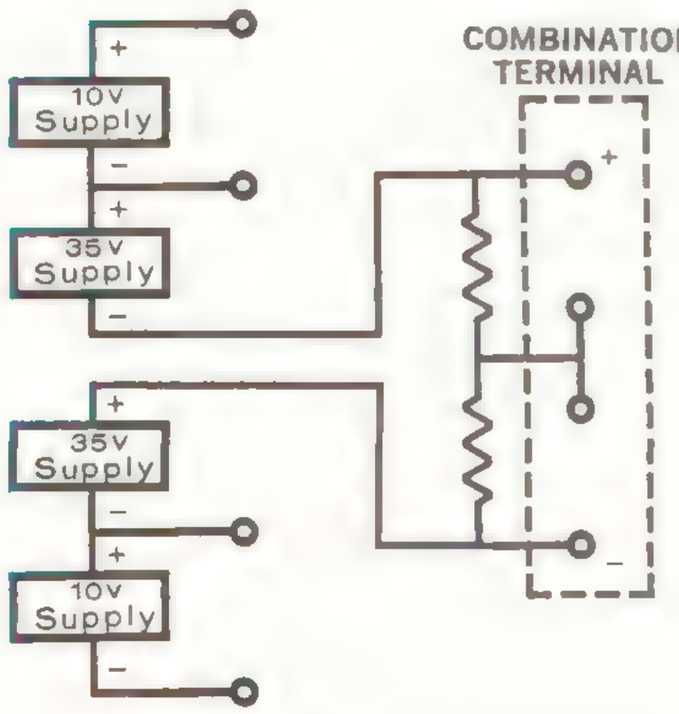


Figure 1

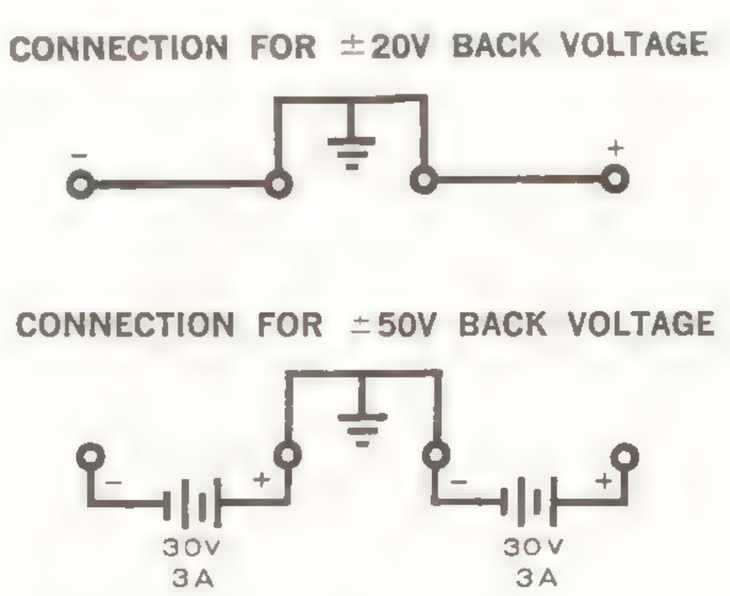


Figure 2

Types 52 and 62 Current Drivers will withstand up to ±20 volts back voltage. By adding additional voltage in series with the power supply output, the back voltage tolerance can be increased to ±50 volts. This connection, shown in Figure 2, requires a +30 volt, 1 amp power supply and a −30 volt, 1 amp supply. Intermediate voltages will give correspondingly less back voltage tolerance. It is not necessary that the positive and negative back voltage tolerances be alike. The supplies only have to handle the average output current of the corresponding current drivers.

A clearly marked combination terminal located on the back of the Type 769 allows for the addition of the extra voltage in order to allow the additional back voltage.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGES: Two 35 volt and two 10 volt supplies connected as shown in Figure 1.

MAXIMUM OUTPUT CURRENT: 4 amperes from each 35 volt supply; 0.35 amperes from each 10 volt supply.

LINE AND LOAD REGULATION: For line voltage variation of 105 to 125 volts and load variations from 0 to maximum, the 35 volt supplies will be between 34 and 40 volts, and the 10 volt supplies will be between 9.5 and 10.6 volts.

P-P RIPPLE: 35 volt/1.5 volts maximum 10 volt/ 0.3 volts maximum.

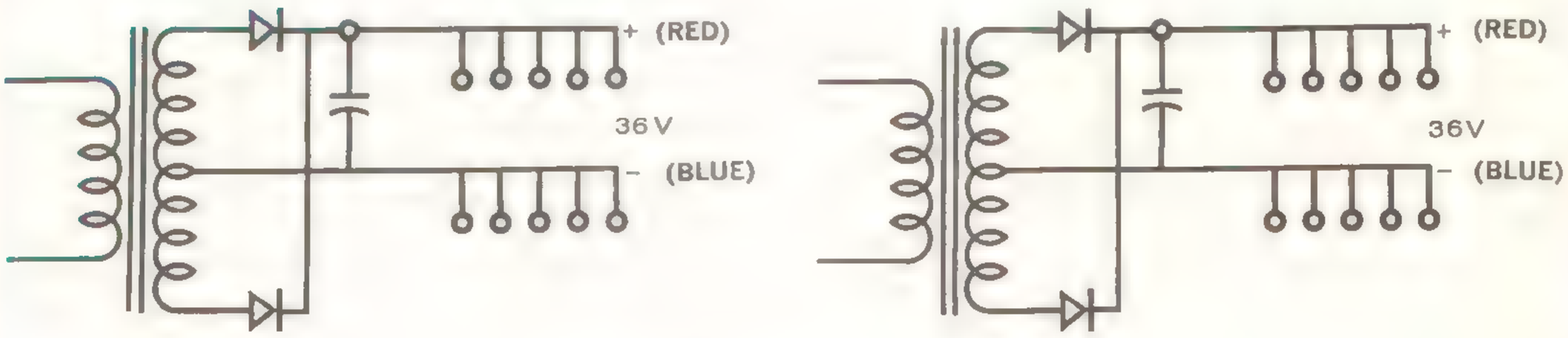
MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19″
PANEL HEIGHT: 5¼″
CHASSIS WIDTH BEHIND PANEL: 17⅛″
CHASSIS DEPTH BEHIND PANEL: 10¾″
CHASSIS HEIGHT BEHIND PANEL: 5″
FINISH: Chassis — Chromicoat; panel — Brown "tweed"
POWER INPUT CONNECTION: Amphenol 160-5 sockets
POWER OUTPUT CONNECTION: DC: 8 Amphenol 26-4401-8P sockets.
AC: Amphenol 160-4 sockets.

772

POWER SUPPLY

The Type 772 is a dual channel floating, 36-volt DC power supply. Each output can supply 1.0 to 5.0 amperes. Each channel contains a resonant transformer, a full wave silicon rectifier, and filter capacitors, resulting in a simple rugged supply able to adequately withstand wide line and load variations for general system use. The unit was designed to be mounted on the plenum door of a DEC Computer Cabinet and may be mounted on standard racks with suitable adapter plates.



DUAL POWER SUPPLY TYPE 772

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGE: 36 volts DC, floating

OUTPUT CURRENT: 1.0 to 5.0 per channel

LINE AND LOAD REGULATION: Output voltage will be between 35 and 39 volts when load varies from minimum to maximum and line voltage varies from 105 to 125 volts AC

RIPPLE: $\leq$2 volts

LINE FREQUENCY REGULATION: 60 cycles $\pm$0.5

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16 5/8"

PANEL HEIGHT 8"

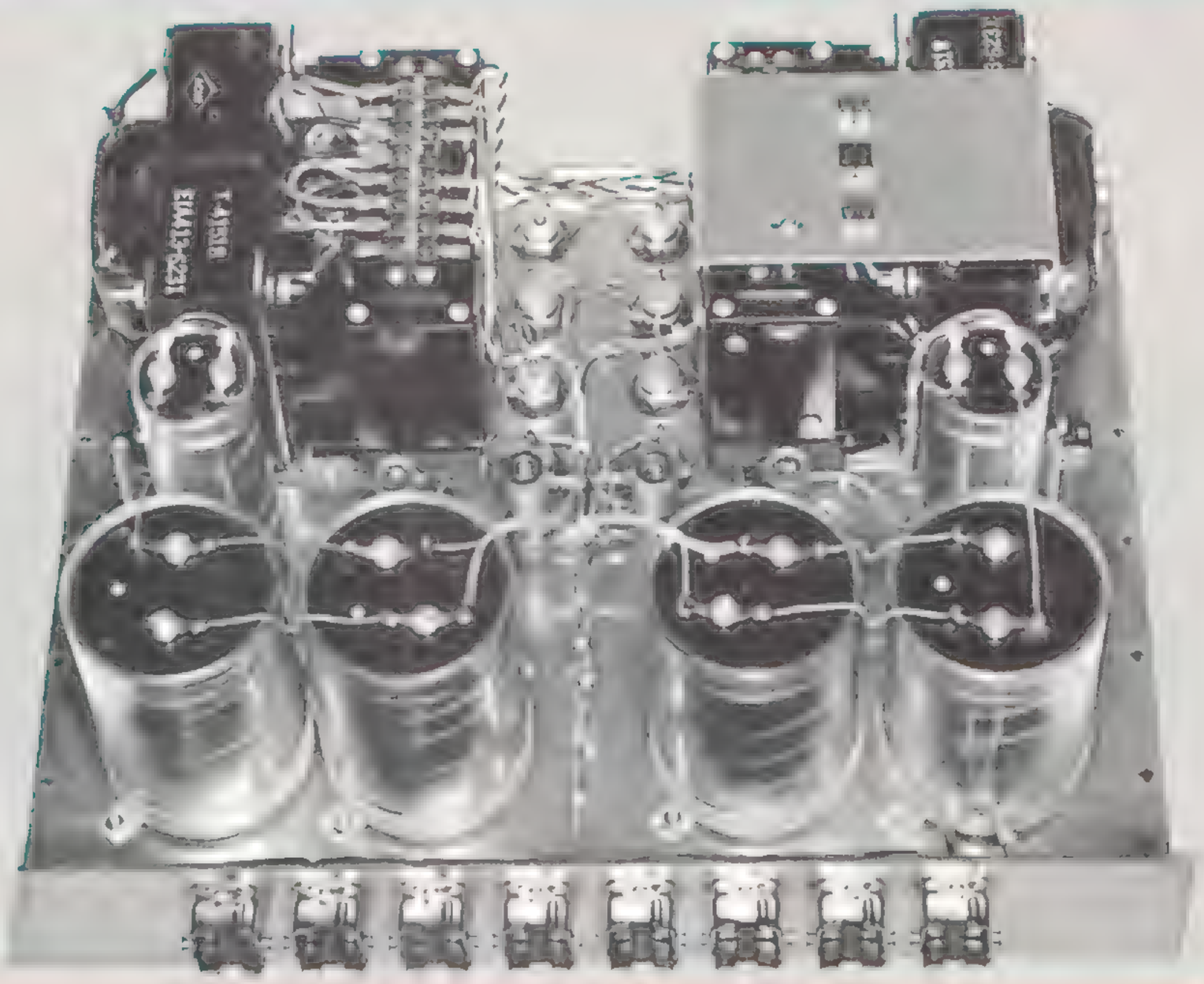
DEPTH BEHIND PANEL: 5"

FINISH: Chromicoat

POWER INPUT CONNECTION: Cinch Jones No. 141 terminal strip

POWER OUTPUT CONNECTION: Heyman Tab terminals to fit with Amphenol "Faston" Receptacles Series 250, part No. 41774.

776
POWER SUPPLY



The Type 776 is intended for use with DEC Current Drivers Types 52 and 62. The supply can drive up to four Type 52 Negative Current Drivers and four Type 62 Positive Current Drivers. Four output voltages are available. These are: +35 volts, −35 volts, +45 volts, and −45 volts. Figure 1 shows how these voltages are obtained from 35 volt and 10 volt resonant transformer supplies.

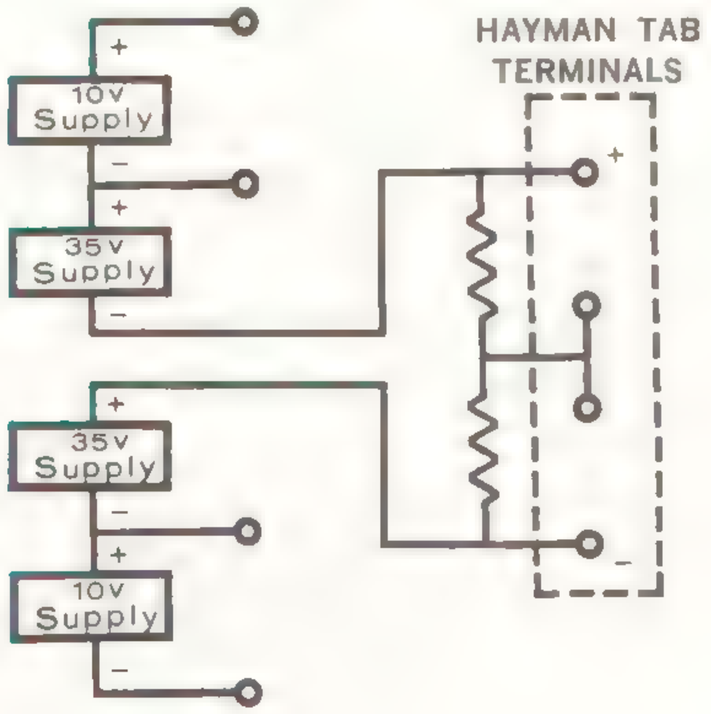


Figure 1

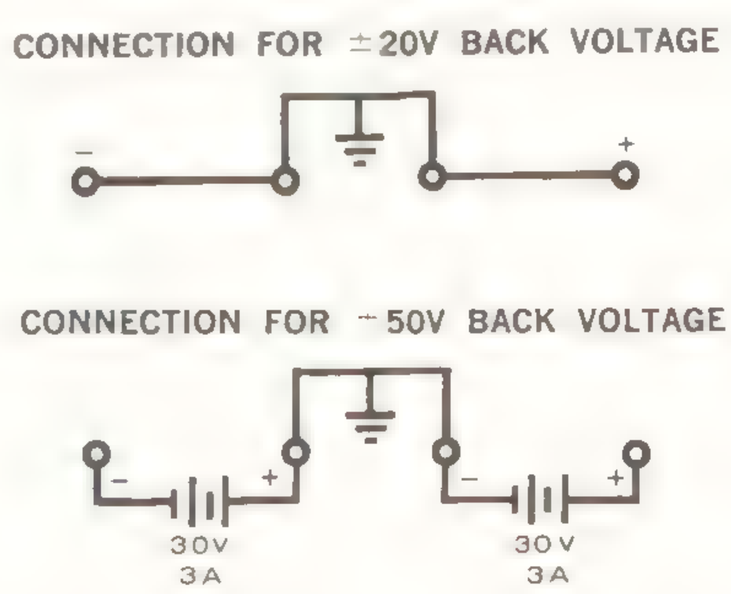


Figure 2

Types 52 and 62 Current Drivers will withstand up to ±20 volts back voltage. By adding additional voltage in series with the power supply output, the back voltage tolerance can be increased to ±50 volts. This connection, shown in Figure 2, requires a +30 volt, 1 amp power supply and a −30 volt, 1 amp supply. Intermediate voltages will give correspondingly less back voltage tolerance. It is not necessary that the positive and negative back voltage tolerances be alike. The supplies only have to handle the average output current of the corresponding current drivers.

ELECTRICAL CHARACTERISTICS

OUTPUT VOLTAGES: Two 35 volt and two 10 volt supplies connected as shown in Figure 1.

MAXIMUM OUTPUT CURRENT: 4 amperes from each 35 volt supply; 0.35 amperes from each 10 volt supply

LINE AND LOAD REGULATION: For line voltage variation of 105 to 125 volts and load variations from 0 to maximum, the 35 volt supplies will be between 34 and 40 volts, and the 10 volt supplies will be between 9.5 and 10.6 volts.

P-P RIPPLE: 35 volt/1.5 volts maximum 10 volt/0.3 volts maximum

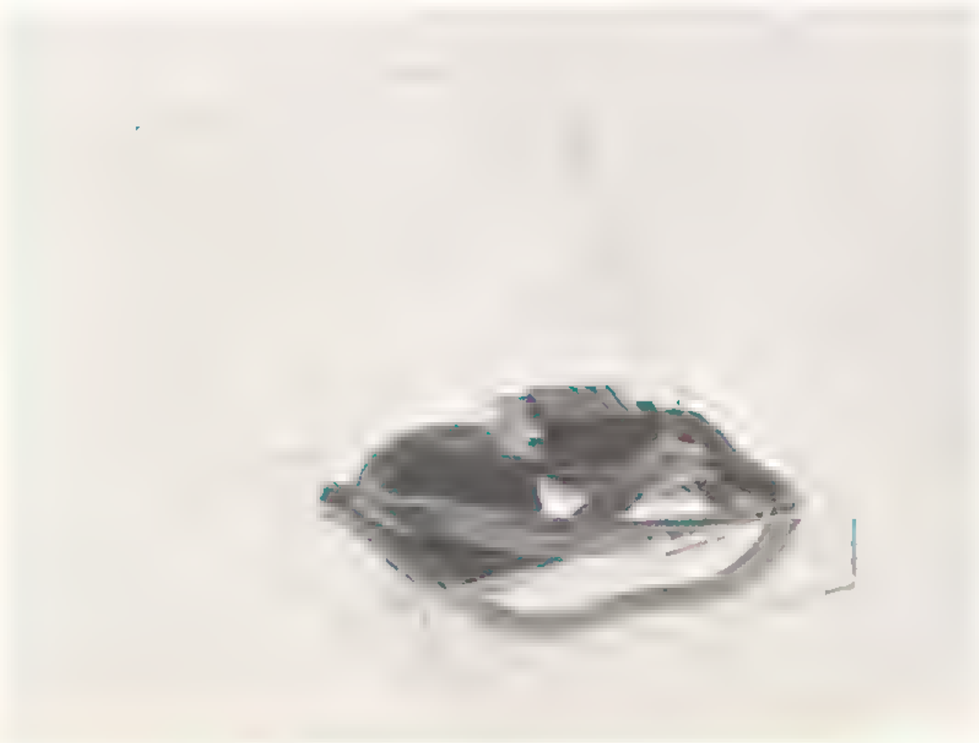
MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝"
PANEL HEIGHT: 14"
DEPTH: 5"
FINISH: Chromicoat
POWER INPUT CONNECTION: Cinch Jones no. 141 Terminal Strip
POWER OUTPUT CONNECTION: DC: 8 Amphenol 26-4401-8P sockets.

901-750-911-921

MOUNTING PANEL AND ACCESSORIES

The Type 901 Mounting Panel accepts up to nine DEC 500 kilocycles, 5 megacycles or 10 megacycle Digital Laboratory Modules. The required power connections to each module are completed automatically when the module is plugged into the banana-jack lugs located at the rear of the mounting panel. The panel requires 5¼ inches of vertical space in a standard 19-inch rack and may be connected to a DEC Type 722 Power Supply using a DEC Type 750 Power Supply Connector Cable.



POWER CABLE TYPE 750

The Type 750 is a 2½ foot power cable equipped with Jones plugs on both ends for connecting the Mounting Panel Type 901 to the DEC Power Supply 722.

PATCHCORDS TYPE 911

DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 inches (brown), 4 inches (red), 8 inches (orange), 16 inches (yellow), 32 inches (green), and 64 inches (blue). These easy-to-use patchcords may be stacked to permit multiple connections at any circuit point on the graphic front panels of the DEC line of Digital Laboratory Modules. The cords are supplied in snap-lid plastic boxes for handy storage.

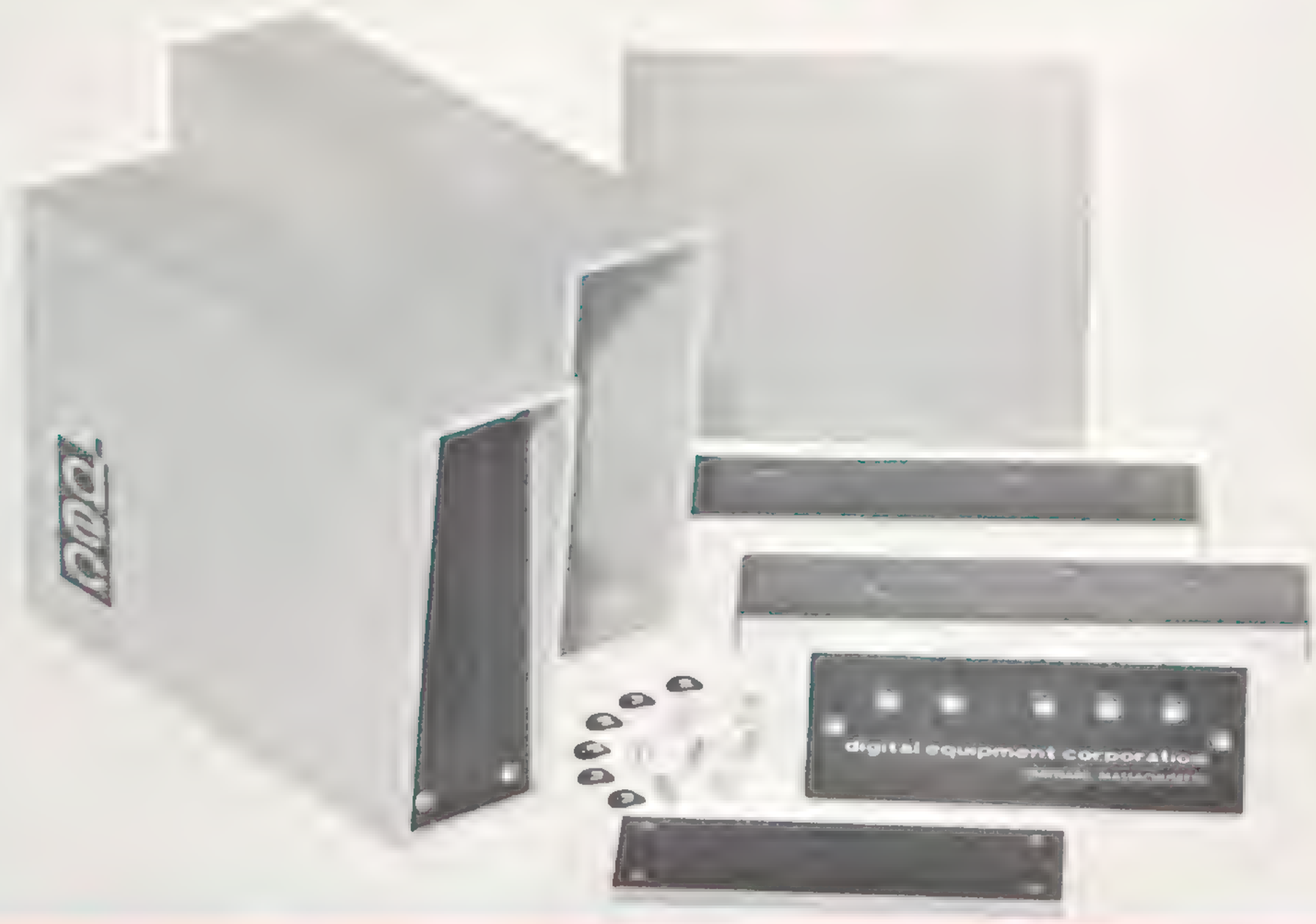
LABORATORY MODULE TEST POWER CABLE TYPE 921

The Test Power Cable connects a single laboratory module to a Type 722 Power Supply (or similar type). It allows the module to operate with aluminum housing removed for test purposes.

digital

MODULE ACCESSORIES

950-951
BLANK
LABORATORY MODULES



Blank Laboratory Modules are available for mounting special circuits.

The Type 950 is an assembled Laboratory Module. The circuit board is not copper clad, and both the circuit board and the front panel are blank.

The Type 951 is an unassembled Laboratory Module. The circuit board is copper clad to permit the user to print his own special circuit. All necessary parts are provided, including a protective aluminum case, blank circuit board, blank front panel, back panel with power connections, set of brackets, and the required nuts and bolts.

digital

MODULE ACCESSORIES

1901-1903-1904-1905 MOUNTING PANELS

DEC Mounting Panels, Types 1901, 1903, 1904, and 1905 provide economical flexibility for DEC 500 kilocycle, 5 megacycle and 10 megacycle System Modules. The panels are rack mounting and are finished in brown "tweed"

Power wiring is factory-installed and coded connectors assure that power voltages will never appear at the wrong module input terminals. Logical wiring is solder-connected to the mounting chassis, thus allowing the modules to be removed for other applications, or for testing purposes, without disrupting the logic. The functions of the various lettered connecting points can be readily determined from the logical diagrams of the DEC System Modules.

Panels utilize 22-pin Amphenol Type 143-022-04 pin connectors and require only 5¼ inches of vertical space. Chassis depth is 7⅞ inches. The table of mechanical characteristics describes the individual panel lengths and the number of units each panel can accommodate.

Table of Mechanical Characteristics

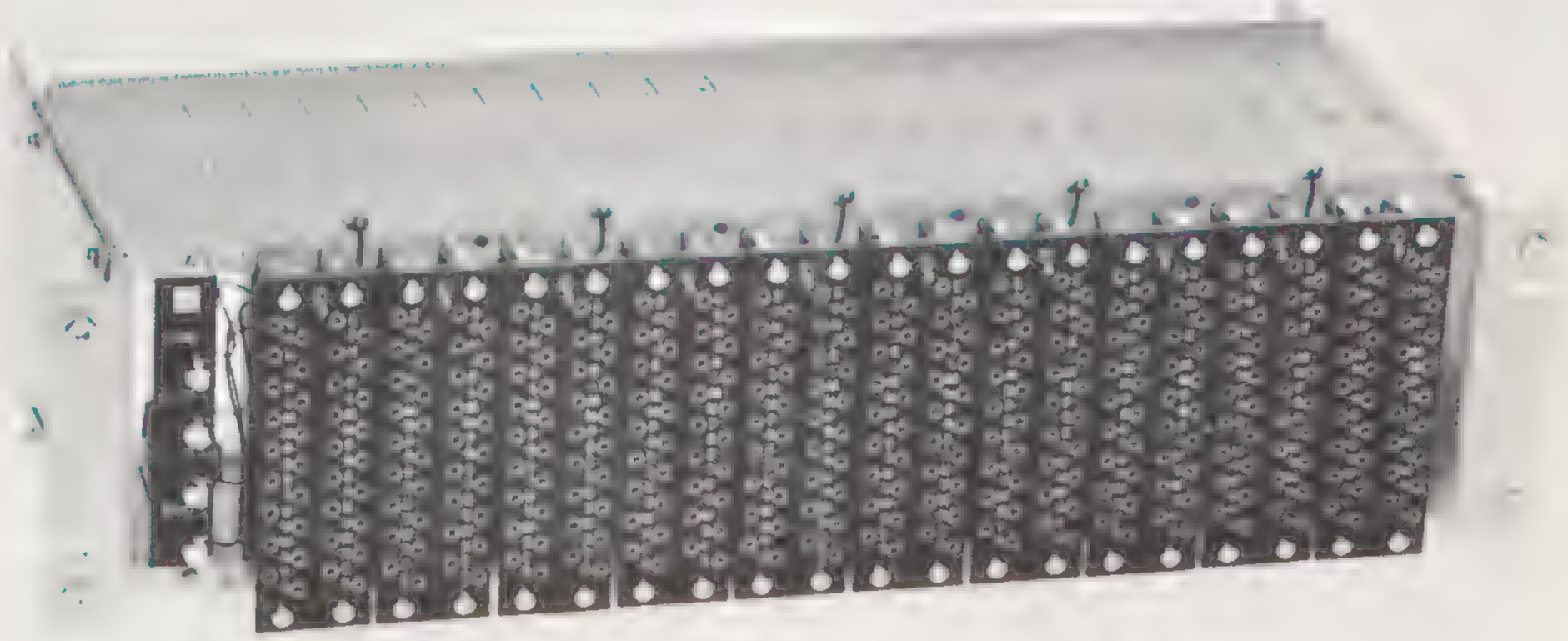
TYPE NUMBER	MODULES HOUSED	PANEL LENGTH	CHASSIS LENGTH
1901	25	19″	17 5/16″
1903	20	19″	17 5/16″
1904	43	30″	28″
1905	33	24″	21 7/8″

digital

MODULE ACCESSORIES

1906-911

PATCHCORD MOUNTING PANEL



DEC Type 1906 Mounting Panel now provides patchboard flexibility for up to 20 DEC System Modules, widely used as plug-in units for permanent systems. This new patchcord mounting panel brings many of the advantages of DEC Digital Laboratory Modules to the system units. The panel permits 1000 and 4000 Series System Modules to serve either as a permanent or as an experimental logic package, thus providing additional economy. This should not be used with 6000 Series Modules.

The panel uses 5¼ inches of vertical space in a standard 19-inch relay rack. The chassis is furnished in brown "tweed". The patchboard is "chocolate brown".

The terminals (E through Z) of each module connector are attached to 18 corresponding banana-jack sockets on the front of the mounting panel, making possible speedy interconnection with stacking banana-jack patchcord. The functions of the various lettered sockets can be readily determined from the logical diagrams of the respective System Modules, enabling the engineer to make a rapid circuit "set up" that is easily modified.

A further advantage of the Type 1906 Mounting Panel is that System Modules can be unplugged for another application without disconnecting the logic on the patchboard.

911 PATCHCORDS

DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 inches (brown), 4 inches (red), 8 inches (orange), 16 inches (yellow), 32 inches (green), and 64 inches (blue). These easy-to-use patchcords may be stacked to permit multiple connections at any terminal point. The cords are supplied in snap-lid plastic boxes for handy storage.

digital

MODULE ACCESSORIES

1907-1925-1926

COVER PLATE AND

BLANK PANELS

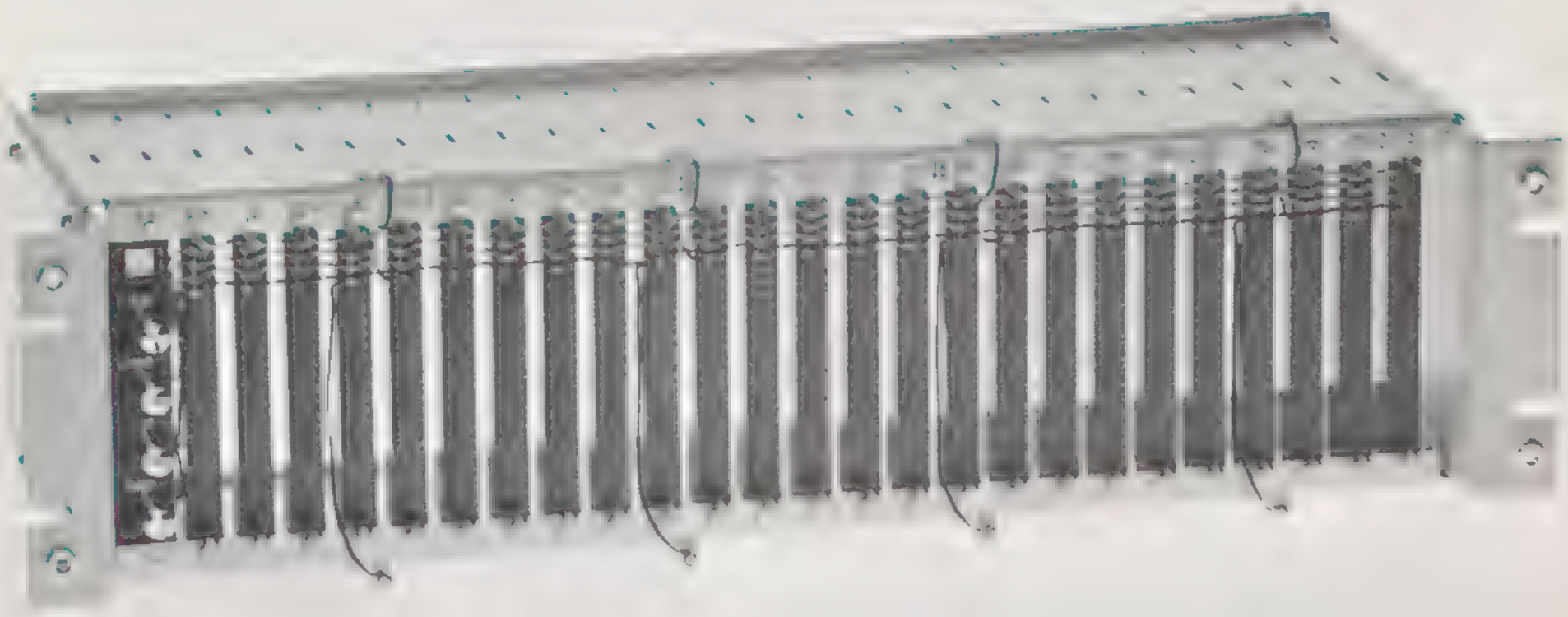
The Mounting Panel Cover Type 1907 is designed to cover the power and logic wiring for the Type 1901 and 1903 Mounting Panels. The cover is fastened to the mounting panels with captive screws that fit tapped holes provided for the purpose in the mounting panels. The cover is shaped to fit over the wiring terminals and is finished in brown "tweed". Dimensions are 5¼ inches by 19 inches.

Blank panels designed to fit 19-inch racks are available for mounting indicator lights and control switches. Panels are finished in brown "tweed" and are available in 3½ inch (Type 1925) or 5¼ inch (Type 1926) heights.

digital

MODULE ACCESSORIES

1909-1910-1915-912
1961-1962-1963
TAPER-PIN PATCHCORD
MOUNTING PANELS

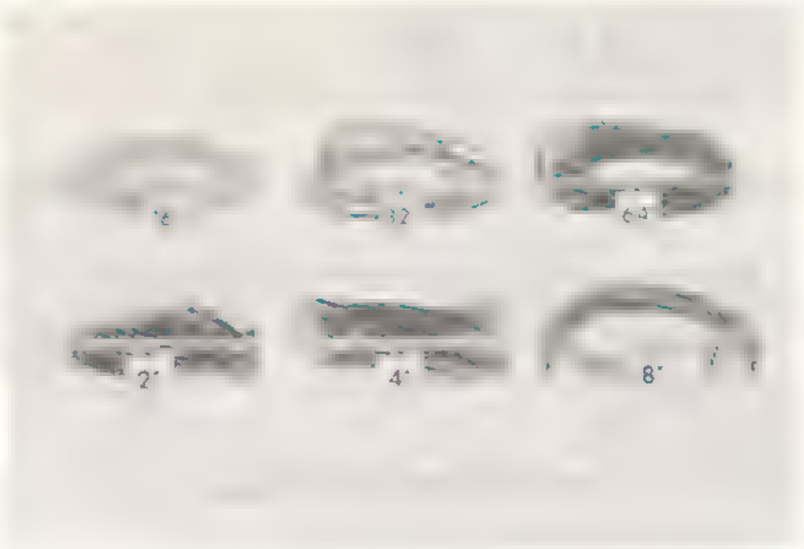


The DEC Types 1909, 1910 and 1915 Taper-Pin Patchcord Mounting Panels provide economical flexibility for DEC 500 kilocycle, 5 megacycle and 10 megacycle System Modules. These panels permit the use of patchcords of the low-cost taper-pin type. The panels serve to combine the complete flexibility of DEC Digital Laboratory Modules with the wide selection of compact DEC System Modules. The space-saving logic units can thus be made to serve dual functions as experimental packages, which can be easily connected or changed without soldering or as permanent logic circuits. Since the patchcords are not plugged into the units themselves, the modules can be removed for other applications or for testing purposes without disrupting the patchcord logic.

The panels utilize 22-pin connectors, Amphenol Type 143-827-1002, and require only 5¼ inches of vertical space in standard 19 or 24-inch relay racks. The Type 1910 accommodates 20 System Modules in a 19-inch panel. Up to 25 System Modules can be inserted in the 19-inch Type 1909 Mounting Panel. Type 1915 can accommodate up to 33 System Modules and measures 24 inches in length. Each connecting point has two pin sockets for easy in-out connections. The functions of the various lettered connecting points can be readily determined from the logical diagrams of the DEC line of 500 kilocycle, 5 megacycle and 10 megacycle System Modules.

912 PATCHCORDS

Taper-pin patchcords can be inserted or removed from the mounting panels with needle-nosed pliers or with special inserter and puller tools available as optional accessories. Type 912 Patchcords featuring gold-plated taper pins, are available in color-coded standard lengths of 2, 4, 8, 16, 32, and 64 inches. All cords are shipped in handy polystyrene window-type, snap-lid boxes. Gold plated taper-pins are Amp "53" series part number 41649 (strip form) or 41666 (loose piece).



1961-1962-1963 TAPER PIN TOOLS

Taper pin inserter and extractor tools are available for easy handling of the taper pin connections. A crimper tool is also available for attaching taper pins to special wires.

The spring loaded taper pin inserter tool, Type 1962, permits taper pins to be easily seated in their mating receptacles. The tool is designed to permit dexterity in confined areas. The spring mechanism in the tool assures that the proper amount of force will be exerted for placing the pin firmly in the receptacle. In addition, the inserter tool will firmly support both the pin and wire during the entire operation. This tool may also be purchased from AMP Inc. as AMP Model Number 380306-3.

The Type 1963 Taper Pin Extractor Tool allows the pins to be removed easily from the mating connectors. The two-prong fork may be hooked over the metal portion of the pin so that the connector is removed without strain on the wire. The AMP Model Number is 380305-1.

A hand crimper tool, Type 1961, may be used to crimp taper pins. Use of this tool assures a good electrical connection. The AMP Model Number is 47042.

digital

MODULE ACCESSORIES

1913
MOUNTING PANEL

Type 1913 is a 19-inch mounting panel designed to accommodate a maximum of six current drivers (Types 52 and 62), or four current drivers and one current/voltage calibrator Types 71 and 72.

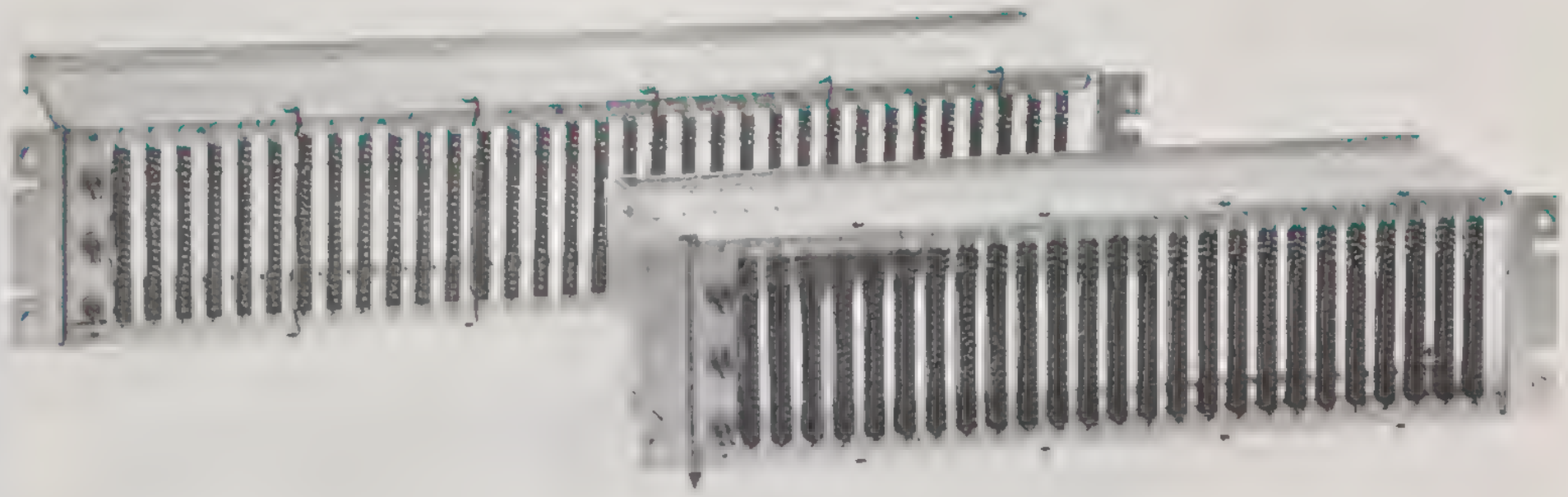
MECHANICAL CHARACTERISTICS

PANEL HEIGHT: 10½"
CHASSIS DEPTH: 7"
FINISH: SIDE PANELS — Brown "Tweed"
UPPER AND LOWER PANELS — Chromicoat

digital

MODULE ACCESSORIES

1914-1916-1917
MOUNTING PANELS



The Types 1914, 1916 and 1917 Mounting Panels are designed for use with the DEC System Modules. Logical wiring is solder-connected to the mounting panel. Marginal check switches are provided at the power input terminals. Mounting panel finish is chromicoat.

These mounting panels are similar to the Type 1901 and 1905. The Type 1914 is designed for mounting in standard 19-inch racks and will accommodate up to twenty-five system modules. The Type 1917 mounts in a standard 24-inch rack and accommodates up to thirty-three modules. The Type 1916 is a 17-inch rack mounting panel designed to fit on the plenum doors of DEC computer cabinets. It will accommodate up to twenty-two modules.

MECHANICAL CHARACTERISTICS

TYPE NUMBER	MODULES HOUSED	PANEL LENGTH	CHASSIS LENGTH
1914	25	19″	17 5/16″
1916	22	17″	14 13/16″
1917	33	24″	21 7/8″

digital

MODULE ACCESSORIES

1918-1923 MOUNTING PANELS

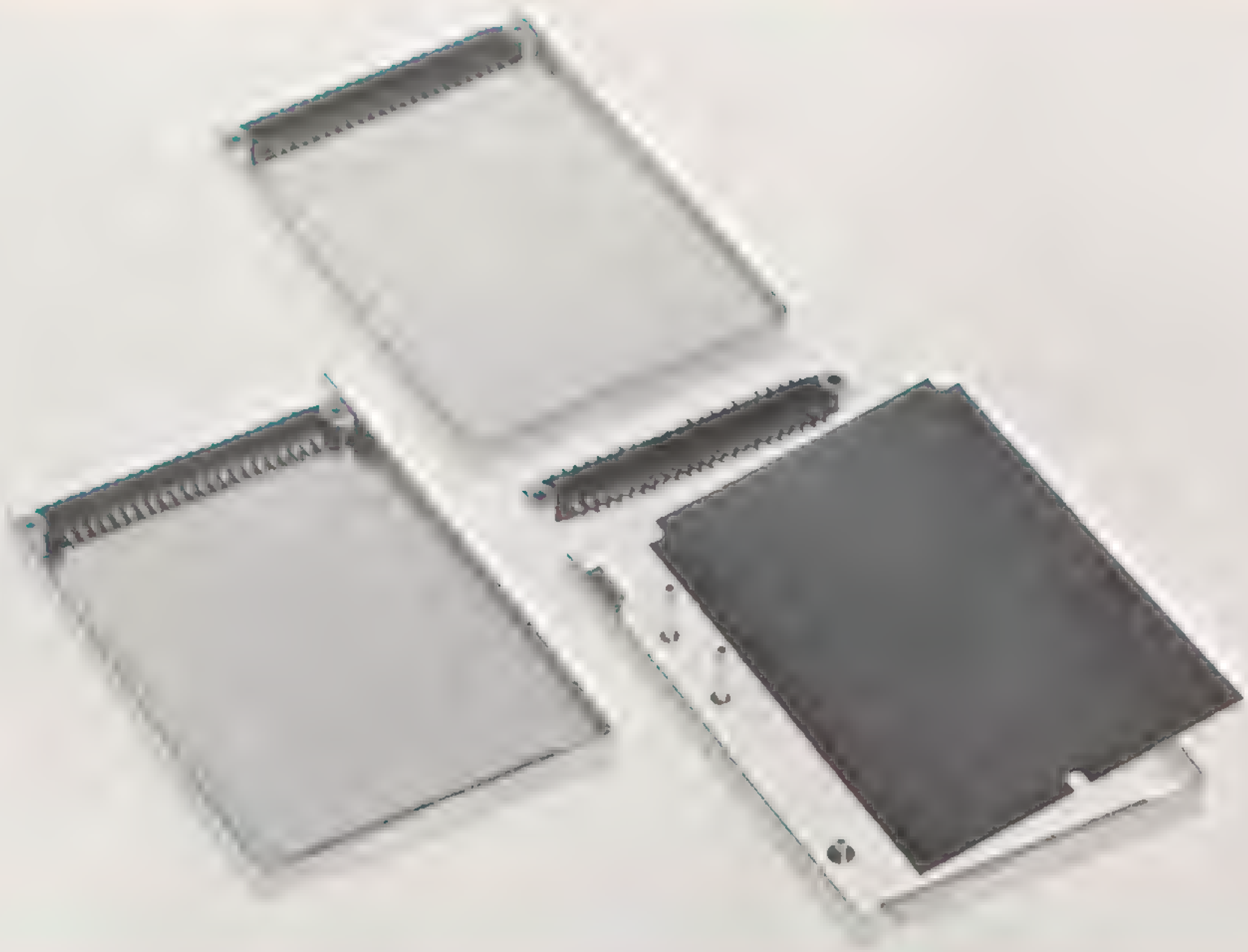
The Types 1918 and 1923 Mounting Panels are designed for use with DEC System Modules. These panels are similar to the Types 1901 and 1903 except that the logical connections are made with wire wrap terminals. The panels are finished in brown "tweed" and are suitable for mounting in standard 19-inch racks.

The Type 1918 will accommodate up to 25 modules and the Type 1923 will accommodate up to twenty modules. The four power input terminals, +10 volts (A), +10 volts(B), −15 volts and ground are brought out to a terminal strip for connection to the power supplies with spade lugs.

For both the mounting panels, the overall paneled length is 19 inches; the chassis length is 17 5/16 inches; and the height is 5¼ inches.

digital MODULE ACCESSORIES

1950-1951-1955
BLANK SYSTEM MODULES



Blank System Modules are available for mounting special circuits. All necessary hardware is provided, including the circuit board, standard 22-pin Amphenol plug part #133-022-21 protective aluminum frame, and a set of eyelets. Board space available for circuit lay out is 4 inches by 5 inches.

The Type 1950 is an assembled System Module. The circuit board is not copper clad.

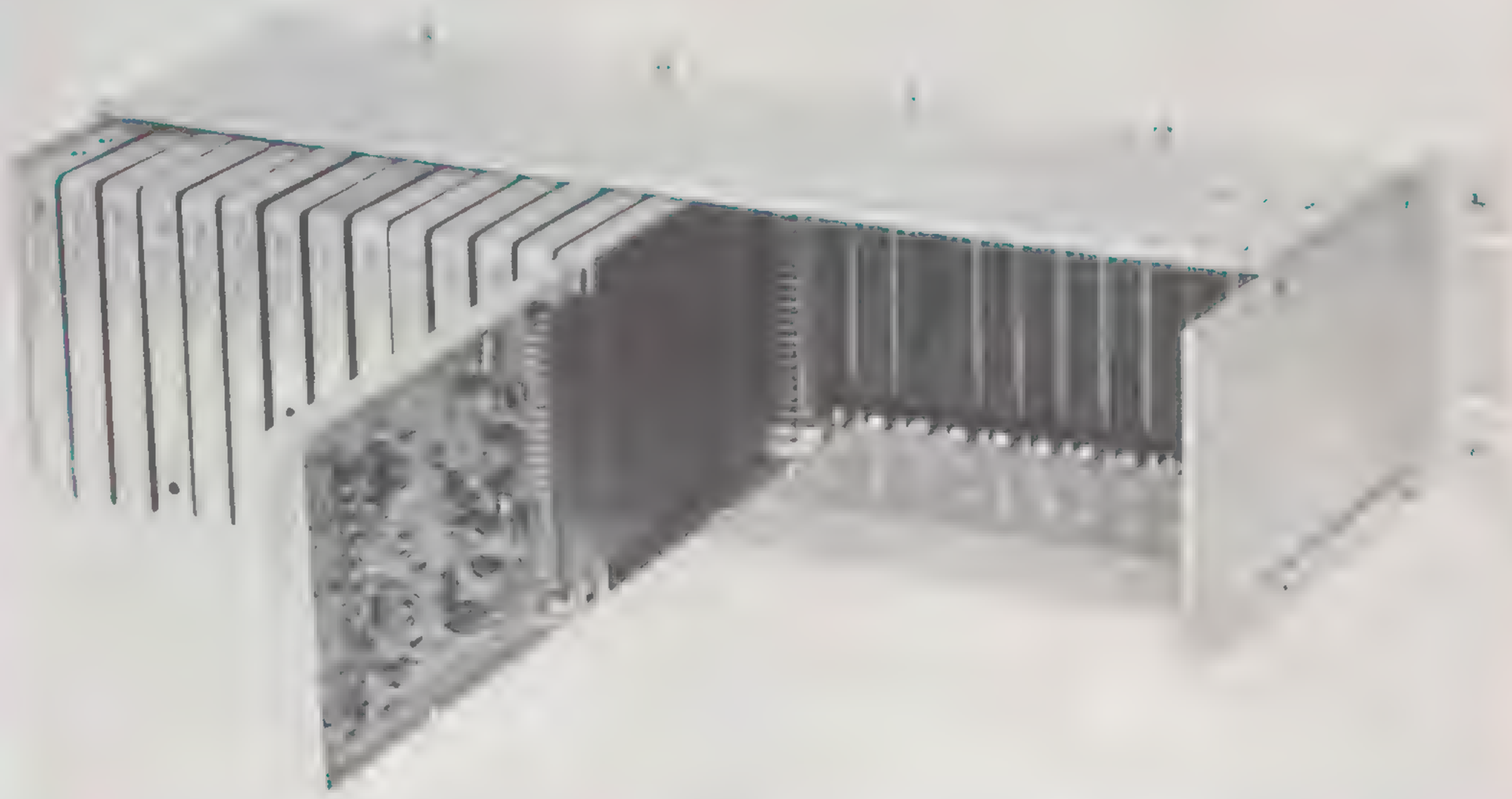
The Type 1951 is an unassembled System Module. The circuit board is copper clad to permit the user to print his own special circuit.

The Type 1955 is an assembled System Module. The circuit board is a pre-punched vector board. Leads may be inserted directly on the board or vector type T28 miniature terminals may be used.

digital

MODULE ACCESSORIES

1954-1960-922
ACCESSORIES



1954 SYSTEM MODULE EXTENDER

The Type 1954 System Module Extender allows access to the module circuitry without breaking connections between the unit and the mounting panel wiring. The module extender is particularly useful with the digital-to-analog converters and other modules which contain potentiometers to be adjusted.

1960 SYSTEM MODULE PULLER

The Type 1960 System Module Puller may be used to remove System Modules from the mounting panels. The modules may also be removed by hand, if desired.

922 TEST POWER CABLE

A Tvpe 922 Test Power Cable permits testing and maintenance of individual System Modules. Power is brought into the module through a cable with a Cinch Jones male plug which connects to the Type 722 or the Type 765 Power Supplies. Logical connections are brought out to eyelets for use with the Type 911 stacking banana-jack patchcords.

OTHER DIGITAL PRODUCTS

In addition to the Laboratory and System Modules described on the preceding pages, Digital designs and manufactures modules for instruction in logic techniques, special systems and general purpose digital computers.

TRAINING MODULES

A number of 3000 Series Laboratory Modules are available with MIL symbology on the graphic front panels in place of the standard DEC symbology. Units in this line are the Type 3102 Inverter, Type 3112 OR-NOR, Type 3114 AND-NAND, Type 3203 Flip-Flop, and Type 3302 Delay.

CLASSROOM MODULES

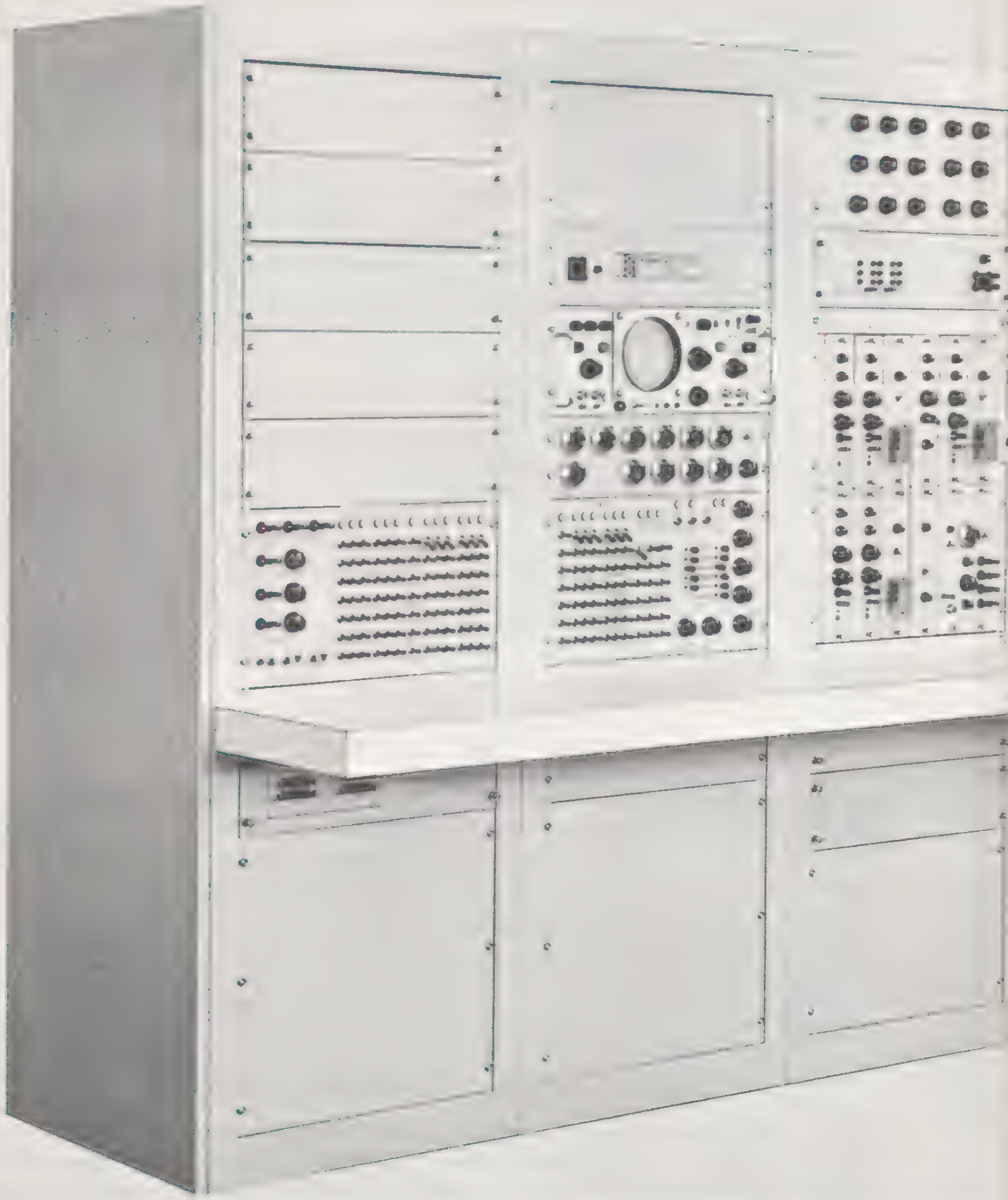
To facilitate classroom instruction, a basic selection of 500 kilocycle Laboratory Modules is produced with front panels which accommodate graphic symbology four times the normal size. Both MIL symbology and DEC symbology units are available. The overall dimensions of these units are 4⅞ by 12 by 1½ inches. Up to 10 units may be inserted in the special wall-type mounting panel Type 901C. Included in the 3000C Series are the Types 3101C and 3102C Inverters, Type 3110C NOR, Type 3112C OR-NOR, Type 3114C AND-NAND, Types 3201C and 3203C Flip-Flops, Types 3301C and 3302C Delays, Type 3401C Clock, Type 3410C Pulse Generator, and Type 3602C Pulse Amplifier

SPECIAL DIGITAL SYSTEMS

Digital's Special Systems Division builds a variety of digital systems from high reliability System Modules and DEC High Current Pulse Equipment. The Digital Automatic Memory Testers, Memory Exercisers, Memory Core Testers, and Buffer Systems shown on the following pages have achieved widespread acceptance as standard test equipment in the memory industry. The systems within each series are similar in basic design and have only minor modifications to meet individual customer requirements. Numerous other special systems, however, are designed and built to specification.

PROGRAMMED DATA PROCESSORS

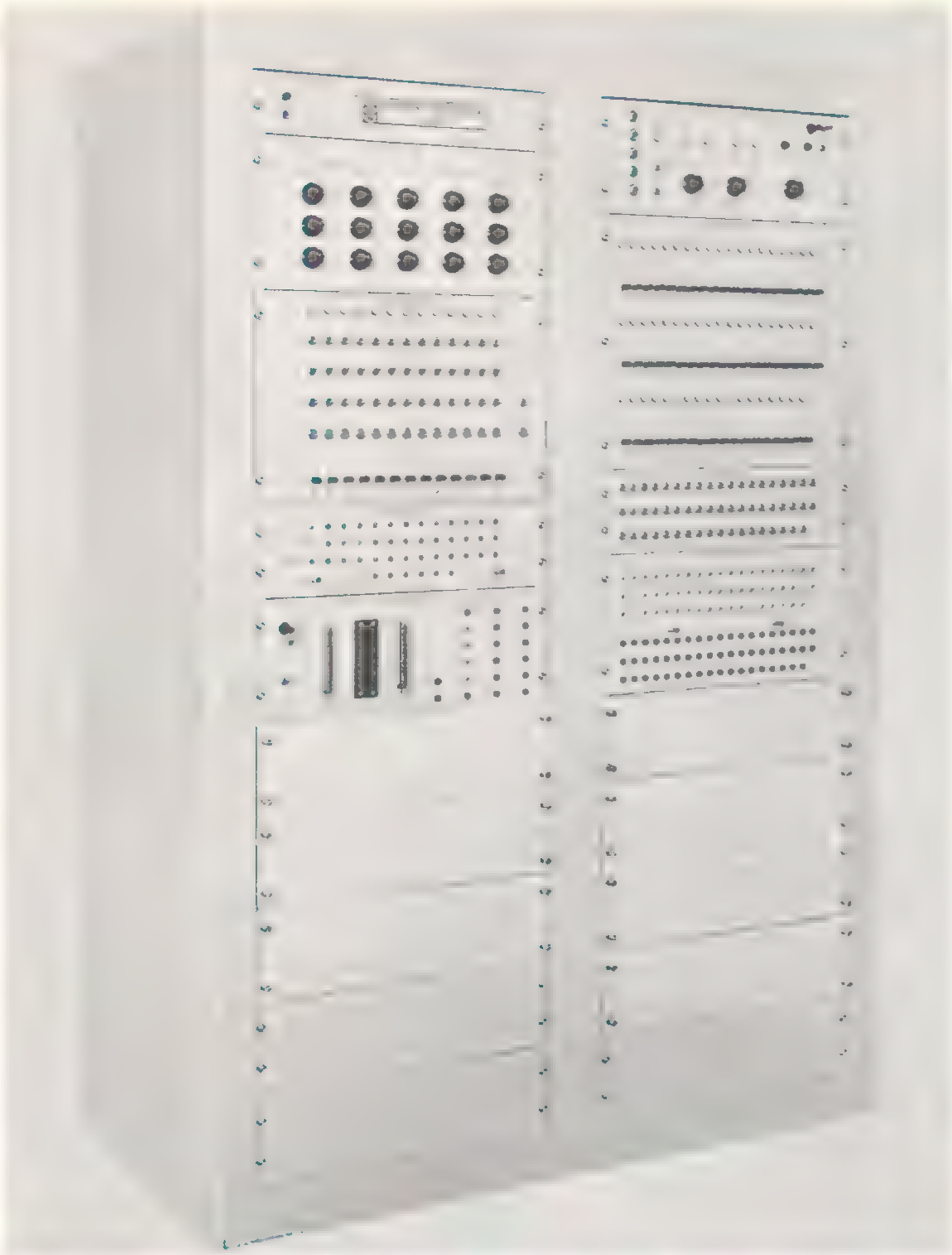
Digital's Computer Division produces solid state, general purpose digital computers with a computation rate of 100,000 additions per second (including two calls on memory), exceptionally flexible input-output capability, and such important programming features as multiple-step indirect addressing. The speed, versatility and programming power of the PDP-1 has made it a popular choice among scientific and research organizations.



1500 SERIES MEMORY TESTERS

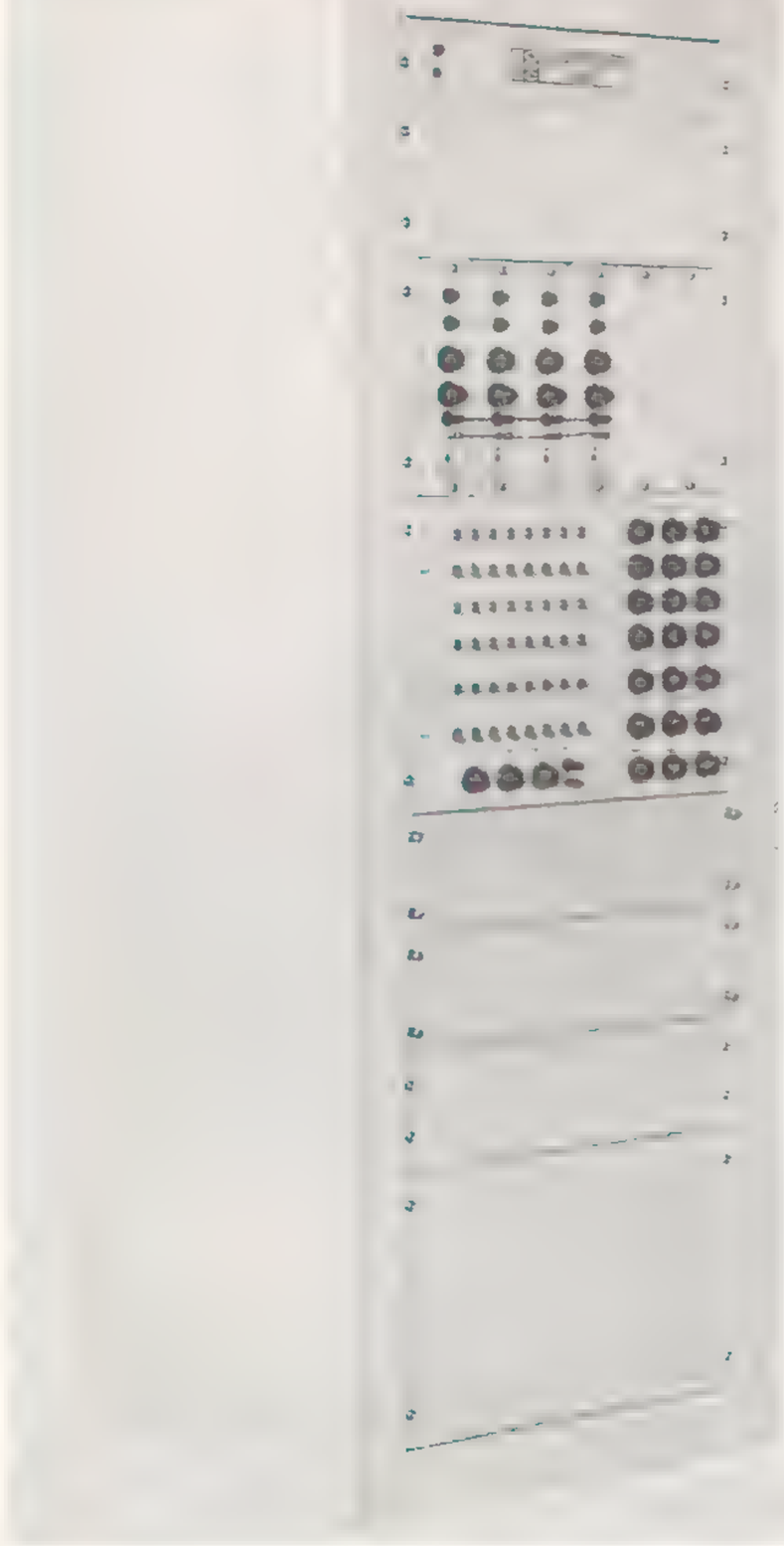
Digital 1500 Series Automatic Test Systems provide complete facilities for the rapid testing of coincident current and word address memory planes and stacks under simulated operational conditions using electronic switching techniques.

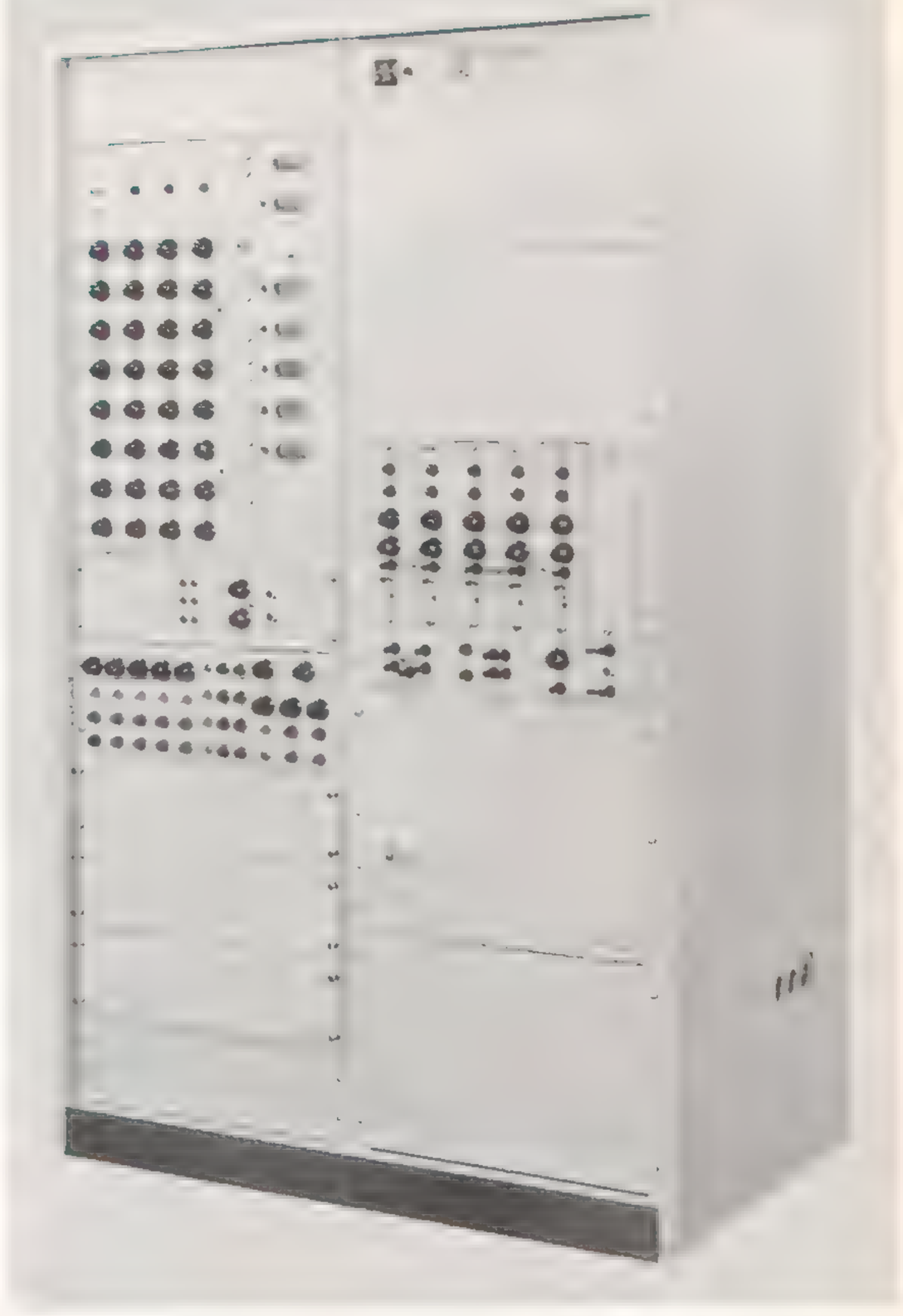
The Type 1516 tester is a completely integrated system containing power supplies, current drivers, logic switching, timing circuits, and other components necessary for the testing of coincident current memories of up to 128 by 128 cores per plane. It can be programmed to switch sequentially through as many as 64 planes. In addition, the Type 1516 can test word address memory planes of up to 128 words by 64 bits with the 2:1 or 3:1 selection schemes, one core per bit or two cores per bit, and wiring configurations of 2, 3 and 4 wire patterns. The tester requires no supplementary equipment other than oscilloscope and memory jigs.



2200 SERIES MEMORY EXERCISERS

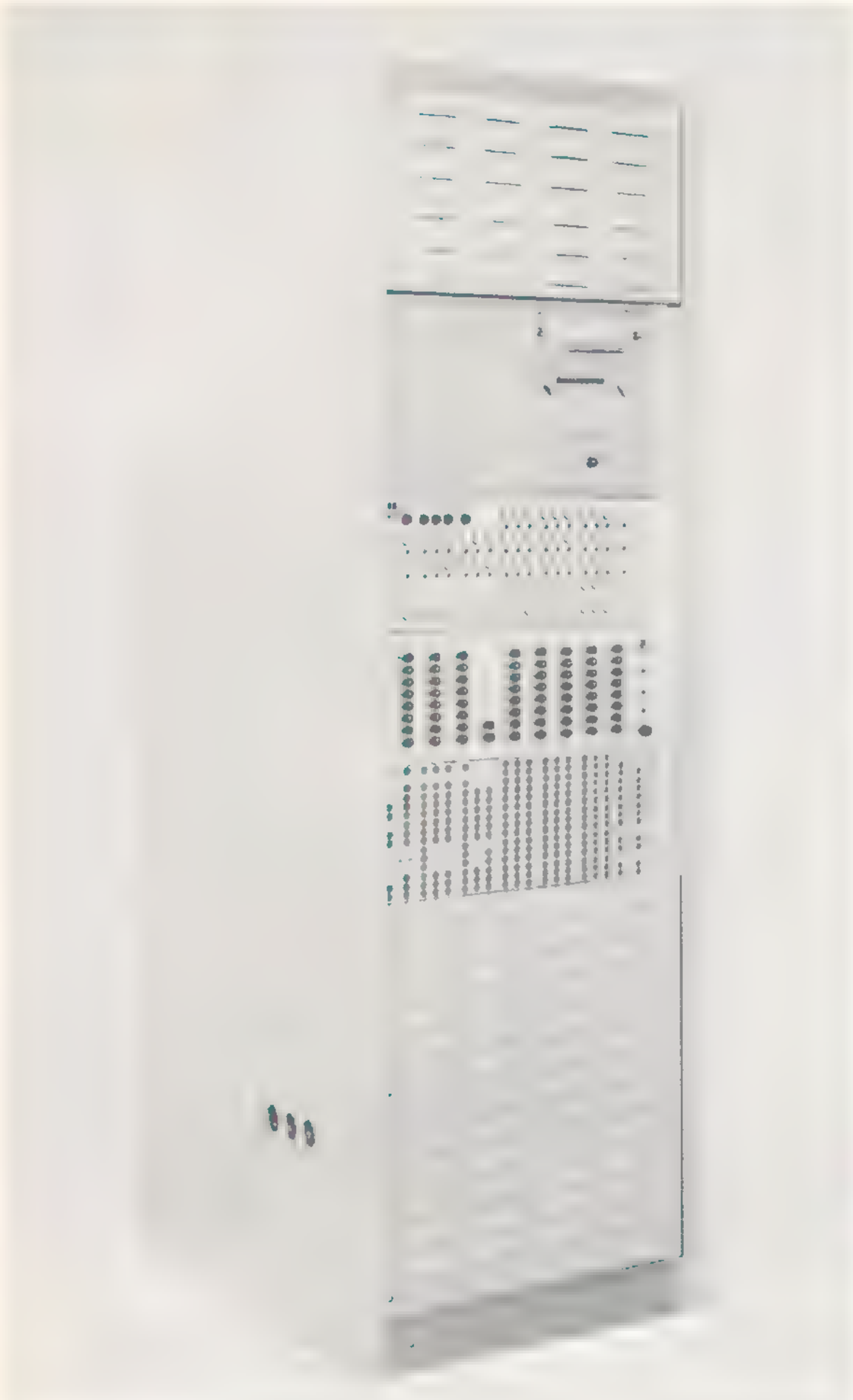
Digital 2200 Series Memory Exercisers are designed to test both coincident current and word address memory systems up to 128 by 128 by 64. They write a variety of patterns into memory and then read these patterns out again, checking for errors. The machines can be programmed to stop on an error, indicating the exact address and digit location of the defective bit. The several modes of operation and many patterns of information available can serve to simulate the most extreme noise conditions of actual computer operation. Completely variable timing allows for ease of set up and marginal checking of all types of memory systems. Output bus drivers with variable output voltage levels solve the problem of interface connections with many different systems.





2100 SERIES MEMORY CORE TESTERS

Digital 2100 Series Memory Core Testers are completely integrated systems for the automatic production-line testing of ferrite magnetic memory cores. The systems operate in conjunction with conventional core feeding devices and use decision making logic which can be programmed to accept or reject cores to a large variety of specifications. The 2100 Series Testers furnish a number of different programs of current driving pulses, completely variable in timing and amplitude, and a calibrated sensing system which measures core output at five specific strobe times against six known variable amplitude levels.



2000 SERIES MEMORY BUFFERS

Digital 2000 Series Buffer Memory Systems are completely self-contained. They normally include a counter register, general purpose registers, and a random access memory system, consisting of a memory address register, a memory buffer register, and a coincident current magnetic core memory. Control Panels contain indicator lights for all register bits, push buttons for manual setting and clearing of the counter and general purpose registers, and a keyboard input for manually loading the memory. Input and output jacks enable the systems to be completely integrated with outside control systems.

OTHER SPECIAL SYSTEMS

Digital has the staff and facilities for complete, in-house production of special digital systems of many types. The scanner shown above is typical of such a system, incorporating both electronic and mechanical design and construction. Circuit modules, power supplies, panels, and custom mechanical parts can all be manufactured within the Digital plant. Sub-assembly, final assembly and check-out are done under the same roof. Thus the customer not only gets top-grade electronic design service; he also gets step-by-step supervision of the entire construction operation, from the testing of basic components through crating for delivery.

PROGRAMMED DATA PROCESSOR-1

Digital's Programmed Data Processor-1 is a compact, solid state, general purpose digital computer. It has transistorized logic circuits based on the DEC line of Digital Modules, an expandable random access core memory with a cycle time of five microseconds, and 18-bit fully parallel processing. These design features give the PDP-1 a computation rate of 100,000 additions per second including two calls on memory. Key programming features are multiple-step indirect addressing, 12 variations of arithmetic and logical shifting, 15 conditional instructions, and capability for Boolean operation. The PDP-1 is engineered to accommodate a variety of input-output equipment without internal machine changes. Standard equipment items are an alphanumeric typewriter for on-line input and output, a punched tape reader, a punched tape punch, and single-channel automatic interrupt. The PDP-1 operates on ordinary 110-volt current and requires no special wiring, subflooring or air conditioning.

PROGRAMMED DATA PROCESSOR-4

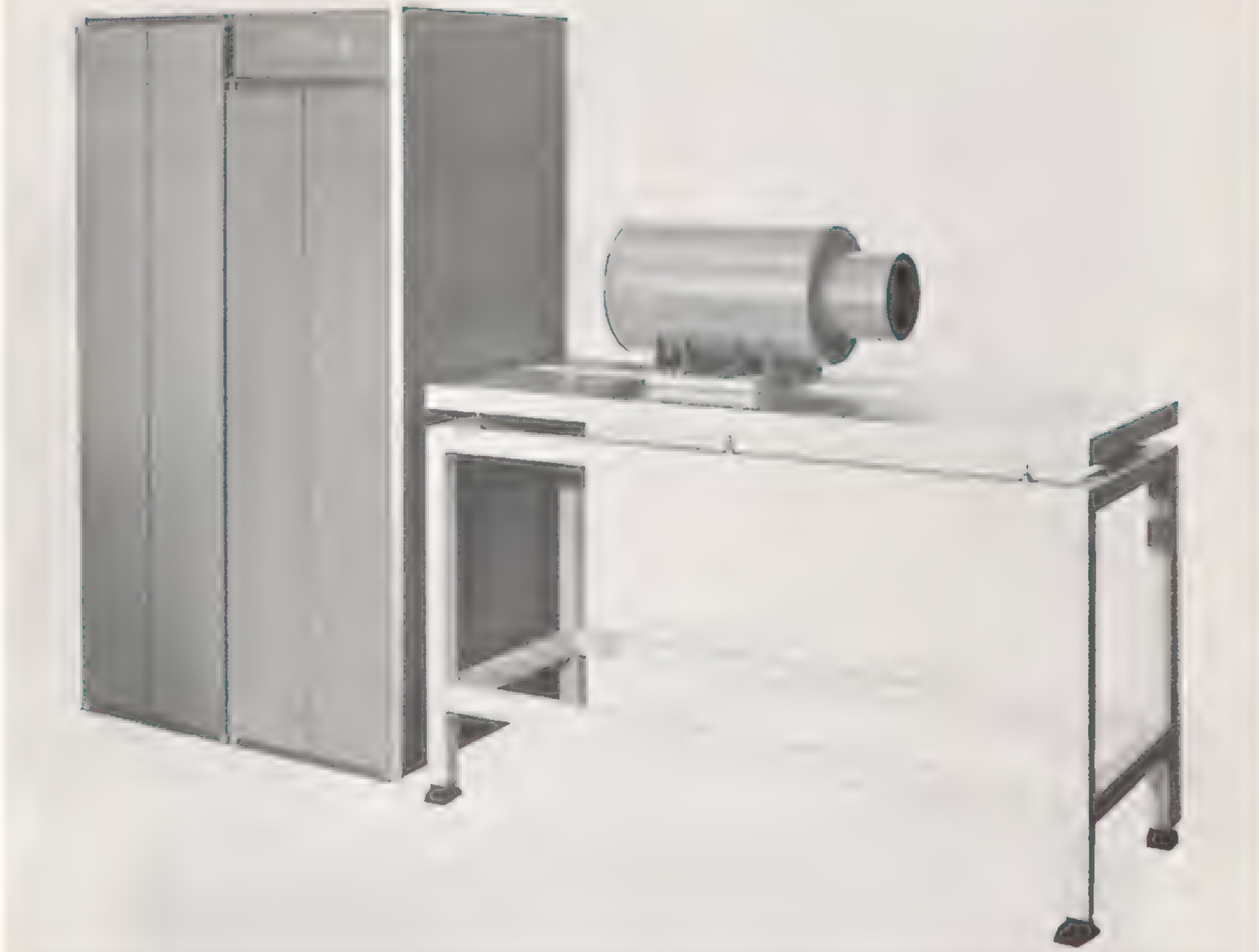
The Programmed Data Processor-4 (PDP-4) is designed to be the control element in an information processing system. PDP-4 is a single address, parallel, binary machine with an 18-bit word length using one's or two's complement arithmetic. Standard features of the machine are stored program operation, a random access magnetic-core memory, a complete order code, and indirect addressing.

Standard core memory size is 1024 or 4096 words, expandable to 8192 words. The memory cycle time is 8 microseconds. Instruction enactment times are multiples of the 8-microsecond memory cycle, with two-cycle instructions such as add, deposit, load, etc., performed in 16 microseconds. Indirect addressing requires an additional 8 microseconds.

Flexible, high-capacity input-output capabilities of the PDP-4 enable it to operate in conjunction with a variety of peripheral devices, such as perforated-tape readers and punches, punched-card readers and punches, teletype printer-keyboard, line printers, magnetic tape transports, and analog-to-digital converters.

VISUAL CRT DISPLAY TYPE 30

The Type 30 is a 16-inch cathode ray tube display for the presentation of graphic or tabular data to the operator. The "display" command will plot one point on the tube at the position indicated by the Accumulator and the In-Out Register. Plotting a point requires approximately 50 microseconds. For each display instruction, one point is displayed. The first 10 bits of the IO Register, bits 0 through 9, are the Y coordinate of the point. Bits 0 through 9 of the Accumulator are the X coordinate of the point. Information is displayed at a rate of 20,000 points per second.



PRECISION CRT DISPLAY TYPE 31

The Type 31 is equipped with a 5-inch cathode ray tube for precision data display. One bit is displayed for each display instruction. Bits 0 through 11 of the IO register are the Y coordinate of the point, and Bits 0 through 11 of the accumulator are the X coordinate. This unit has a mounting bezel to accept a camera or a photomultiplier device. The display head is mounted on a massive shock-mounted table. The table top has a precision surface for accurate and stable mounting of viewing devices.

LIGHT PEN TYPE 32

The Type 32 Light Pen is a photosensitive device which allows information to be "written" on the cathode ray tube of the Visual Display Type 30 or the Precision Display Type 31. The pen detects displayed information, and the pen output sets a program flip-flop in the machine each time a pulse of light strikes the pen. The Type 32 is particularly useful for such applications as trace monitoring, pattern recognition and data manipulation.

TAPE TRANSPORTS TYPE 50 AND AUTOMATIC TAPE CONTROL UNIT TYPE 52

Digital Tape Transports read and write IBM 727 and 729 I format tape. Two hundred 7 bit characters of information are stored on each inch of tape, and the tape is read or written at the rate of 75 inches per second.

The Type 52 Tape Control Unit automatically transfers information between the computer memory and the tape in blocks of characters. It allows computation to continue while the transfer is in process, and it does automatic error detecting while reading and writing. One to eight Tape Transports can be controlled by each Type 52 Control Unit.

AUTOMATIC LINE PRINTER AND CONTROL TYPE 62

The Type 62 is an on-line printing station capable of operating at 600 lines per minute (120 columns per line with 64 characters per column). A simple one-line buffer is used. The appropriate iot instruction is repeated to fill the buffer. The order to print is then given. Following the completion of the line print, the printer returns a completion pulse. Spacing of paper is controlled by an eight channel format type. The space paper command selects the format channel to give single space, double space, page space, etc.

OTHER PDP-1 OPTIONS

The optional equipment shown in the preceding section illustrates the wide choice of input-output devices available to expand the capabilities of the PDP. Additional external equipment and the Central Processor options are described below.

CENTRAL PROCESSOR OPTIONS

MULTIPLY/DIVIDE TYPE 10

The order "Multiply Y" forms the double length product of the contents of the Accumulator and the contents of Memory Register Y. The instruction "Divide Y" forms the quotient of the double length dividend (stored in the Accumulator and In-Out Register) and the divisor contained in Register Y. Divide normally skips the following instruction. If an overflow occurs, the skip does not occur. Multiplication requires 25 microseconds maximum, and divide takes 40 microseconds maximum.

MEMORY MODULE TYPE 12

Each memory module consists of 4096 18-bit words. A maximum of sixteen modules may be connected to the PDP-1.

MEMORY EXTENSION CONTROL TYPE 15

The Type 15 allows for memory expansion of up to fifteen additional memory modules.

HIGH SPEED CHANNEL CONTROL TYPE 19

The Type 19 is used to transfer blocks of words between memory and three in-out devices. Such a channel is installed with the Tape Control Unit Type 52 or may be installed separately for special applications.

INPUT-OUTPUT OPTIONS

SEQUENCE BREAK TYPE 20

This automatic interrupt feature allows concurrent operation of several in-out devices and the main sequence. The system has 16 automatic interrupt channels arranged in a priority chain. An interrupt or break can be initiated by an in-out device at any time. When a break occurs, the states of the arithmetic and control elements are automatically stored in memory, and program control is transferred to a routine which deals with the device causing the interrupt.

CARD PUNCH CONTROL TYPE 40-523

The Type 40-523 Control operates a standard card punching machine. It contains an 80 bit buffer which is loaded from the In-Out Register, using the "In-Out Transfer" command, for each card row punched. The control is for use with a 523 Summary Punch at speeds of 100 cards per minute.

CARD READER CONTROL TYPE 41-523

The Type 41-523 Control is for use with standard card reading equipment. It allows the read brush outputs to be directed to the In-Out Register. The control is for use with a 523 Summary Punch at speeds of 100 cards per minute.

PROGRAMMED TAPE CONTROL UNIT TYPE 51

The Type 51 Control transfers information between the computer and the tape one character at a time. All transfer options, including error checking and assembly of characters into computer words, are performed by routines. The Type 51 allows a choice of tape format, including the IBM Type 729 Mod I.

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PRINTER-KEYBOARD AND CONTROL TYPE 65

The Type 65 Printer-Keyboard and Control, optional for the PDP-4, is a Teletype Model KSR-28 Printer and Keyboard with an input and printing speed of 10 characters per second. A five-bit code represents the character. The printing (output) and keyboard (input) functions have separate commands and control logic. The signals to and from the Printer-Keyboard to the control logic are standard, serial, 7.5 unit code Teletype signals.

PAPER TAPE PUNCH AND CONTROL TYPE 75

The Type 75 Paper Tape Punch and Control, optional for the PDP-4, is a Teletype BRPE Punch with an operating speed of 63.3 lines or characters per second. It perforates 5, 7 or 8 hole tape.

OTHER PDP-4 OPTIONS

In addition to the Printer-Keyboard and Control Type 65 and the Paper Tape Punch and Control Type 75, several of the PDP-1 input-output options shown on Pages 402-406 are also optional for the PDP-4. These include the Visual CRT Display Type 30, Light Pen Type 32, Magnetic Tape Transport Type 50, Magnetic Tape Control Type 54, and Automatic Line Printer and Control Type 62.

CENTRAL PROCESSOR OPTIONS

MEMORY MODULE TYPE 17

Each Memory Module Type 17 consists of 4096 words. One module may be added to the basic PDP-4 to form an 8192-word memory. Additional modules require the use of a Memory Extension Control Type 16.

MEMORY EXTENTION CONTROL TYPE 16

The Type 16 extends the memory control capability of the PDP-4 from 8192 words to 32,768 words.

DRUM SYSTEM TYPE 18

The Drum System operates on a serial transfer basis in 256-word blocks. It is available in three capacities — 16, 32 and 65 thousand words.

EXTENDED ARITHMETIC CONTROL UNIT TYPE 22

This unit, essentially an extension of the Accumulator, gives the computer a multiply and divide capability without the use of subroutines.

REAL TIME OPTION TYPE 25

The Type 25 Real Time Option greatly increases the flexibility of the PDP-4 by providing these additional functions:

Device Selection — consists of decoding elements which produce pulses when the iot instruction corresponding to its address is given. The pulses may be used to (a) set or reset control flip-flops, (b) read in information to an external register from PDP-4 through the Information Distributor, and (c) read in information to PDP-4 from external registers or devices through the Information Collector. The standard DS contains provisions for up to 20 selector elements.

Information Collection — allows for the collection of information appearing in the form of static levels. A total of 8 times 18 signals may be interrogated.

Information Distribution — permits the distribution of the information contained in the AC to all connected devices. Eight groups of 18 outputs are available in the ID.

In-Out Skip Facility — allows PDP-4 programs to skip according to various extra machine states. There are 16 inputs to the IOS.

Program Interrupt — permits certain conditions to interrupt the program. Any one of 10 signals may cause an interruption of a program. When the interrupt occurs, the contents of the PC are stored in memory location 0. The subroutine begins in memory location 1.

Data Interrupt — allows a device to interrupt the program and transmit data directly to or receive data directly from the memory.

Real Time Clock — provides a signal which may interrupt the program. This signal is used to provide a stable real time reference.

INPUT-OUTPUT OPTIONS

THE CARD READER AND CONTROL, TYPE 41-200-4

Cards are read at a rate of up to 200 cards per minute, column by column. Column information may be read in alphanumeric or binary mode. The alphanumeric mode converts the 12-bit Hollerith Code of one column into the six-bit binary-coded decimal code with code validity checking. The binary mode reads a 12-bit column directly into the PDP-4. Approximately 1.0 per cent of a Card Reader program running time is required to read the 80 columns of information at the 200-cards-per-minute rate.

THE CARD PUNCH CONTROL, TYPE 40-523-4

The Type 40-523-4 enables the operation of a standard IBM Type 523 Summary Punch with PDP-4. Cards are punched on a row-by-row basis at a rate of 100 cards per minute. Approximately 0.3 per cent of program running time is required to operate the Card Punch at the 100-cards-per-minute rate.

THE 18-BIT RELAY BUFFER TYPE 67

This option provides contacts which operate devices of higher power rating. The relays have form "D" contacts, which open and close in approximately 3 milliseconds.

SUPPLEMENTARY PAGES

FOR

digital MODULES CATALOG

Please insert these pages in the pocket provided for this purpose on the inside back cover of your catalog.

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DIGITAL

digital

MODULE ACCESSORIES

53-63

CURRENT DRIVERS

The DEC Types 53 Negative and 63 Positive solid-state Current Drivers provide shape-controlled, constant current pulses of up to 1 amp to variable loads. DEC Logic Modules, used in conjunction with these current drivers, generate complex current pulse sequences for thorough evaluation of magnetic memory core characteristics under all operating conditions. The high impedance output of the driver ensures a fixed driving current even during changing back voltage of up to 50 volts.

The circuit, similar for negative and positive drivers, can be considered in two parts. The first part generates a trapezoidal control voltage, and the second converts the control voltage to an output current. The duration of the current corresponds to the duration of the input signal. Linear rise and fall slopes are generated by a Milier integrator. The current for charging the integrating capacitor is fixed, but the discharge current may be varied to establish a symmetrical control voltage. High speed transistors with high power and voltage ratings convert the trapezoidal control voltage to a trapezoidal output current pulse.

CONTROLS: Coarse and fine amplitude controls, on concentric shafts, permit the pulse current to be set between 10 ma and 1 ampere (with a maximum average output current of ¼ ampere). Two additional fine amplitude controls on concentric shafts may be independently switched-in; each increases the output current by an amount variable from 8.0 to 150 ma. Coarse and fine slope controls establish the duration of the linear current rise, variable from 50 nanoseconds to 1 microsecond over the full range of output currents. The fall trim control adjusts the duration of the linear current fall ±10% so that it can be made equal to rise time.

INPUT: Ground produces no output; a −3 volt level input produces an output pulse of the same duration as the input. The load is 1 unit of 5 megacycle Base Load. The maximum repetition rate is 2 megacycles. Input connections may be made on the front or rear panel of current drivers with DEC Type 911 Patch Cords.

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OUTPUT: 50 ma to 1 ampere current pulses with linear rise and fall are generated for back voltages up to 50 volts (20 volts if no extra supplies boost the output of the DEC Type 766 Power Supply). The minimum output impedance is 5000 ohms at 1 ampere current; it is considerably higher at lower currents. Droop and overshot are less than 1%. Amplitude jitter is less than 0.1%. The nominal temperature coefficient of the output current is 0.02%/°C. The duty factor is limited to 50% for pulse currents up to 500 ma; at higher pulse amplitudes it is limited by the maximum average output current rating of 250 ma.

Output terminals are binding posts on ¾" centers which accept double banana plugs. Positive and negative drivers may be paralleled in any combination for pulse mixing or to obtain higher currents.

DIMENSIONS: Up to six current drivers (2½" wide x 10½" high x 10½" deep) or four drivers and one current/voltage calibrator fit into one DEC Type 1913 19" mounting panel.

POWER:* Type 53: +35 volts DC/0.2 ma; −35 volts DC/253 ma + average output current; − 45 volts DC/96 ma. **Type 63:** +45 volts DC/75 ma; +35 volts DC/275 ma + average output current; −35 volts DC/9.5 ma.

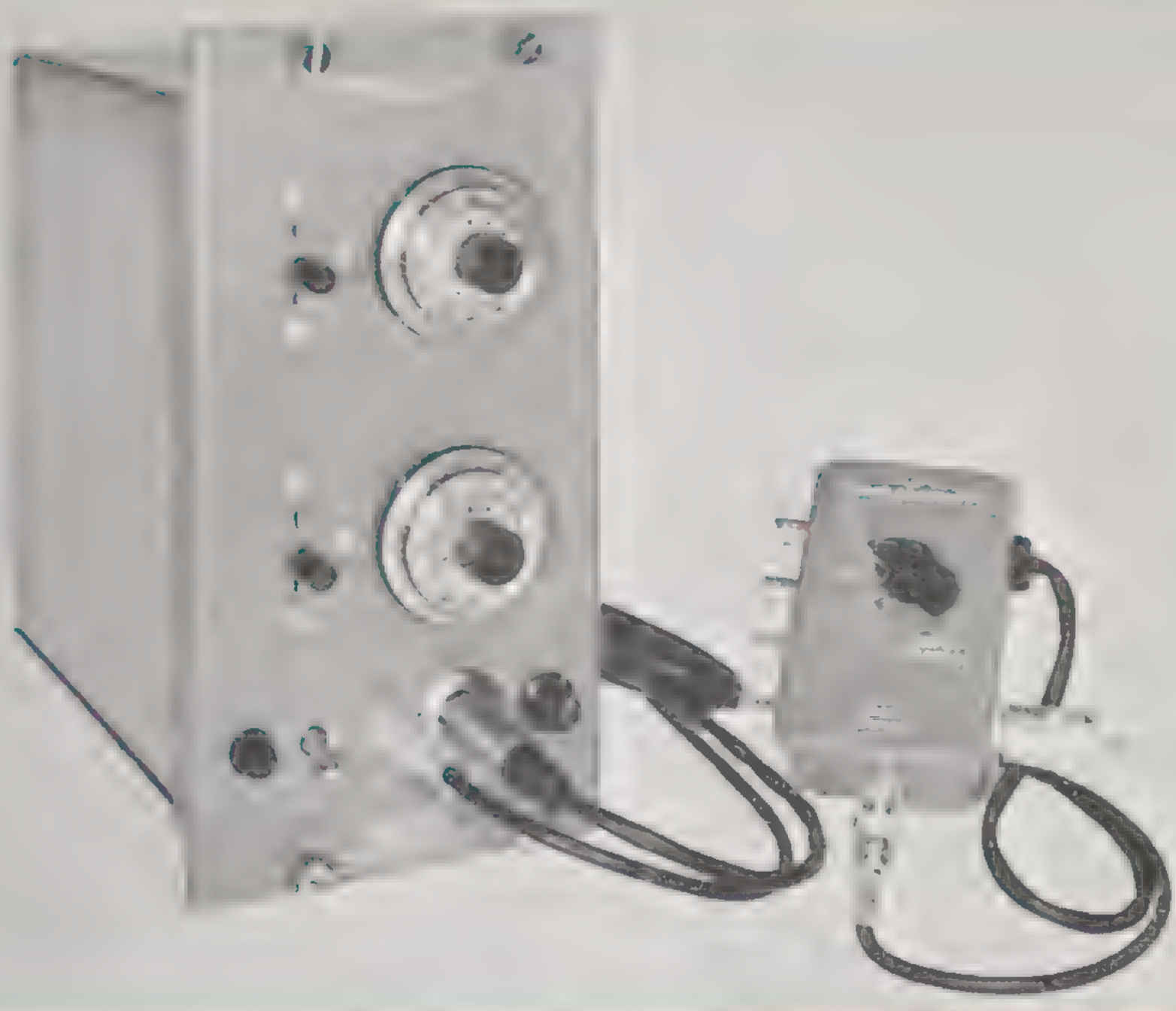
*These data apply for drivers operating from a DEC Type 766 Power Supply. Supplies used to provide additional back voltage supply only the average output pulse current.

d g i t a l

MODULE ACCESSORIES

72

CURRENT VOLTAGE CALIBRATOR



The Type 72 Calibrator provides high accuracy measurement of current and voltage pulses, which makes it an ideal companion for the Types 53 and 63 solid-state or the Types 51 or 61 vacuum-tube current drivers. The calibrator generates two precise reference voltages using Zener regulated voltage supplies and resistive dividers with very low temperature coefficients. High-precision, high resolution decade potentiometers with ±0.01% linearity control the reference amplitudes.

To superimpose the reference and input waveforms for comparison on a display oscilloscope, two mercury-wetted contact relay choppers provide commutation between the reference voltages and the input signal. A compact box containing one of these relays mounts directly on a standard type VHF connector, such as is used on most oscilloscope plug-in preamplifiers. This box also houses a selector switch and four BNC connectors which allow up to four signal sources to be connected to the box, and displayed at will. A small printed circuit board makes all connections, providing short leads and consequently negligible distortion of fast-rise signals. For minimum distortion, series resistors used for measuring current pulses are located near the device under test. Relay drive power and the reference signal for the small relay box come from the connectors on the main calibrator front panel.

CONTROLS: The on-off switch controls the power for the reference supplies and for the time-sharing choppers. The selected input is displayed when the switch is off. The reference controls are calibrated in increments of one tenth millivolt from zero to one volt. A three position lever switch for each reference makes it positive or negative, or grounds it. The dwell control apportions the display time between the references and the input signal, which permits control of their relative brightness. The input selector switch, located on the oscilloscope box, connects one of the four input connectors to the time-sharing commutator.

INPUT: Four standard BNC female connectors on the small relay box accept inputs between −1 volt and +1 volt.

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OUTPUT: A standard VHF male connector fixed to the relay box provides both mechanical and electrical connection to the display oscilloscope. The output resistance of the reference voltage sources is nominally 1000 ohms/volt. Error is limited to less than ±0.08% ±0.2 mv at 23°C, when calibration is performed under controlled line voltage conditions, such as in a DEC magnetic core, plane, or memory testing system using a harmonically corrected line voltage regulating transformer. The temperature coefficient of the reference voltage is within ±50 parts per million/°C for the operating range of 0°C to 50°C. When operated without line regulation, reference error is limited to ±0.28% ±0.2 mv for line voltages from 105 to 125.

POWER: The input power is less than 10 watts at 115 volts AC, 50-60 cycles. The plug on the back panel is a standard three-prong grounded plug.

d g t l

COMPUTER OPTIONS

31

ULTRA PRECISION CRT DISPLAY

The DEC Ultra Precision CRT Display Type 31 is a 5-inch random position, point-plotting cathode ray tube. It is a highly stable, precision device, with built-in deflection and focus correction and meets the particular needs of those requiring a high degree of resolution. The Type 31 is especially suited for photographic recording of digital output data and may be used in combination with a photomultiplier as a precision programmed spot scanner for the input of photographic data to digital computers. Upon command, it will display a single point at any location on a 3-inch by 3-inch raster, the coordinates of which are specified by two twelve-bit words, one for each axis. The unit has a mounting bezel to accept a camera or a photomultiplier mounting adapter. The display head is mounted on a massive shock-mounted table. The table top has a precision surface for accurate and stable mounting of viewing devices.

The Type 31 consists of two major sections. One section contains two bays of equipment joined together to form a cabinet; the other section is a massive shock-mounted table providing support for the CRT housing. The table is clamped to the right of the cabinet with the CRT housing mounted near the cabinet. Half-width doors on the front and rear of each bay of the cabinet provide access to the interior for installation and maintenance. When closed, the doors on the rear are sealed to prevent loss of the forced-air cooling convection currents. A fan in the bottom of each bay draws cooling air into the cabinet and forces it over the electronic components and out the front of the cabinet. Construction is solid state throughout with excellent stability.

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OPERATING SPECIFICATIONS

INPUT POWER: 115 volt, 15 ampere; 60 cycle, single phase power.

POWER CONTROL: A.C. power is supplied to the display through a modified Type 811 Power Control, which can be turned on either by an external −15 volt, 5 milliampere level or by a toggle switch located on the Power Control. A circuit breaker in the Control can also be used to turn power on or off.

ADDRESSING SCHEME: 1's complement with +0= −0 at the center.

RASTER SIZE: 3 inches by 3 inches maximum, 4096 x 4096 addressable locations.

CATHODE RAY TUBE: C5A24S 5-inch flat face tube.

DEFLECTION: Corrected magnetic deflection.

FOCUS: Magnetic with dynamic focus correction.

UNDEFLECTED SPOT SIZE: .004 inch visually to edge of spot.

DEFLECTION SETUP TIME: 35 microseconds.

INTENSIFICATION TIME: 10 microseconds.

TOTAL TIME TO DISPLAY ONE POINT: 50 microseconds including information transfer time.

REPEATABILITY: On a short term basis, any point will fall within 0.01 inch of its previous location regardless of the location from which it came.

STABILITY OF (0, 0) POINT: ±0.2% of raster size for a 10°C. change in temperature over an eight hour period.

OVERALL ACCURACY OF DISPLAYED POINTS: ±0.5% of raster size.

INTENSIFICATION CIRCUIT: One intensify input and one level of intensity are available on the standard Type 31 Display. Six input OR gates and eight voltage levels of intensity are available upon special order. Rise and fall times are less than 0.6 microsecond.

INDICATORS: All buffer and control flip-flops have visible panel indicators.

OPERATING TEMPERATURE RANGE: 20°C. to 50°C.

PHYSICAL SPECIFICATIONS

WEIGHT OF CABINET: 1000 pounds.

WEIGHT OF TABLE AND HOUSING: 400 pounds.

DIMENSIONS OF CABINET: 27¼ inches wide, 41¼ inches deep, 67¼ inches high.

DIMENSIONS OF TABLE: 60 inches wide, 22 inches deep, 35 inches high.

DIMENSIONS OF CRT HOUSING: 17½ inches wide, 26 inches deep, 17¾ inches high.

FLOOR LOADING OF CABINET: 8 swivel, castered support points at 125 pounds per point.

FLOOR LOADING OF TABLE AND HOUSING: 4 rubber shock-mounted support points at 100 pounds per point.

SERVICE CLEARANCE: 3 feet clearance required all around display.

TABLE TOP: 2 inches thick magnesium milled to a flatness of 0.005 inch per foot. Six adjustable points are available for levelling the table top.

INTERFACE CONNECTIONS

INPUTS:* 12 levels for each axis are required. These must be present for 2.5 microseconds before a display pulse is supplied. In addition to the levels, a standard DEC negative 2.5 volt 0.4 microsecond pulse must be supplied for each point to be displayed to clear the display buffer followed, a minimum of two microseconds later, by another DEC standard negative pulse to load the buffer with the 24 information bits.

OUTPUTS:* 45 microseconds after the display pulse is provided a completion pulse will be emitted. This pulse is a standard DEC 3 volt negative pulse.

*Other pulse and level amplitudes are available upon request.

d g t l

COMPUTER OPTIONS

40-523

CARD PUNCH CONTROL

The Type 40-523 Control allows for on-line, buffered operation of an IBM Model 523 card punch. It contains an 80 bit buffer, which is loaded from the In-Out Register using five "In-Out Transfer" commands for each card row punched. Since any or all punching positions may be used, the standard IBM format is not a restriction and any format may be used. Maximum speed of the punch is 100 cards per minute.

PHYSICAL SPECIFICATIONS

PUNCH DIMENSIONS: 40 inches wide, 26 inches deep, 50 inches high.

PUNCH WEIGHT: 678 pounds.

CONTROL DIMENSIONS: 21¾ inches wide, 27 inches deep, 35¾ inches high.

CONTROL WEIGHT: 260 pounds.

OPERATING SPECIFICATIONS

POWER REQUIREMENTS: 115 VAC, 60 cps, 11 amperes.

PUNCH SPEED: 100 cards per minute.

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The Type 41 provides on-line reading of standard punched cards. The cards are read lengthwise and sensed optically. They may be read in the Alpha-numeric or Binary mode at rates up to 200 cards per minute. Output is 6 parallel bits. The Alpha-numeric mode converts the 12-bit Hollerith code of one column into the 6-bit binary-coded decimal code with code validity checking. The Binary mode reads a 12-bit column directly into the computer. Hopper and stacker capacity is 500 cards.

PHYSICAL SPECIFICATIONS

DIMENSIONS: 42½ inches high, 29⅞ inches long, 18 inches deep. With computer cable attached add 7 inches to the depth.

WEIGHT OF READER: 100 pounds including supporting base. This weight rests on 4 casters at the corners of the supporting base.

Weight of Reader and Control: 678 pounds.

MECHANICAL: Access to the inside of the reader mechanism by removal of 3 panels (with 3/16 inch Allen wrench). The line filter, power supply filter capacitor, connector, connector mount and cable are inside the supporting base.

ENVIRONMENT: The reader and control will operate from 40°F to 105°F ambient temperature and from 10% to 90% relative humidity. Since only 130 watts are dissipated as heat in the reader, no active cooling methods are used. The reader control is mounted inside the computer and is cooled by forced air.

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ELECTRICAL SPECIFICATIONS

POWER REQUIREMENTS: 115 VAC ±5%; 60 cycles; maximum allowable turn-on transient= 2.5 times nominal line voltage for ½ cycle; minimum turn-on transient= .7 times nominal voltage for ½ cycle; current consumption= 1.2 amps steady-state and when reading cards.

EXTERNAL CONNECTIONS: A.C. for the reader comes directly from the common power line through a line filter and toggle switch. The reader attaches to its control circuitry with a 25 foot cable with Amphenol 50-pin connectors (male) on each end. The female receptacle is flush-mounted in the reader support base.

515

INFORMATION REQUEST

INFORMATION REQUEST

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REVISED EDITION

The Digital Logic Handbook has been enlarged and is now included in the first 83 pages of this new catalog

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